Transient-Induced Latchup in CMOS Technology: Physical Mechanism and Device Simulation

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Abstract

The physical mechanism of transient-induced latchup (TLU) in CMOS ICs has been clearly characterized by device simulation and experimental verification in time domain perspective. An underdamped sine-wave-like voltage has been clarified as the real TLU-triggering stimulus under system-level electrostatic discharge (ESD) test. The specific "sweep-back" current caused by the minority carriers stored within the pnpn structure of CMOS ICs has been qualitatively proved to be the major cause of TLU.

Introduction

Transient-induced latchup (TLU) will increasingly be a primary reliability issue in CMOS IC products [1], [2]. This tendency is caused by several reasons. First, there are much more complicated implementations of circuitry such as mix-signal, multiple power supplies, RF, SOC, etc. The environment where these CMOS devices locate will suffer from a lot of noises coming from both the interior and exterior of ICs to induce TLU more easily than before. Second, more and more ICs are rather susceptible to TLU under a strict-demanded system-level ESD test [3]. During this test, electromagnetic interference (EMI) coming from the ESD zapping gun will be coupled into the ICs of the system. Such EMI-generated transient voltage can range from about several tens to hundreds volts on the power lines of ICs to cause TLU failures [4]. Third, aggressive scaling of device feature size and clearance between the PMOS and NMOS leads to the parasitic silicon controlled rectifier (SCR) in CMOS ICs exhibiting a worse immunity against latchup.

Unlike a single positive or negative current pulse [5], an underdamped sine-wave-like voltage [6] which can reflect the real TLU-triggering stimulus under system-level ESD test is used for TLU characterization in this work. The physical mechanism of TLU has been clearly explained in time domain by device simulation. All the simulation results on TLU have been verified in silicon chips fabricated by 0.25-μm CMOS technology.

Test Structure and Measurement Setup

The device cross-sectional view and layout top view of the parasitic SCR structure in CMOS ICs for TLU measurements are sketched in Figs. 1(a) and 1(b), respectively. The geometrical parameters such as *D*, *S*, and *W* represent the distances between well-edge and well (substrate) contact, anode and cathode, and the adjacent contacts, respectively. The SCR structure shown in Fig. 1(a) is also used in the two-dimensional device simulation tool (MEDICI) for TLU characterization under different geometrical parameters.

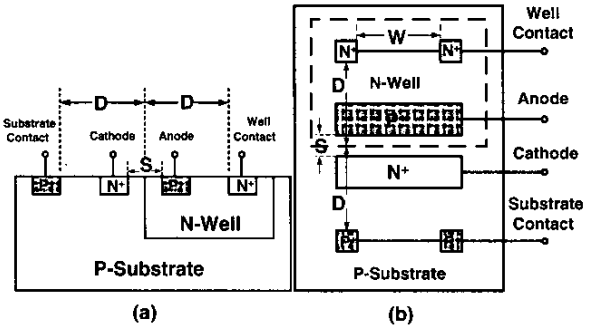

Fig. 1. (a) Device cross-sectional view, and (b) layout top view, of the SCR structure for TLU measurements.

The typical measurement setup for TLU test [4] is depicted in Fig. 2. An electrostatic-discharge simulator is used as the TLU-triggering source, V_{Charge}, to supply an underdamped sine-wave-like voltage. For example, with V_{Charge} of +10V (or -2V), the inset figures in Fig. 2 show the measured underdamped sine-wave-like voltage waveforms on V_{DD} of CMOS ICs, which are similar to the real situation under the system-level ESD test.

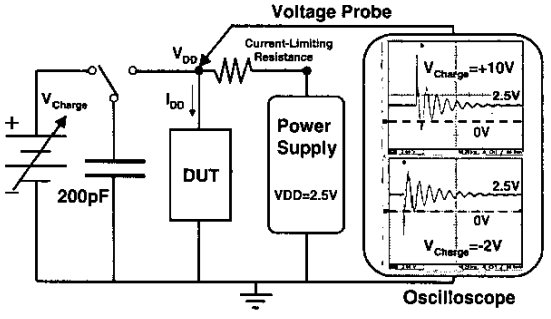

Fig. 2. The typical measurement setup for TLU test.

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Device Simulation

The simulated latchup DC *I-V* characteristic in an SCR structure with layout parameters of D=6.7μm and S=1.2μm is performed in Fig. 3. In CMOS ICs, the P+ anode (source of PMOS) and the N+ well contact in Fig. 1(a) are connected to V_{DD}. Whereas, the N+ cathode (source of NMOS) and the P+ substrate contact in Fig. 1(a) are connected to ground. When the latchup occurs, the parasitic SCR structure will cause a low-impedance path from V_{DD} to ground. A huge current will be conducted from V_{DD} to ground through this low-impedance path, which generates the heat to burn out the chip. Clearly, under a latchup state, when the power-supply voltage, V_{DD}, keeps at its normal operating voltage, +2.5V, the total power-supply current, I_{DD}, flowing into both anode and well contact is about 150mA in Fig. 3. This will be a vital evidence used to judge whether TLU certainly occurs in time domain through device simulation.

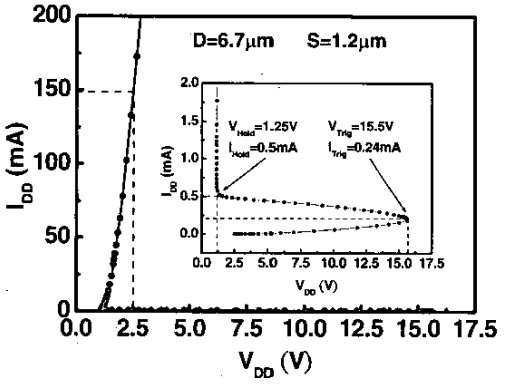


Fig. 3. The simulated latchup DC *I-V* characteristic in an SCR structure.

With a negative V_{Charge}, Fig. 4 shows the simulated V_{DD} and I_{DD} transient responses for TLU. Here a 20-MHz underdamped sine-wave-like voltage is used to meet the real situation [6]. First, during the period of 50ns≤t≤62.5ns, V_{DD} begins decreasing rapidly from +2.5V at t=50ns, and will eventually reach the negative peak voltage, $-V_{peak}$ (~ -8V), at t=62.5ns. Within this duration, the N-well/P-substrate junction is gradually becoming slightly reverse-biased when V_{DD} decreases from +2.5V to 0V, and even becoming forward-biased when V_{DD} drops below 0V. Thus, at t=62.5ns, the largest forward-biased N-well/P-substrate junction can generate the forward peak current, $-I_{peak}$ (~20mA). Next, during the period of 62.5ns<t≤75ns, when V_{DD} increases from $-V_{peak}$ to its normal operating voltage, +2.5V, the N-well/P-substrate junction will rapidly change from the forward-biased state to its original reverse-biased state. Meanwhile, inside the N-well (P-substrate) region, large number of stored minority holes (electrons) offered by the forward peak current at t=62.5ns, will be instantaneously "swept-back" to its original P-substrate (N-well) region. Thus, such "sweep-back" current, I_{Sb}, will produce a voltage drop while flowing through the parasitic P-substrate or N-well resistance. Once this voltage drop reaches to some critical value, the emitter-base junction of either vertical PNP or lateral NPN bipolar transistors in the parasitic SCR structure will be forward biased to further trigger on latchup. For example, Fig. 5 shows the simulated transient responses of both anode and well contact currents. It clearly proves where these stored minority carriers, Q_{Stored}, come from and when they will be "swept-back" to cause TLU.

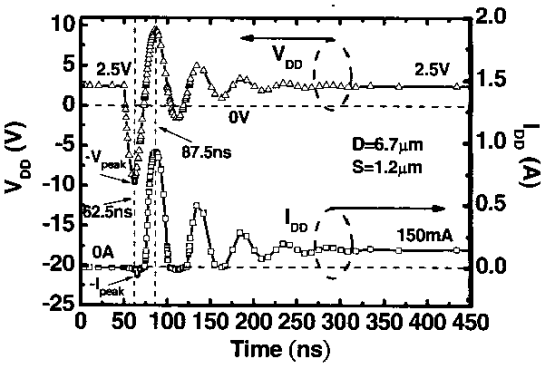


Fig. 4. The simulated V_{DD} and I_{DD} transient responses for TLU with a negative V_{Charge}.

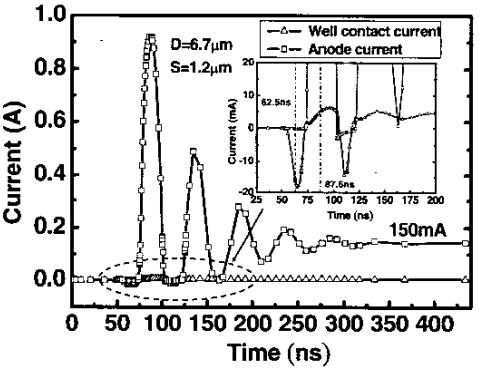


Fig. 5. The simulated transient responses of both anode and well contact current for TLU with a negative V_{Charge}.

To further judge whether TLU indeed occurs, Fig. 6 shows the corresponding simulated two-dimensional current flow-lines with respect to various transient timing-points with a negative V_{Charge}. From the simulation results in Fig. 6, TLU does appear right after the timing-point "C" (at t=75ns).

With a positive V_{Charge}, the simulated V_{DD} and I_{DD} transient responses for TLU are shown in Fig. 7. TLU definitely occurs when t>100ns because of large enough I_{Sb} produced during the period of 87.5ns≤t≤100ns.

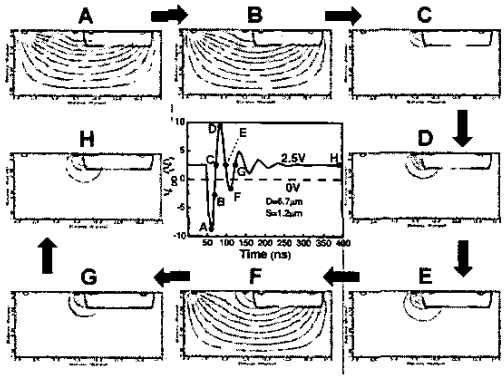


Fig. 6. The simulated 2-D current flow-lines with respect to various transient timing-points for TLU with a negative V_{Charge}.

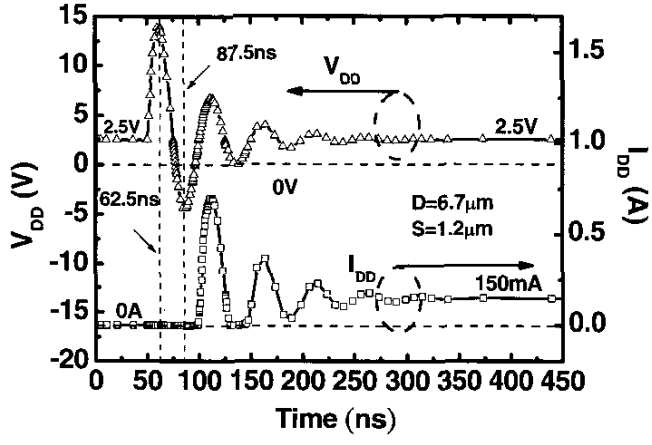
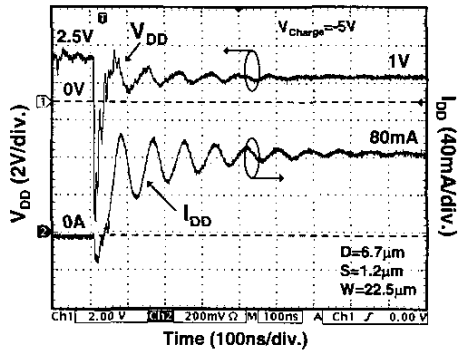


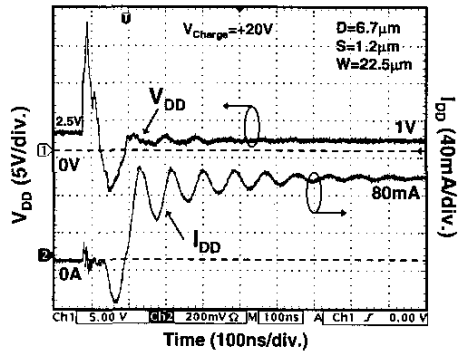
Fig. 7. The simulated V_{DD} and I_{DD} transient responses for TLU with a positive V_{Charge}.

Experimental Results

The SCR structure in Fig. 1 with layout parameters of D=6.7μm, S=1.2μm, and W=22.5μm has been fabricated in a 0.25-μm salicided CMOS process. The experimentally measured V_{DD} and I_{DD} transient waveforms on the SCR structure from the TLU test in Fig. 2 with V_{Charge} of -5V and +20V are shown in Figs. 8(a) and 8(b), respectively. In both cases, TLU will be triggered on due to large enough I_{Sb} while V_{DD} increases from $-V_{peak}$ to its normal operating voltage, +2.5V. As a result, this is fully consistent with the device simulation in time domain shown in Figs. 4 and 7. However, in device simulation, V_{DD} is not pulled-down to its latchup holding voltage (~1V) due to the native limitation of the device simulation tool for transient analysis. The occurrence of TLU can be ensured by observing the I_{DD} waveform. The current level of I_{DD} when the SCR structure triggered into latchup state can be estimated from Fig. 3 in advance.



(a)



(b)

Fig. 8. The measured V_{DD} and I_{DD} transient waveforms from the TLU test with V_{Charge} of (a) -5V, and (b) +20V.

Comparisons between TLU and Quasi-Static Latchup

In quasi-static latchup qualification test [7], TLU never occurs even if I_{Sb} indeed exists, as shown in Fig. 9. Obviously, I_{Sb} does exist when V_{DD} increases from its negative peak voltage, -5V, back to the normal operating voltage, +2.5V. However, latchup doesn't occur even though the under-going negative peak voltage is as low as -5V. To interpret this phenomenon, for simplicity, two reasonable assumptions are given here. First, N-well/P-substrate junction is treated as an ideal one-dimensional diode with step junction profile, as the inset figure shown in Fig. 10. Second, the storage time of minority carriers is assumed to be negligible because I_{DD} can rapidly follow the polarity variation of V_{DD}, as shown in Figs. 8 and 9. Therefore, from the first assumption, Q_{Stored} inside the N-well region can be expressed as

$$Q_{Stored} = \int_{X_n}^{X_n'} \left[P_n(x,t)\Big|_{t=t_B} - P_n(x,t)\Big|_{t=t_A} \right] dx, \quad (1)$$

where t_A (t_B) is the initial (final) timing-point of a specific duration when I_{Sb} exists. From the second assumption, Q_{Stored}

can be totally removed away when I_{Sb} exists, i.e. duration $t_A \le t \le t_B$. This duration in TLU test is much shorter than that in quasi-static latchup test, because V_{DD} has a rather short (about several tens of nanoseconds) damping period for TLU test but much longer (~μs) rise (fall) time for quasi-static latchup test. Thus, once these Q_{Stored} are swept back to the regions where they come from, the "average" I_{Sb} current, I_{Ave}, can be defined as

$$I_{Ave} \equiv Q_{Stored} / t_B - t_A. \quad (2)$$

In both TLU and quasi-static latchup cases, if the initial ($t=t_A$) and the final ($t=t_B$) voltages during $t_A \le t \le t_B$ are equal (i.e. with the same amount of Q_{Stored}), I_{Ave} in TLU case will be about 10^3~10^6 times larger than that in quasi-static latchup case. As a result, I_{Ave} is rather small and hard to trigger on latchup in quasi-static latchup test.

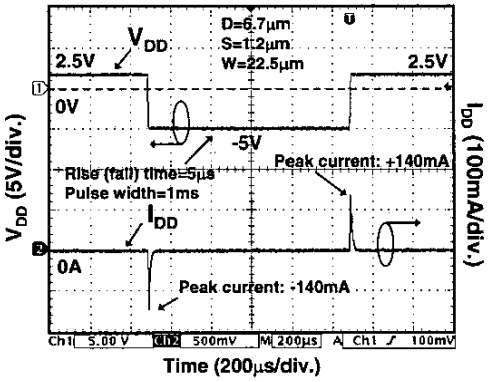


Fig. 9. The measured V_{DD} and I_{DD} transient waveforms from the quasi-static latchup test.

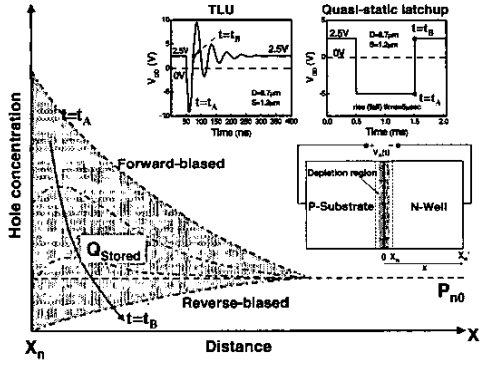


Fig. 10. The total stored minority carriers, Q_{Stored}, causing I_{Sb} ($t_A \le t \le t_B$) inside the N-well region.

Device simulation is also performed to verify the differences between TLU and quasi-static latchup. As shown in Fig. 11, although large forward current does exist within N-well/P-substrate junction (timing-points B-F), latchup never occurs due to a negligible I_{Ave} (timing-points G and H) in the quasi-static latchup test.

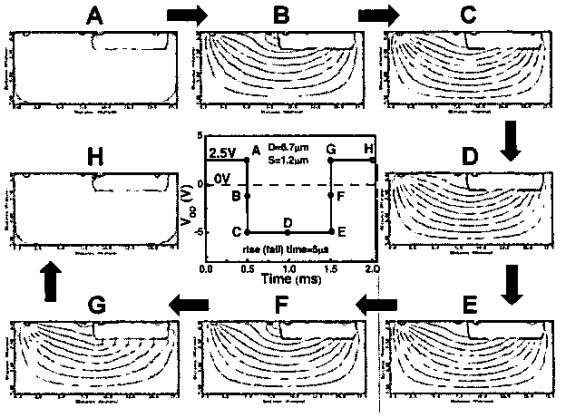


Fig. 11. The simulated 2-D current flow-lines with respect to various transient timing-points in quasi-static latchup test.

Conclusion

The underdamped sine-wave-like voltage stimulus has been clarified as the realistic TLU-triggering stimulus under system-level ESD test. With the aid of device simulation, the occurrence of TLU induced by the sweep-back current from the stored minority carriers has been well explained. Through comparisons between TLU and quasi-static latchup test, TLU reliability issue does still exist within a qualified IC product which had passed the quasi-static latchup test. The physical mechanism and simulation method on TLU, proposed in this work, can be used to investigate the design rules for latchup prevention in CMOS ICs.

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