

Low-Voltage-Triggered PNP Devices for ESD Protection Design in Mixed-Voltage I/O Interface with Over-VDD and Under-VSS Signal Levels

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Abstract

ESD protection design for mixed-voltage I/O interfaces with the low-voltage-triggered PNP (LVTNP) devices is proposed in this paper. The LVTNP, by inserting N⁺ or P⁺ diffusion across the junction between N-well and P-substrate of the PNP devices, is designed to protect the mixed-voltage I/O pads for signals with voltage levels higher than VDD (over-VDD) and lower than VSS (under-VSS). The experimental results in a 0.35- μ m CMOS process have proven that the ESD level of the proposed LVTNP is higher than that of the traditional PNP device.

1. Introduction

To improve circuit operating speed and performance, device dimensions of MOSFET had been shrunk in advanced CMOS technology. In order to follow constant-field scaling requirement and to reduce power consumption, the power supply voltages in CMOS ICs have been also scaled downwards. So, most computer architectures require the interfacing of semiconductor chips or sub-systems with different internal power supply voltages. With the mix of power supply voltages in electronic system, as shown in Fig. 1, the I/O interface circuit and electrostatic discharge (ESD) protection circuit must be designed to avoid electrical overstress across the gate oxide, to avoid hot-carrier degradation on the output devices, and to prevent undesirable leakage current paths between the chips [1], [2].

One of the mixed-voltage circuit applications, such as ADSL which has input signals with voltage levels higher than VDD and lower than VSS, is shown in Fig. 2. The traditional ESD protection circuits shown in Figs. 3(a) and 3(b) are not suitable for such mixed-voltage interfaces. In Fig. 3(a), under the normal condition, the Dp diode will be forward biased when the input signals are higher than VDD. The Dn diode will be forward biased when the input signals are lower than VSS. This ESD protection circuit will cause the current leakage between the chips. In Fig. 3(b), the parasitic drain-to-bulk junction diodes in the

ESD-protection PMOS (Mp) and NMOS (Mn) cause the same leakage issue as that in Fig. 3(a). Moreover, in Fig. 3(b), the ESD-protection PMOS (Mp) and NMOS (Mn) will result in gate-oxide reliability issue when the over-VDD or under-VSS external signals reach to input pad.

In this paper, a new ESD protection design with the low-voltage-triggered PNP (called as LVTNP) has been developed to protect the I/O interface with input voltage level higher than VDD or lower than VSS. The LVTNP with a low breakdown voltage, by avalanche breakdown across the P⁺/N⁺ well or N⁺/P⁺ sub junctions, provides effective discharging path to protect the internal circuits of such mixed-voltage I/O interfaces. Under normal circuit operation conditions, the LVTNP device is kept off without causing current leakage between the chips.

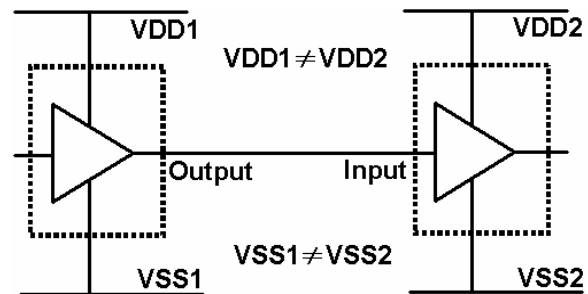


Fig. 1. The mixed-voltage I/O interfaces in electronic system.

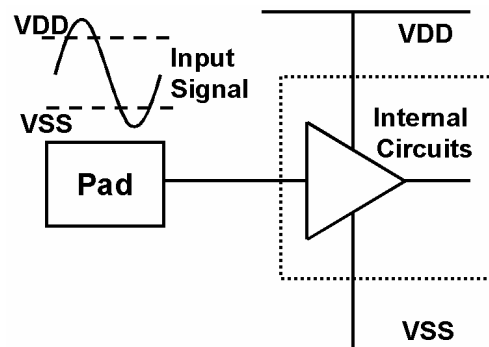


Fig. 2. The input signals with voltage levels higher than VDD and lower than VSS in some mixed-voltage I/O interfaces.

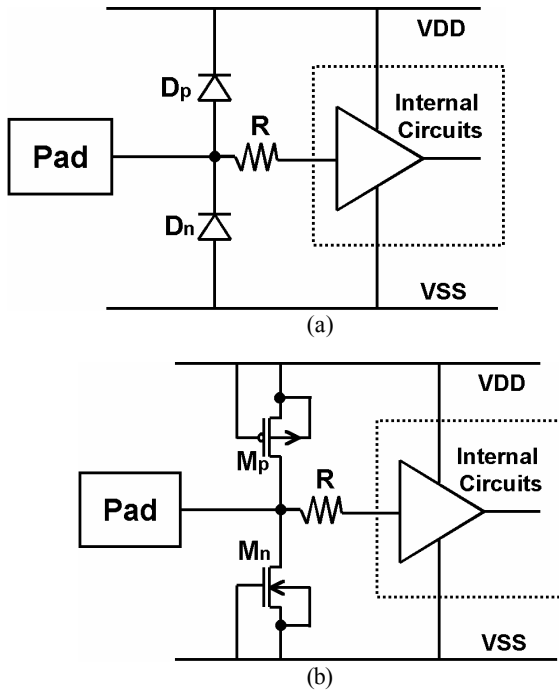


Fig. 3. Two traditional ESD protection designs with (a) double diodes, and (b) gated PMOS and NMOS, for the input pad.

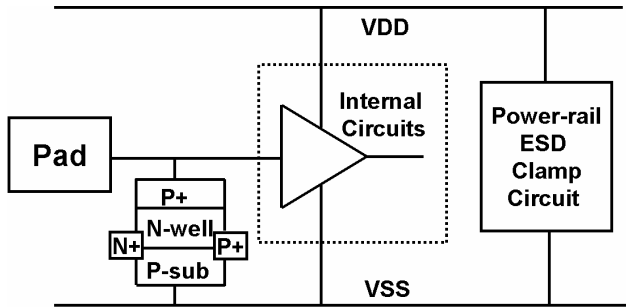


Fig. 4. The new ESD protection design with LVTNP device.

2. ESD Protection Design with LVTNP

Due to the limitation on placing ESD diode between the input pad and VDD/VSS power lines for the mixed-voltage I/O interface with over-VDD and under-VSS signal levels, a new ESD protection design with LVTNP device is shown in Fig. 4. The LVTNP device is connected between input pad and VSS power line, which provides ESD protection for such mixed-voltage I/O interface. With the help of power-rail ESD clamp circuit, the positive-to-VSS, negative-to-VSS, positive-to-VDD, and negative-to-VDD ESD stresses [3] on the input pin can be discharged through the LVTNP to VSS or VDD.

The cross-sectional view of the traditional PNP device in CMOS process is shown in Fig. 5(a). Five new LVTNP devices are proposed and realized in this work to find the optimized design for ESD protection.

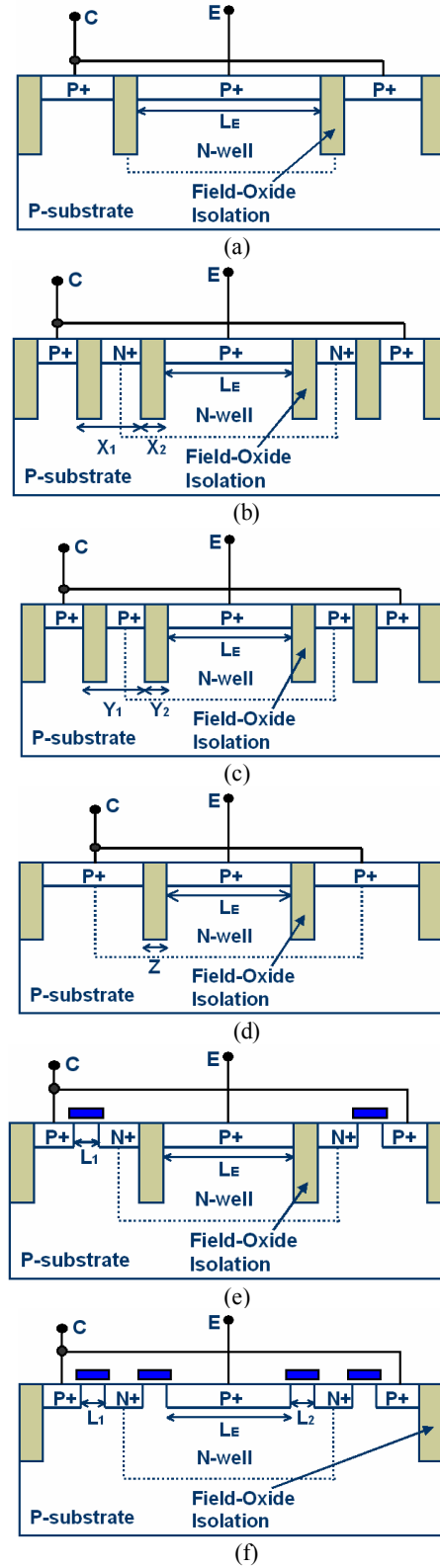


Fig. 5. The device structures of (a) the traditional PNP, (b) the type1 LVTNP, (c) the type2 LVTNP, (d) the type3 LVTNP, (e) the gated1 LVTNP, and (f) the gated2 LVTNP.

In the traditional PNP device, the junction between P+ diffusion and N-well has a low breakdown voltage since the P+ diffusion region is heavily doped. But, the junction between N-well and P-substrate has high breakdown voltage since both of them are lightly doped. The junction between N-well and P-substrate with high breakdown voltage is dis-advantageous for ESD current discharging. In Fig. 5(b), an N+ diffusion is inserted between the N-well and P-substrate. This structure is similar to the traditional PNP but with a low breakdown voltage and a floating N-well, which is called as the type1 LVTPNP. The inserted N+ diffusion is floated to avoid the leakage current paths from the pad to VSS for using in the mixed-voltage I/O interfaces. Thus, under the normal circuit operation condition, only one of the P/N or N/P junctions could be forward biased to eliminate leakage current. The inserted N+ diffusion with n-type heavily doped region to the P-substrate has a lower breakdown voltage, which avalanches earlier than the junction between N-well and P-substrate to discharge ESD current.

In Fig. 5(c), the P+ diffusion instead of N+ diffusion is inserted in the PNP structure to become the type2 LVTPNP. The junction between P+ diffusion and N-well has a low breakdown voltage since the regions adjacent to the N-well and P-substrate are heavily doped. Because of the floating base, the two separate P+ diffusions in Fig. 5(c) can be further merged into one P+ diffusion to form the type3 LVTPNP in Fig. 5(d). The heavily doped P+ diffusion adjacent to the N-well and P-substrate is also used as contact region for P-substrate.

In Fig. 5(e), compared with the type1 LVTPNP in Fig. 5(b), the field oxide region between N+ diffusion and P+ diffusion in P-substrate is replaced by a poly-gate to become the gated1 LVTPNP. In general CMOS process, the minimum design rule of the poly-gate is shorter than that of the field oxide. With the dummy gate, the clearance (marked as L_1) between the N+ and P+ diffusions can be realized with the minimum rule. Moreover, the replacement of field oxide with poly-gate can change the current path from the bottom of field oxide to the surface of the channel under the poly-gate. This will result in a smaller turn-on resistance to discharge ESD current fast. In Fig. 5(f), compared with the gated1 LVTPNP in Fig. 5(e), the field oxide between N+ diffusion and P+ diffusion in N-well is replaced with another poly-gate (marked with a gate length of L_2) to become the gated2 LVTPNP. The replacement of field oxide with poly-gate between the base and emitter will obtain a smaller turn-on resistance and a higher ESD robustness when the heat is located at this region.

3. Experimental Results

3.1. Device Characteristics

The LVTPNP devices with different device structures have been fabricated in a 0.35- μm CMOS process without

any extra mask layer. The measured IV curves of the traditional PNP and LVTPNP devices are shown in Fig. 6. Comparing the traditional PNP with the new proposed LVTPNP devices, the breakdown voltage is about 30V for the traditional PNP, but that of new LVTPNP is reduced to only 8~10V. The lower breakdown voltage of LVTPNP can provide better ESD protection function to the internal circuits.

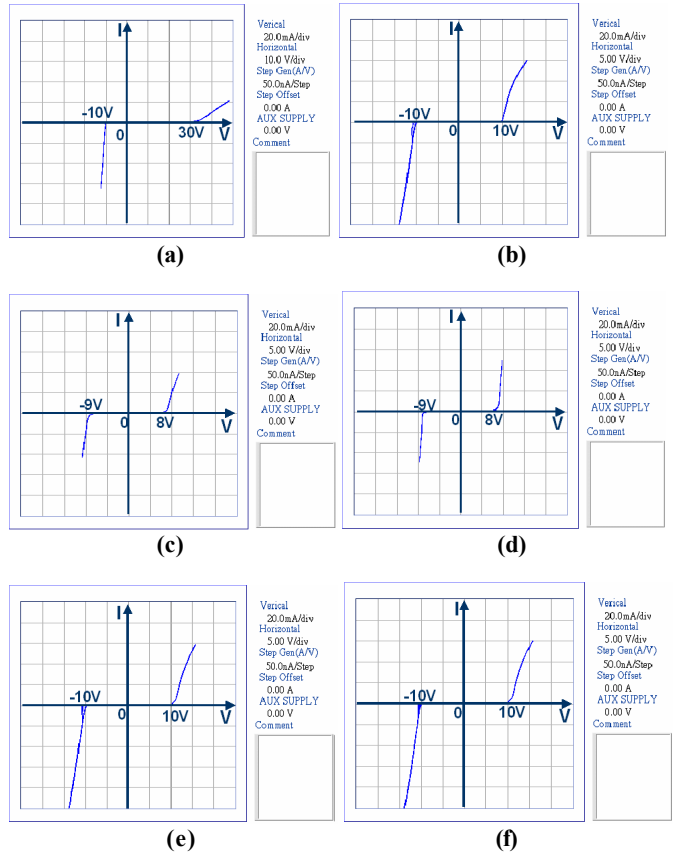


Fig. 6. The breakdown I-V curves of (a) the traditionalPNP, (b) the type1 LVTPNP, (c) the type2 LVTPNP, (d) the type3 LVTPNP, (e) the gated1 LVTPNP, and (f) the gated2 LVTPNP.

3.2. ESD Robustness

With the same device dimension of $30\mu\text{m} \times 30\mu\text{m}$ (the width is defined as $30\mu\text{m}$), the measured ESD levels of the traditional PNP and LVTPNP under the positive-to-VSS ESD-stress condition are compared in Fig. 7(a). The type1 LVTPNP with a lower breakdown voltage has higher ESD level ($\sim 250\text{V}$) than that of the traditional PNP ($\sim 150\text{V}$). Usually, the doping concentration of N-well is heavier than that of P-substrate, so the junction between P+ diffusion and N-well of the type2 LVTPNP has a slightly lower breakdown voltage ($\sim 8\text{V}$) than that of the junction between N+ diffusion and P-substrate in the type1 LVTPNP ($\sim 10\text{V}$). According to such results, the

type2 LVTPNP has higher ESD level (about 400V) than that of the type1 LVTPNP. For the type2 LVTPNP and the type3 LVTPNP, both of them have the same breakdown voltage. However, from the structure, the ESD current path of the type2 LVTPNP is longer than that of the type3 LVTPNP. From the I-V curves, the turn-on resistance of the type2 LVTPNP is larger than that of the type3 LVTPNP. The power dissipation is I^2R , so the type3 LVTPNP has larger ESD level (about 550V) than that of the type2 LVTPNP. Comparing the gated1 LVTPNP with the type1 LVTPNP, the replacement of field oxide by poly-gate can change the current path from the bottom of field oxide to the surface of the channel under the poly-gate. This change increases the area of the current path and makes it efficient to discharge ESD current. So, the gated1 LVTPNP has larger ESD level (about 400V) than that of the type1 LVTPNP under the positive-to-VSS ESD-stress condition. However, for the gated2 LVTPNP, it has the same ESD level as that of the gated1 LVTPNP.

Under the same device dimension of $30\mu\text{m} \times 30\mu\text{m}$ (the width is defined as $30\mu\text{m}$), the measured ESD levels of the traditional PNP and LVTPNP under the negative-to-VSS ESD-stress condition are compared in Fig. 7(b). In this ESD-stress condition, the breakdown occurs at the regions between P+ diffusion (the emitter) in the N-well and N-well. So, the breakdown voltages of these devices are about 9~10V. The traditional PNP, the type1 LVTPNP, the gated1 LVTPNP, and the gated2 LVTPNP have ESD levels about 1200~1250V. However, the type2 LVTPNP has ESD level about 700V, and the type3 LVTPNP has ESD level about 650V. The inserted P+ diffusion between N-well and P-substrate results in a lower ESD level under the negative-to-VSS ESD-stress condition.

3.3. Layout Spacings on ESD Levels

The ESD levels among the proposed LVTPNP devices with different layout spacings are compared in Figs. 8(a) ~ 8(g). The parameters include the width or spacing, L_E , X_1 , X_2 , Y_1 , Y_2 , Z , L_1 , and L_2 , which have been indicated in Fig. 5. For the gated2 LVTPNP device, L_1 and L_2 change simultaneously.

In Figs. 8(a) and 8(b), as the width of the devices increasing, the ESD levels are improved under both positive-to-VSS and negative-to-VSS ESD-stress conditions. The multi-fingers of LVTPNP can be used to increase the total current path from emitter to collector to improve ESD level to the desired ESD specification.

In Fig. 8(c), as the spacing X_1 of the type1 LVTPNP or the spacing Y_1 of the type2 LVTPNP increasing, the ESD level is improved under the positive-to-VSS ESD-stress condition, because the heat will be located at the base and collector junction. In Fig. 8(d), as the spacing X_2 of the type1 LVTPNP (the spacing Y_2 of the type2 LVTPNP, or the spacing Z of the type3 LVTPNP) increasing, the ESD level is improved under the negative-

to-VSS ESD-stress condition, because the heat will be located at the base and emitter junction. From such results, these spacings in LVTPNP devices can be optimized in layout to improve ESD robustness for such mixed-voltage I/O interfaces.

In Fig. 8(e), as the L_E of the devices increasing, the ESD level is improved under negative-to-VSS ESD-stress condition, because the heat will be located at the base and emitter junction. However, under positive-to-VSS ESD-stress, this parameter has no influence to ESD level.

In Fig. 8(f), as L_1 of the gated1 LVTPNP (the gated2 LVTPNP) increasing, the ESD level is improved under the positive-to-VSS ESD-stress condition. However, in such ESD-stress mode, the L_2 has no influence to ESD level. In Fig. 8(g), as L_2 of the gated2 LVTPNP increasing, the ESD level is improved under the negative-to-VSS ESD-stress condition. However, in such ESD-stress mode, the L_1 has no influence to ESD level. Such parameters L_1 (L_2) of the gated LVTPNP play the same role as the parameters X_1 (X_2) of the type1 LVTPNP, so as the parameters Y_1 (Y_2) of the type2 LVTPNP. By suitable adjusting the layout parameters, the desired ESD level can be achieved with the optimized layout style in those proposed LVTPNP devices.

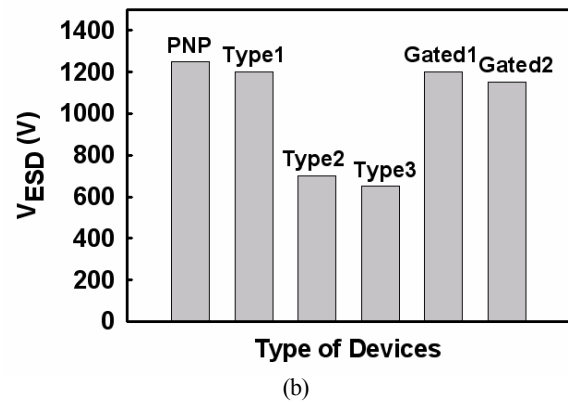
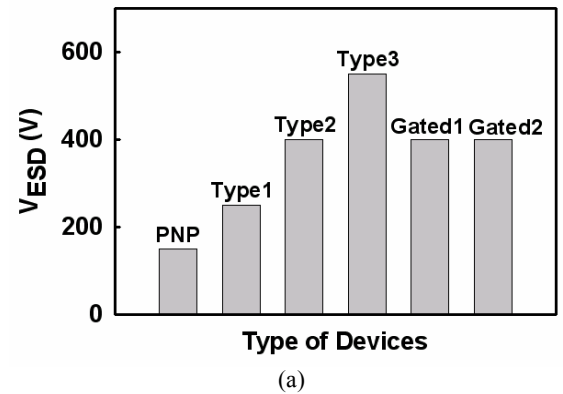
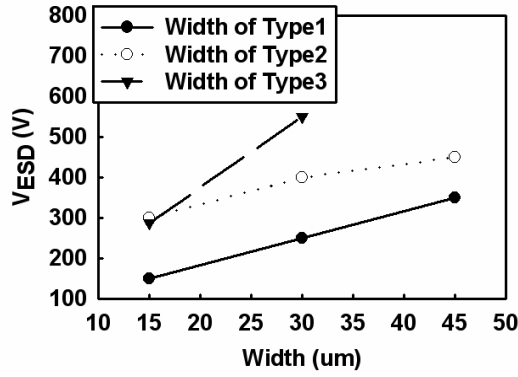
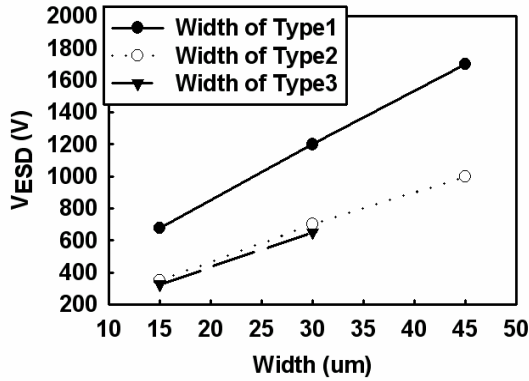


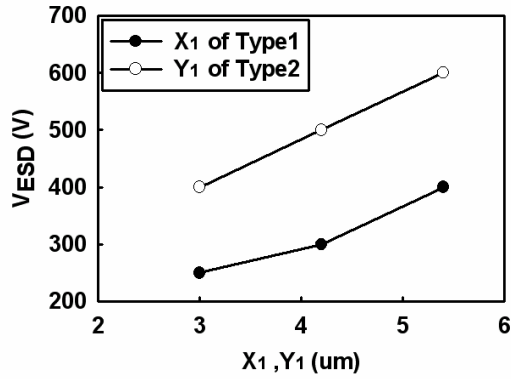
Fig. 7. ESD levels of the PNP devices with the same device dimension ($30\mu\text{m} \times 30\mu\text{m}$) under (a) the positive-to-VSS, and (b) the negative-to-VSS, ESD-stress conditions.



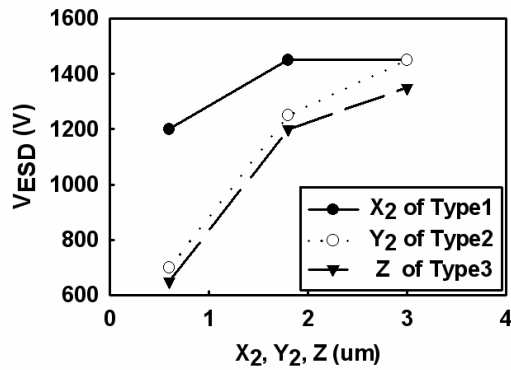
(a)



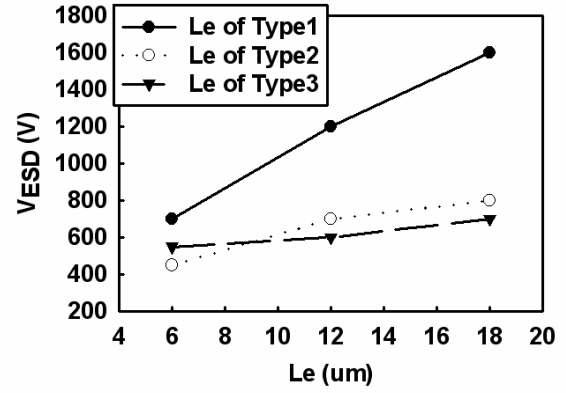
(b)



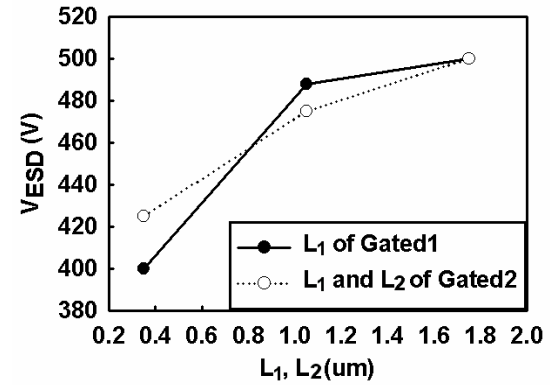
(c)



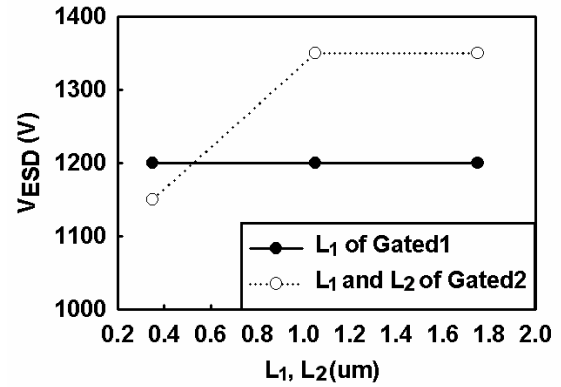
(d)



(e)



(f)



(g)

Fig. 8. (a) The ESD level v.s. device width under the positive-to-VSS ESD-stress condition. (b) The ESD level v.s. device width under the negative-to-VSS ESD-stress condition. (c) The ESD level v.s. the spacing X_1 of the type1 LVTPNP in or the spacing Y_1 of type2 LVTPNP under the positive-to-VSS ESD-stress condition, respectively. (d) The ESD level v.s. the spacing X_2 of the type1 LVTPNP, the spacing Y_2 of type2 LVTPNP, or the spacing Z of type3 LVTPNP under the negative-to-VSS ESD-stress condition, respectively. (e) The ESD level v.s. device L_E under the negative-to-VSS ESD-stress condition. (f) The ESD level v.s. L_1 or L_2 under the positive-to-VSS ESD-stress condition. (g) The ESD level v.s. L_1 or L_2 under the negative-to-VSS ESD-stress condition.

4. Application

One typical application of the proposed LVTPNP is used in the input ESD protection circuit for the ADSL interface, which has a high-voltage signal level of 5V and a low-voltage signal level of -1V. The circuit application for such ADSL input stage is shown in Fig. 9, where the singled-ended operational amplifier is the input stage of ADSL. Under the 0.25- μm CMOS process with VDD of 2.5V, the voltage divider is used to scale down the ADSL input signals when the input signals (between 5V and -1V) transmitted into ADSL IC. The V_{i2} is biased at the reference voltage of 1.25V, which is half of VDD. The voltage divider is formed by R and R_f , which are designed to bias V_{i1} at the scaled-down voltage level and to make the singled-ended operational amplifier well operation. The dc bias of signal level at the output node of operational amplifier is 1.25V (VDD/2). Under normal operating condition, the LVTPNP is turned off as mentioned before and has no influence to the ADSL input circuit. When ESD stress occurs to the input pin, the LVTPNP will breakdown with a lower trigger voltage to discharge ESD current.

Based on the layout parameters of LVTPNP devices, the ESD level mainly depends on the total current path from its emitter to its collector. Hence, the LVTPNP with multi-finger layout structure is used to increase the effective current path for further ESD improvement. Under the positive-to-VSS ESD-stress condition, ESD levels are independent to the emitter length (L_E) and collector length (L_C), hence these two parameters can be minimized in the multi-finger layout structure. The traditional layout structure and the new multi-finger layout structure to realize the LVTPNP devices are shown in Fig. 10(a) and Fig. 10(b), respectively. Under the 0.35- μm CMOS process, the HBM ESD levels of the LVTPNP devices with the traditional layout structure and new multi-finger layout structure are compared in the Table I. With suitable selection on the LVTPNP devices and the layout structure, the overall ESD robustness of ADSL input stage can be successfully designed to meet the ESD specification of 2-kV human-body-model (HBM) and 200-V machine-model (MM) ESD levels.

Table I

HBM ESD Levels of the LVTPNP devices with different layout structures.

Device Layout Structure	Type1 Traditional Structure	Type2 Traditional Structure	Type3 Traditional Structure	Type1 Multi-Finger Structure	Type2 Multi-Finger Structure	Type3 Multi-Finger Structure
Layout Area ($\mu\text{m} \times \mu\text{m}$)	36 \times 32	36 \times 32	36 \times 30.8	33.6 \times 36.5	33.6 \times 36.5	33.6 \times 36.5
HBM ESD Level (V)	250	350	550	950	1050	3.6k
HBM ESD Level ($\text{V}/\mu\text{m}^2$)	0.22	0.3	0.5	0.77	0.86	2.94

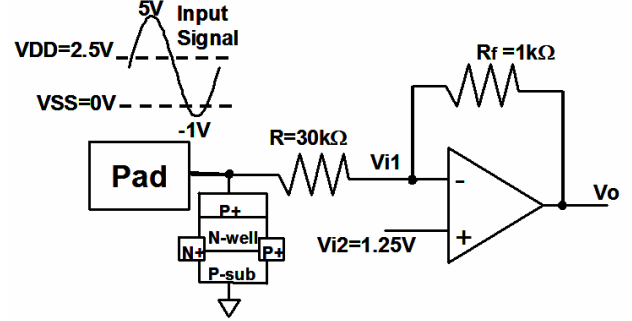


Fig. 9. The ADSL input stage with voltage divider formed by input R (30k Ω) and R_f (1k Ω) under 0.25- μm CMOS process.

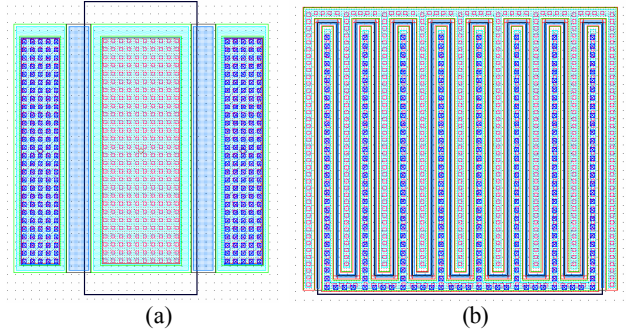


Fig. 10. The LVTPNP devices with different layout style of (a) the traditional structure, and (b) the new multi-finger structure.

5. Conclusion

ESD protection design for the mixed-voltage I/O interfaces with new proposed LVTPNP devices has been successfully designed to achieve a good ESD protection in 0.35- μm CMOS process. The LVTPNP devices indeed have the higher ESD level than that of the traditional PNP device. Comparing these LVTPNP devices, the type3 LVTPNP with the lowest trigger voltage and the highest ESD robustness will be the best choice as the ESD protection device for such mixed-voltage I/O interfaces. The multi-finger layout structure can be used to further increase the effective current discharging path among the LVTPNP device for improving ESD robustness.

References

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