Design to Avoid the Over-Gate-Driven Effect on ESD Protection Circuits in Deep-Submicron CMOS Processes

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Abstract

Although the gate-driven (or gate-coupled) technique was reported to improve ESD robustness of NMOS devices, the over-gate-driven effect has been found to degrade ESD level. This effect makes the gate-driven technique hard to be well optimized in deep-submicron CMOS ICs. In this work, a new design is proposed to overcome such over-gate-driven effect by circuit design and to achieve the maximum ESD capability of devices. The experimental results have shown significant improvement on the machine-model (MM) ESD robustness of ESD protection circuit by this new proposed design. This new design is portable (process-migration) for applications in different CMOS processes without modifying the process step or mask layer.

1. Introduction

To sustain reasonable electrostatic discharge (ESD) robustness in deep-submicron CMOS ICs, on-chip ESD protection circuits must be added into the chips [1]. The typical ESD levels required by general commercial IC products are 2kV in human-body-model (HBM) ESD test and 200V in machine-model (MM) ESD test [2]. To sustain the required ESD levels, ESD protection devices are often drawn with large device dimensions, which are often realized in multi-finger layout style to reduce the total occupied silicon area [3]. However, due to the non-uniform turn-on effect, ESD robustness of NMOS with multi-finger layout style was not linearly increased when the device dimension of NMOS is increased. To improve turn-on uniformity among the multi-fingers of ESD protection NMOS, the gate-driven (or gate-coupled) technique had been reported to increase ESD level of the large-device-dimension NMOS [4]-[6]. By using the gate-driven design, some ESD transient voltage is coupled to the gate of ESD protection NMOS during ESD transition to enhance turn-on uniformity among its multiple fingers. However, ESD robustness of the gate-driven NMOS had been found to be degraded dramatically when the coupled gate voltage was somewhat increased during ESD transition [6]-[8]. The over coupled ESD transient voltage on the gate of NMOS generates the strong inversion layer along the channel of NMOS to discharge ESD current [8]. With the limited area along the NMOS channel to discharge the huge ESD current (~ 1.33A for 2-kV HBM ESD), the NMOS is burned out more frequently. Such over-gate-driven effect becomes further worst, when the IC is fabricated by the advanced deep-submicron CMOS processes with the much thinner gate oxide and shallow junction depth.

In this paper, the over-gate-driven effect is introduced briefly, and then the new design method to overcome such a problem in the on-chip ESD protection circuits is proposed, which has been successfully verified in silicon chips.

2. Over-Date-Driven Effect

The measured snapback I-V curve of gate-grounded NMOS (GGNMOS) in a 0.35-μm CMOS process by transmission-line-pulse (TLP) system is shown in Fig. 1. The TLP system has been widely used to investigate device snapback characteristics during ESD overstress. Under ESD stress, the drain-substrate junction of NMOS begins to avalanche due to the high ESD voltage across it and electron-hole pairs are generated. The electrons are swept across the drain junction while the holes drift toward the source junction of the NMOS, generating a base current to the parasitic n-p-n bipolar. Once the potential of source-substrate junction of NMOS is forward biased, the parasitic n-p-n bipolar junction transistor (BJT) in the NMOS device structure is triggered on. The parasitic n-p-n BJT in the NMOS device can carry amperes of current under ESD stress condition.

However, due to the different distances from the base region to the substrate guarding which is often directly connected to ground through wide metal line, the base voltage of parasitic n-p-n BJT in the central region of multi-finger NMOS layout is higher than that in the sided regions of multi-finger NMOS layout. The parasitic n-p-n BJT in the central region is often triggered on before other fingers in the multi-finger NMOS device.

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Therefore, the overstress ESD voltage is clamped to the holding voltage of NMOS by the center fingers of multi-finger NMOS device. If the secondary breakdown voltage (Vt2) is smaller than the trigger voltage (Vt1) of the parasitic BJT in NMOS device, the parasitic n-p-n BJT in the central region prevents other fingers from being turned on. Therefore, all ESD current is discharged only through the parasitic n-p-n BJT in the central region of NMOS to cause non-uniform turn-on phenomenon. Consequently, ESD robustness of the ESD protection device can not be linearly increased by increase of the device dimension.

Non-uniform turn-on phenomenon can be alleviated by increasing the ballast resistance to increase Vt2, or by gate-driven technique to lower Vt1 [4]-[6]. The traditional gate-coupled technique with simple RC circuit is shown in Fig. 2, which is used to ensure that all fingers of NMOS can be turned on during ESD stresses. Since the ESD transient is a high voltage event in a very short period, some ESD-transient voltage is coupled to the gate of the gate-coupled NMOS (GCNMOS) through the capacitor (C), shown in Fig.2. As long as the gate voltage (Vg) is greater than the threshold voltage (Vt) of the GCNMOS, channel current of the GCNMOS is induced and help to forward bias the potential across source-substrate junction of the GCNMOS. Therefore, Vt1 of the GCNMOS can be lowered.

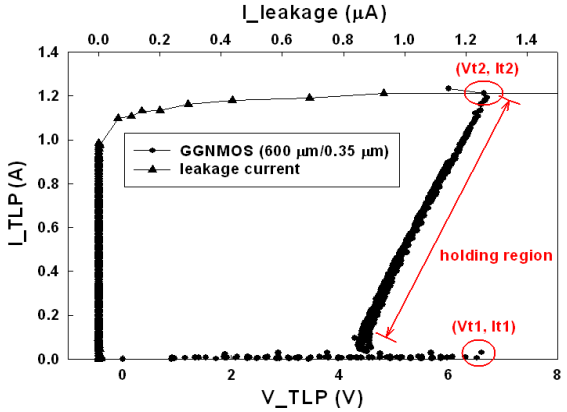


Fig. 1. The typical TLP-measured I-V curve of GGNMOS fabricated in a 0.35-μm CMOS process.

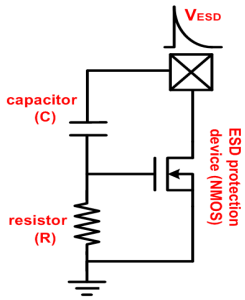


Fig. 2. The traditional RC gate-coupled technique to solve the non-uniform turn-on phenomenon in the ESD protection NMOS.

If Vt1 is lowered to be smaller than Vt2, the parasitic n-p-n BJT in the sided region of NMOS layout can be further turned on to share the huge ESD current. Thus, the ESD protection NMOS can be more robust by the gate-coupled technique. However, the over large gate voltage on GCNMOS causes excessive channel current, which makes the channel of GCNMOS being burned out easily by huge ESD current [8]. This causes the over-gate-driven effect, which decreases ESD robustness of GCNMOS dramatically.

3. New ESD Protection Design

Since over-coupled transient voltage on the gate of GCNMOS will result in the over-gate-driven effect, it can be successfully overcome by adding a clamping string to limit the gate voltage of GCNMOS during ESD transient, as shown in Fig. 3. In this work, the diodes or NMOS devices connected in series are used to realize the clamping string. With the clamping string, the gate voltage (Vg) of GCNMOS at the node a in Fig. 3 can be limited to Vt × n, where n is the number of clamping devices. In order to observe the operation of the clamping string during ESD transient, a small NMOS Mn2 with its gate connected to the gate of GCNMOS is added in the test chip, as shown in Fig. 4. A 1-kΩ resistor is connected to the drain of Mn2 (node b) to monitor the current through Mn2.

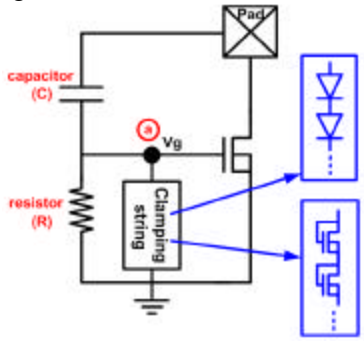


Fig. 3. A new proposed gate-coupled ESD protection circuit with the clamping string to overcome the over-gate-driven effect.

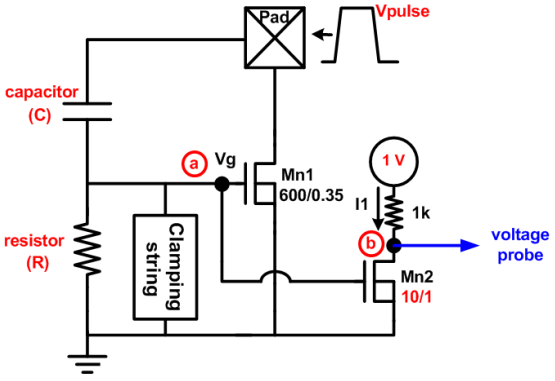


Fig. 4. Circuit to observe the operation of the clamping string.

Initially, a 1-V DC bias is applied to the drain of Mn2 through the 1-kΩ resistor. Then, the voltage pulses (Vpulse) with different pulse heights are applied to the pad. If Vg (node a) is coupled higher than the threshold voltage of Mn1 (also Mn2) by the applied voltage pulse, Mn2 will be turned on to drop the potential on node b from the initial 1V to a certain value by the current I1.

Base on this observing method, Fig. 5 shows some measured results of a RC gate-coupled circuit without the clamping string. The circuit structure is the same as that shown in Fig. 4 but the clamping string has been removed in the test chip. A 3-pF capacitor is designed to make the occurrence of over-gate-driven effect easily under ESD stresses, and a NMOS (W/L= 30μm/1.5μm) with its gate connected to VDD is used to realize the resistor R.

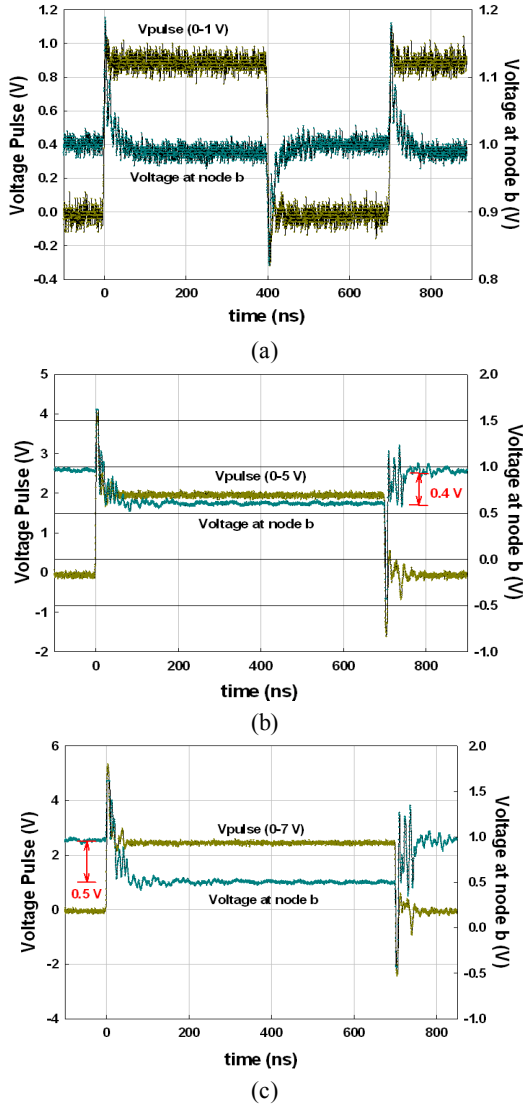


Fig. 5. The observed voltage on the node b of a RC gate-coupled circuit without the clamping string under the Vpulse of (a) 1 V, (b) 5 V, and (c) 10 V.

In Fig. 5(a), a 0-to-1V voltage pulse is applied to the pad. The voltage observed at the node b is almost unchanged, because the coupled Vg is less than the threshold voltage of Mn2. When a larger (0-to-5V) voltage pulse is applied to the pad, the voltage observed at the node b drops from 1V to 0.6V, as shown in Fig. 5(b). This result proves that the Vg is coupled higher than the threshold voltage of Mn2. Therefore, Mn2 is turned on and the voltage at node b drops to the voltage level of 1V – (I1×1kΩ). In Fig. 5(c), a 0-to-10V voltage pulse is applied to the pad. A 0.5-V voltage drop at the node b is observed. With the larger applied voltage pulse (Vpulse), the coupled gate voltage (at node a) is higher, which causes a larger voltage drop observed at the node b.

When different magnitudes of voltage pulses are applied, the voltage drop at the node b can be kept as constant only if the Vg is clamped at a certain fixed value by the clamping string in Fig. 3. Therefore, by monitoring the voltage waveform at the node b, the effectiveness of the clamping string to limit the coupled gate voltage (at node a) can be verified.

4. Experimental Results

The TLP-measured I-V curves of a GCNMOS (W/L= 600μm/0.35μm) with or without the clamping string are compared in Fig. 6. Due to the non-uniform turn-on phenomenon, the It2 value of GGNMOS which has shown in Fig.1 with the same device dimension is lower than that of GCNMOS with or without the clamping string. With RC gate-coupled technique, the It2 value of the GCNMOS (W/L= 600μm/0.35μm) can be increased greater than 6A. The over-gate-driven effect probably does not affect the It2 level of GCNMOS in these TLP measured I-V curves. However, since MM ESD stress has a faster rise time than that of HBM ESD stress, the over-gate-driven effect on the GCNMOS can be more easily observed under MM ESD stress.

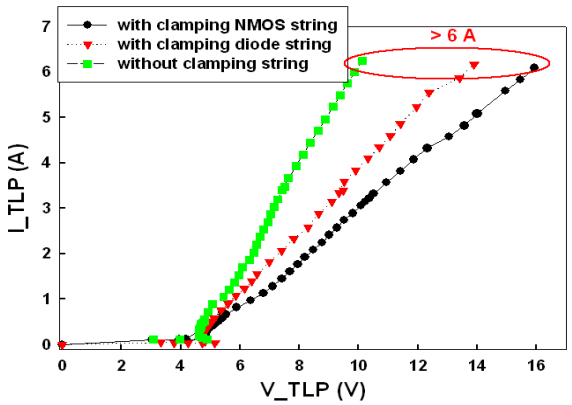


Fig. 6. TLP-measured I-V curves of GCNMOS with or without clamping string.

In order to investigate the voltage level which causes the over-gate-driven effect to NMOS, the MM ESD levels of NMOS (W/L= 600µm/0.35µm) under different gate biases are measured and shown in Fig. 7. After 175-V MM ESD stress on the NMOS under 2-V gate bias, the total leakage current Id of NMOS (biased at drain voltage of Vd=3.3V and source grounded) comes mainly from the gate current Ig, instead of source current Is, as those shown in Fig. 8. It indicates that the ESD failure location of this NMOS, which is subjected to 175-V MM ESD stress under 2-V gate bias, is located at the gate instead of source/drain junction. Therefore, the voltage level to cause over-gate-driven effect on NMOS fabricated in the 0.35-µm CMOS process is less than 2 V. Comparing the MM ESD level of GCNMOS with that of NMOS with gate bias, the later has lower MM ESD level. This may result from that channel of the gate-biased NMOS has already been induced before ESD transient, while channel of GCNMOS is induced during ESD transient. This phenomenon can be investigated in the future.

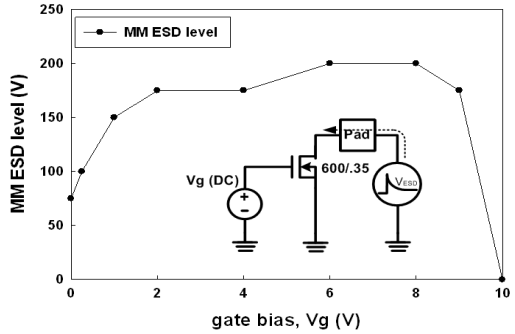


Fig. 7. MM ESD level of NMOS device (W/L= 600µm/0.35µm) under different gate biases.

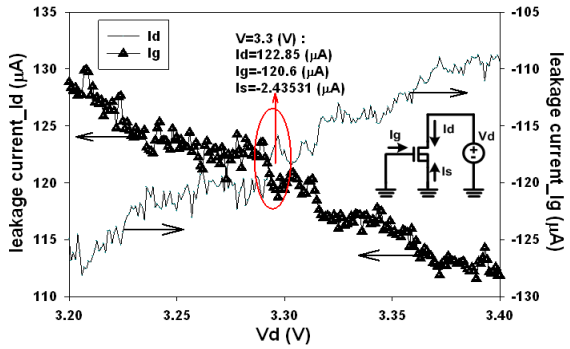


Fig. 8. Leakage current in the NMOS after 175-V MM ESD stress under 2-V gate bias.

4.1 With clamping diode string

To observe the operation of GCNMOS with the clamping diode string, the voltage pulses (Vpulse) with different pulse heights are applied to the pad, as shown in Fig. 9(a). If the gate voltage Vg of Mn1 (at node a) is limited by the clamping diode string, the current I1 and the voltage drop at the node b will not increase when the magnitude of Vpulse is increasing. Therefore, the gate voltage of Mn1 can be monitored by measuring the voltage drop at the node b during the transition of voltage pulses with different magnitudes. As comparing the measured voltage waveforms shown in Figs. 10(a) and 10(b), the voltage drops at the node b are the same with regard to the 0-to-5V and 0-to-7V voltage pulses. Therefore, Vg of Mn1 is limited to a constant voltage level by the clamping diode string.

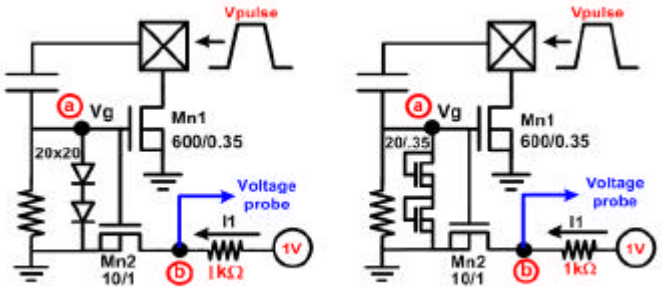


Fig. 9. The experimental setup to monitor the RC gate-coupled ESD protection circuit with (a) the clamping diode string, and (b) the clamping NMOS string, to limit the gate voltage.

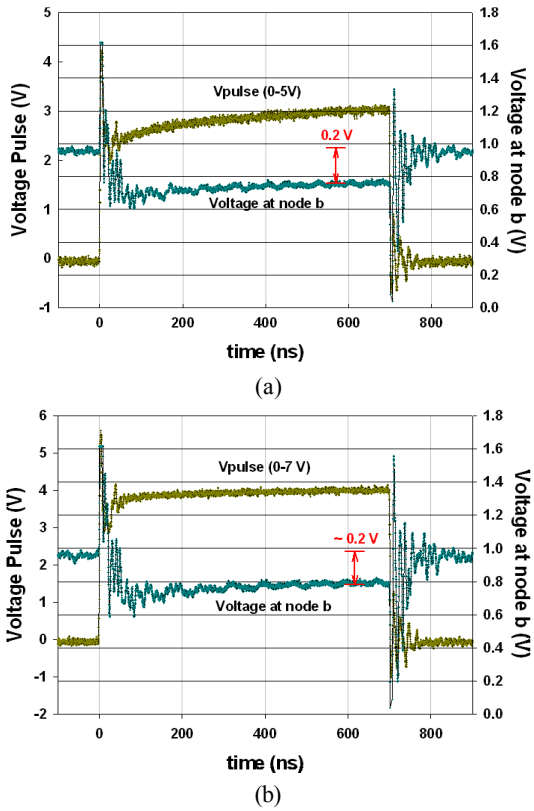


Fig. 10. The measured voltage on the node b of the RC gate-coupled ESD protection circuit with clamping diode string under (a) 0-to-5V, and (b) 0-to-7V, voltage pulses.

The MM ESD robustness per layout area of GCNMOS with clamping diode string is shown in Fig. 11, where the clamping strings are realized with diodes of different sizes or different numbers. With the two stacked diodes in the clamping diode string, MM ESD level of the GCNMOS can be improved from 0.83V/μm^2 to 1.12V/μm^2. The MM ESD level of GCNMOS with clamping diode string starts to degrade, when three diodes connected in series in the clamping string with each diode dimension of 20 × 20 μm^2. However, MM ESD level of GCNMOS with larger number of diodes in the clamping string does not seriously degrade, when the diodes are drawn with larger diode dimensions. To understand the effect of different diode dimensions in the clamping diode string, a 0-to-10V voltage pulse is applied to two RC gate-coupled circuits which have different clamping diode strings. One has two clamping diodes connected in series with each diode dimension of 20 × 20 μm^2, and the other has two clamping diodes connected in series with each device dimension of 30 × 30 μm^2.

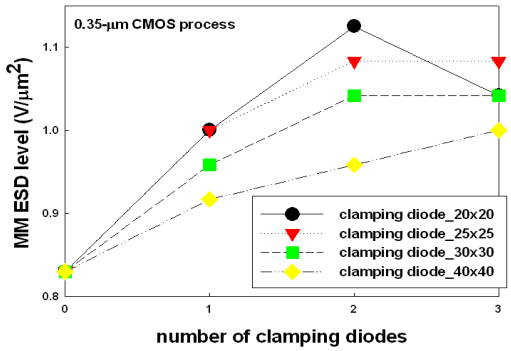


Fig. 11. MM ESD level of GCNMOS with the clamping diode strings of different diode numbers or diode dimensions.

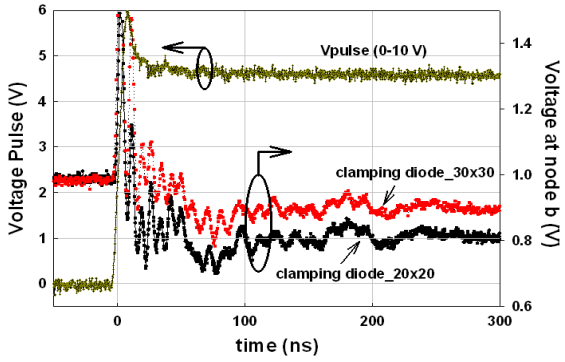
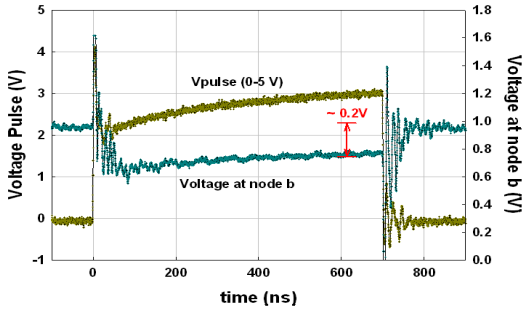


Fig. 12. A 0-to-10V voltage pulse is applied to two RC gate-coupled ESD protection circuits with different clamping diode strings.

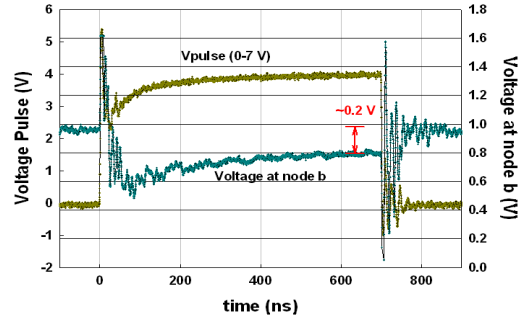
As shown in Fig. 12, the clamping diode string with larger diode dimension results in a smaller voltage drop at the node b. Due to the turn-on resistance of the clamping string, the gate voltage of GCNMOS, Vg in Fig. 9(a), is higher than Vt×n, where n is the number of clamping diodes. The smaller diode dimension in the clamping string results in a higher turn-on resistance of the clamping string to sustain a larger Vg during ESD transient. Thus, in Fig. 11, when the GCNMOS has the clamping diode string with three diodes connected in series, the smallest diode dimension in the clamping string can not successfully prevent the over-gate-driven effect during ESD stress. However, the clamping string with larger diode dimensions can still safely protect the GCNMOS from over-gate-driven effect. When design the clamping string to overcome the over-gate-driven effect, both the number of clamping diodes and the turn-on resistance (which is relative to the dimension of the clamping diodes) should be taken into consideration.

4.2 With clamping NMOS string

NMOS devices connected in series are also treated as the clamping string in this work. Similarly, to observe the operation of clamping NMOS string, the voltage pulses with different magnitudes are applied to the pad, as shown in Fig. 9(b). The transient voltage waveforms at the node b are measured in Figs. 13(a) and 13(b), respectively, under the voltage pulses of 0-to-5V and 0-to-7V. As seen in Figs. 13(a) and 13(b), the voltage drops at node b are almost the same. So, the clamping NMOS string can successfully limit the gate voltage of NMOS Mn1 during ESD transient.



(a)



(b)

Fig. 13. The measured voltage on the node b of the RC gate-coupled ESD protection circuit with clamping NMOS string under (a) 0-to-5V, and (b) 0-to-7V, voltage pulses.

The MM ESD per layout area of the GCNMOS with the different clamping NMOS strings can be improved from 0.83V/μm^2 to 1.08V/μm^2, as shown in Fig. 14. By well controlling the gate voltage, 30% increase of the MM ESD level of GCNMOS can be achieved. As shown in Fig. 14, when five NMOS devices connected in series are used in the clamping NMOS string, only the ESD level of GCNMOS with the largest NMOS dimension in the clamping NMOS string does not degrade. The effect of different NMOS dimensions in the clamping NMOS strings is the same as that in the clamping diode string.

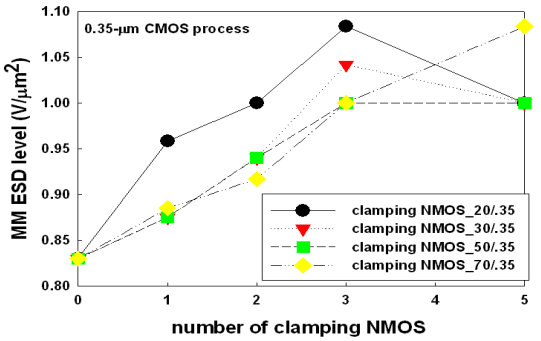


Fig. 14. MM ESD level of the GCNMOS with clamping NMOS string.

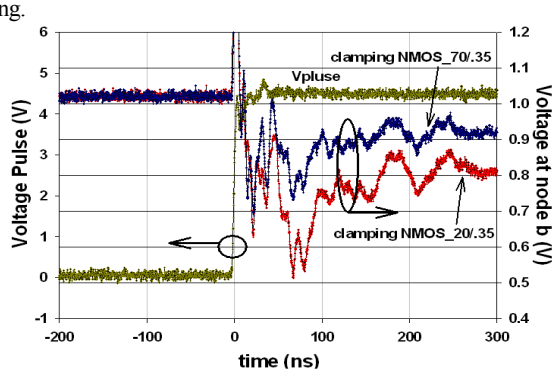


Fig.15. A 0-to-10V voltage pulse is applied to two RC gate-coupled ESD protection circuits with different clamping NMOS strings.

A 0-to-10V voltage pulse is applied to two RC gate-coupled ESD protection circuits with different NMOS dimensions in the clamping NMOS strings. One has two clamping NMOS devices connected in series with each NMOS dimension (W/L) of 20μm/0.35μm, and the other has two clamping NMOS devices connected in series with each NMOS dimension of 70μm/0.35μm. The measured voltage waveforms at the node b of these two RC gate-coupled ESD protection circuits with clamping NMOS strings are shown in Fig. 15. The clamping NMOS string with a larger NMOS dimension causes a smaller voltage drop at the node b. This results from the different turn-on resistance of clamping NMOS strings with different device dimensions. Therefore, the design to overcome the over-gate-driven effect on gate-coupled ESD protection NMOS can be optimized by selecting the numbers of NMOS and the dimensions of NMOS in the clamping NMOS string. Such a result provides a high flexibility to realize this method in different CMOS processes without modifying the process step or mask layer.

5. Conclusion

The new proposed ESD design method with the clamping string can successfully prevent over-gate-driven effect to continually improve ESD level of ESD protection circuits with the gate-coupled or gate-driven technique in the sub-quarter-micron CMOS processes. From experimental results in a 0.35-μm CMOS process, the increase of 35% and 30% on the MM ESD level of GCNMOS with clamping diode string and clamping NMOS string have been achieved, respectively. The new proposed method provides a high flexibility to realize the clamping string in different CMOS processes without modifying the process step or mask layer.

6. References

[1] A. Amerasekera and C. Duvvury, *ESD in Silicon Integrated Circuits, 2nd Edition*, New York: Wiley, 2002.

[2] *ESD Test Standard*, ESD Association, ESD STM5.1, 1998.

[3] C. Jiang, E. Nowak, and M. Manley, "Process and design for ESD robustness in deep submicron CMOS technology," in *Proc. IEEE Int. Reliability Physics Symp.*, 1996, pp. 233–236.

[4] C. Duvvury, C. Diaz, and T. Haddock, "Achieving uniform NMOS device power distribution for submicron ESD reliability," in *Tech. Dig. IEDM,* 1992, pp. 131–134.

[5] M.-D. Ker, C.-Y. Wu, T. Cheng, and H.-H. Chang, "Capacitor-couple ESD protection circuit for deep-submicron low-voltage CMOS ASIC," *IEEE Trans. VLSI Syst.*, vol. 4, pp. 307–321, Mar. 1996.

[6] J. Chen, A. Amerasekera, and C. Duvvury, "Design methodology and optimization of gate-driven NMOS ESD protection circuits in submicron CMOS processes," *IEEE Trans. Electron Devices*, vol. 45, pp. 2448–2456, Dec. 1998.

[7] T.-Y. Chen and M.-D. Ker, "Analysis on the dependence of layout parameters on ESD robustness of CMOS devices for manufacturing in deep-submicron CMOS process," *IEEE Trans. Semiconductor Manufacturing,* vol. 16, pp. 486-500, Aug. 2003.

[8] T.-Y. Chen and M.-D. Ker, "Investigation of the gate-driven effect and substrate-triggered effect on ESD robustness of CMOS devices," *IEEE Trans. Device and Materials Reliability*, vol. 1, pp. 190-203, Dec. 2001.