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NEW DESIGN CONCEPT FOR ON-CHIP ESD PROTECTION CIRCUITS WITH ALREADY-ON DEVICE IN NANOSCALE CMOS TECHNOLOGY

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ABSTRACT

A new design concept for on-chip electrostatic discharge (ESD) protection circuits with the already-on device is proposed to provide efficient ESD protection for ICs in nanoscale CMOS technologies. The already-on device used in this work is the native-NMOS-triggered SCR (NANSCR) device, which has a trigger voltage of almost zero in a 130-nm CMOS process. The already-on NANSCR has the lowest trigger voltage, smaller turn-on resistance, lower holding voltage, faster turn-on speed, and higher ESD level than those of traditional design.

1. INTRODUCTION

For CMOS IC applications with a maximum voltage level of VDD below 1.2 V, SCR can be a great candidate for on-chip ESD protection due to its highest ESD robustness, smallest layout area, and free to latchup issue, as compared with non-SCR ESD protection devices. But, the SCR still has a higher trigger voltage of ~18 V in a 130-nm CMOS process, which is generally greater than the gate-oxide breakdown voltage of the input stages. Furthermore, the gate oxide thickness has been scaled down to only ~25 Å, and its time-to- breakdown (t_{BD}) or charge-to-breakdown (Q_{BD}) will also be decreased in the same CMOS process. So, it is imperative to reduce the trigger voltage and turn-on time of SCR for efficiently protecting the ultra-thin gate oxide from latent damage or rupture [1], especially against the fast charged-device-model (CDM) ESD events. Some reports had presented the solutions to reduce the trigger voltage of SCR device [2]-[5] for protecting the thin gate oxide.

In this paper, a new design concept for on-chip ESD protection circuits with the already-on device is proposed to provide efficient ESD protection for ICs in the nanoscale CMOS technologies. A new whole-chip ESD protection scheme realized by the already-on NANSCR has been designed with the consideration against the pin-to-pin ESD stresses.

2. THE ALREADY-ON DEVICE

The native NMOS is directly built in a lightly-doped p-type substrate, whereas the normal NMOS (PMOS) is in a heavily-doped p-well (n-well) in a P-substrate twin-well CMOS technology, as shown in Fig. 1. The native NMOS is fully process-compatible with the standard CMOS process without adding extra mask. The threshold voltage of native NMOS is almost zero (~0.1V), however, that of normal NMOS is about 0.34 V in a 130-nm CMOS process. The native NMOS and lateral SCR are merged together as the native-NMOS-triggered SCR (NANSCR).

The lumped equivalent circuits of NANSCR and the traditional low-voltage-triggered SCR (LVTSCR) [2] are shown in Figs. 2(a) and 2(b), respectively. The drain of native NMOS in NANSCR is directly coupled to the pad of anode, but the drain of NMOS in LVTSCR is located across the n-well/P-substrate junction of the SCR device. The gate of native NMOS is connected to a negative bias circuit (NBC) [6] to turn off the NANSCR, but the gate of NMOS in LVTSCR is connected to VSS to ensure that LVTSCR is off, under normal circuit operating condition.

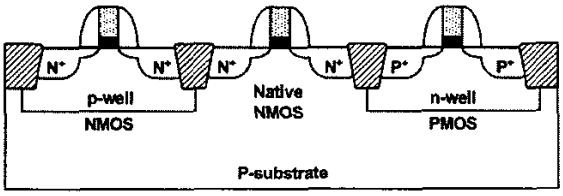

Fig. 1 The device cross-sectional views of the NMOS, PMOS, and native NMOS in a P-substrate twin-well CMOS technology.

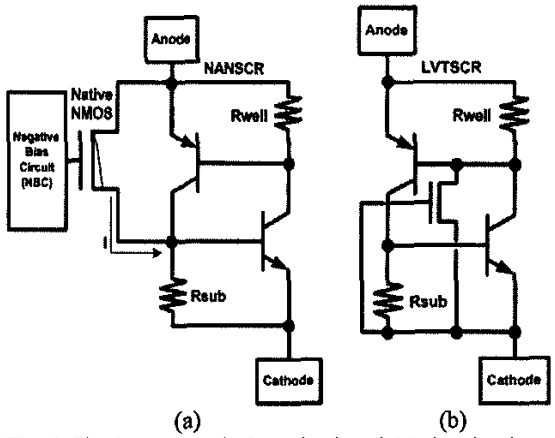

Fig. 2 The lumped equivalent circuits of (a) the already-on native-NMOS-triggered SCR (NANSCR) device and (b) the traditional LVTSCR device.

The new proposed already-on NANSCR and the traditional LVTSCR have been fabricated in a 130-nm salicided CMOS process. The active area (without including the guard rings) of SCR in NANSCR is drawn

as 20μm×8μm. The active area of LVTSCR is drawn as 20μm×7.5μm, and the W/L of NMOS within LVTSCR is 20μm/0.13μm. The comparison of DC I-V curves between NANSCR and LVTSCR is shown in Fig. 3. The native NMOS in NANSCR structure has two different device dimensions of 20μm/0.3μm and 40μm/0.3μm for comparison. With the substrate-triggered technique [4], the trigger voltage of NANSCR with native NMOS of 20-μm channel width is about ~4 V, which is smaller than that (~5 V) of LVTSCR. So, the NANSCR can be triggered on faster than the LVTSCR. Moreover, if the channel width of native NMOS in NANSCR is increased to 40μm, the trigger voltage of NANSCR with native NMOS of 40-μm channel width can be further reduced to only ~2.5 V. The holding voltage of NANSCR is about ~1.6 V, which is immune from latchup issue in CMOS ICs with 1.2-V voltage supply. Such a holding voltage of NANSCR is still low enough to provide higher ESD robustness, as compared with other ESD protection devices.

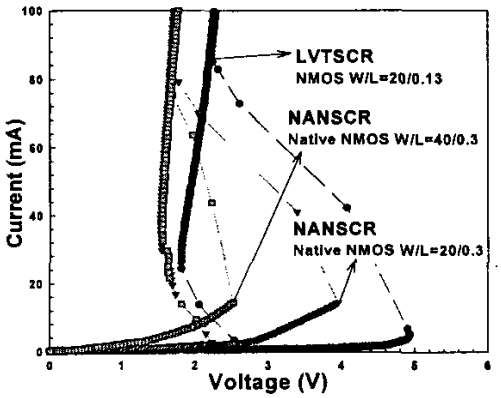

Fig. 3 The DC I-V curves of the NANSCR and LVTSCR.

3. ON-CHIP ESD PROTECTION CIRCUITS

3.1. ESD Protection Circuit for I/O Pads

The ESD protection circuit for input or output pads, which is realized with NANSCR devices, is shown in Fig. 4. The n-well in NANSCR_1 is connected to VDD, but not connected to I/O pad. The gates of native NMOS in the NANSCR_1 and NANSCR_2 are connected to the same negative bias circuit (NBC). Under normal circuit operating conditions, the gates of native NMOS in all NANSCR devices are biased by the same NBC to turn off the NANSCR devices. So, the NANSCR_1 and NANSCR_2 will not interfere with the functions of I/O circuits, whenever the input/output signals are logic high (VDD) or logic low (VSS). Because the holding voltage of NANSCR (~1.6 V) is greater than the maximum voltage level (1.2 V) of input/output signals, the transient-induced latchup issue in such NANSCR devices is vanished.

Under the positive-to-VSS (PS) ESD-zapping condition (with grounded VSS but floating VDD), the gate of native NMOS in the NANSCR_1 is floating. The NANSCR_1 is triggered on quickly by the triggering current generated from the already-on native NMOS. So, the positive ESD current can be effectively discharged from the I/O pad through the NANSCR_1 to grounded VSS line. Under the negative-to-VDD (ND) ESD-zapping condition (with grounded VDD but floating VSS), the gate of native NMOS in the NANSCR_2 is floating but with an initial voltage level of 0 V. The negative ESD voltage at the I/O pad will pull down the source voltage of native NMOS through the base-emitter junction of NPN in the NANSCR_2 device. Therefore, the native NMOS in NANSCR_2 will be turned on first, resulting in the NANSCR_2 being triggered on. The negative ESD current will be discharged from the I/O pad through the NANSCR_2 to grounded VDD line.

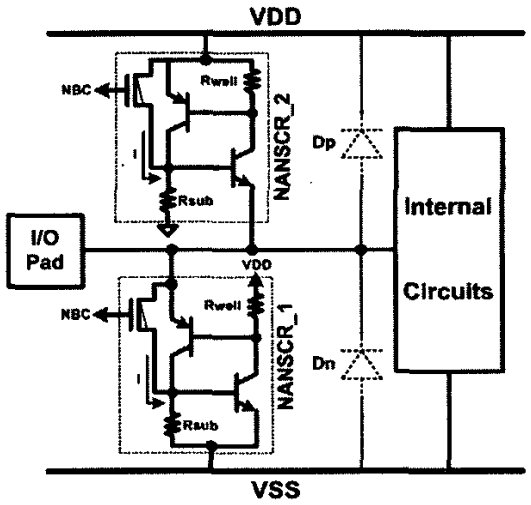

Fig. 4 Design of ESD protection circuit for the input or output pads with the already-on NANSCR devices.

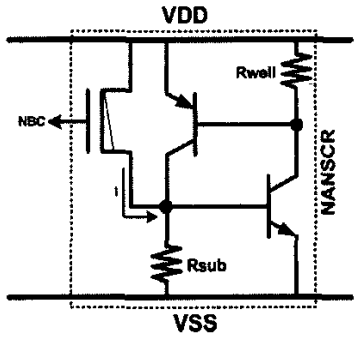

Fig. 5 The VDD-to-VSS ESD clamp circuit realized with the already-on NANSCR device.

3.2. Power-Rail ESD Clamp Circuit

The VDD-to-VSS ESD clamp circuit realized with the NANSCR device is shown in Fig. 5. Under normal circuit operating conditions, the NBC is active to turn off the NANSCR device. When a positive ESD pulse is applied on the VDD line with grounded VSS line, the NANSCR device will be quickly triggered on by the already-on native NMOS to discharge the positive ESD current to grounded VSS line. If a negative ESD pulse is applied on the VDD line with grounded VSS line, the

parasitic diode (P-substrate/n-well junction) in the NANSCR structure will be forward biased to discharge the negative ESD current.

3.3. Whole-Chip ESD Protection Scheme

A new whole-chip ESD protection scheme with the proposed NANSCR devices is shown in Fig. 6. The anode terminals of NANSCR devices are all connected to the pads (including I/O, VDD, and VSS pads) and their cathode terminals are all connected to the ESD path. The ESD path indicated by the bold line in Fig. 6 can be realized with the wide and top metal line in the chip to efficiently discharge the ESD current of several amperes during ESD events. The gates of native NMOS in the NANSCR devices are biased by an on-chip NBC to fully turn off all NANSCR devices under normal circuit operating conditions.

During ESD-zapping condition, the already-on NANSCR devices without negative bias in the whole-chip ESD protection scheme can be triggered on more quickly to effectively protect the internal circuits. Except the four modes of ESD stresses on the I/O pads with VDD or VSS grounded, all pin-to-pin ESD-zapping conditions (such as input-to-input, output-to-output, input-to-output, or VDD-to-VSS, or VSS-to-VDD can be fully protected by this whole-chip ESD protection scheme. By using this new whole-chip ESD protection scheme, the pin-to-pin ESD stress can be discharged through only a NANSCR, the ESD path, and a parasitic diode between the zapping pin and the grounded pin.

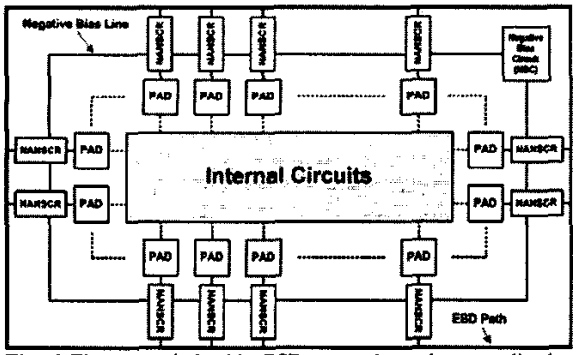

Fig. 6 The new whole-chip ESD protection scheme realized with the already-on NANSCR devices.

4. EXPERIMENTAL RESULTS

4.1. Turn-On Verification

The measured voltage waveform of input signal on the pad with the NANSCR as ESD protection device under normal circuit operating condition is shown in Fig. 7. The voltage waveform has no any degradation, when a 1.2-V voltage signal is applied to the pad and the gate of native NMOS in NANSCR is biased at -0.1V. So, the proposed NANSCR device does not interfere with the functions of I/O circuits or degrade the voltage level of input/output signals under normal circuit operating conditions.

The comparison of turn-on speed between NANSCR and LVTSCR under 0-to-7 V voltage pulse with the pulse rise time of 5 ns is measured and shown in Fig. 8. The W/L of native NMOS in the NANSCR under this test is 20μm/0.3μm. In Fig. 8, the turn-on speed (~10 ns) of NANSCR is faster than that (~30 ns) of LVTSCR. In addition, NANSCR can clamp the ESD-like voltage pulse to a lower voltage level than that of LVTSCR. From the experimental results, the NANSCR is more suitable than LVTSCR to quickly discharge ESD energy and to efficiently protect the ultra- thin gate oxide.

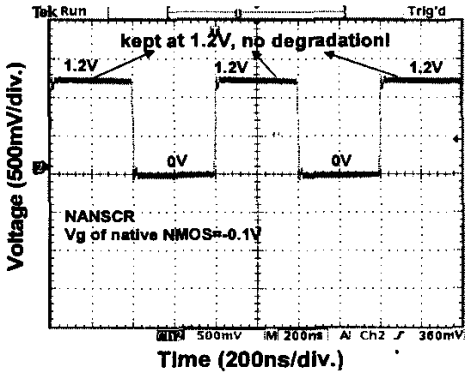

Fig. 7 The measured voltage waveform of input signal on the pad with the NANSCR device under normal circuit operating conditions, when a 1.2-V voltage signal is applied to the pad.

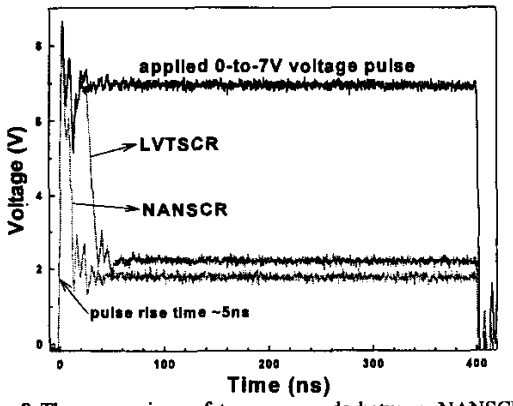

Fig. 8 The comparison of turn-on speeds between NANSCR and LVTSCR under 0-to-7 V voltage pulse with 5-ns rise time.

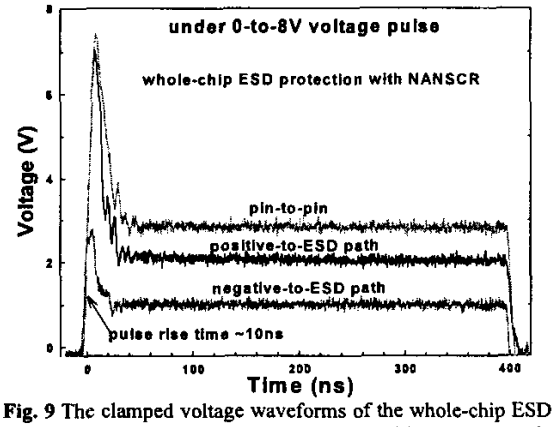

Fig. 9 The clamped voltage waveforms of the whole-chip ESD protection scheme with NANSCR under positive-to-ESD path, negative-to-ESD path, and pin-to-pin ESD-zapping conditions.

Fig. 9 verifies the turn-on waveforms (magnitude) of the whole-chip ESD protection scheme with NANSCR proposed in Fig. 6 under the positive-to-ESD path, negative-to-ESD path, and pin-to-pin ESD-zapping conditions. When a 0-to-8 V voltage pulse is applied to a pad and the ESD path is relatively grounded, the voltage waveform on the pad is clamped to ~2V by the turned-on NANSCR device. Under the negative-to-ESD path ESD-zapping condition, the amplitude of clamped voltage waveform on the zapping pad is clamped to ~1V by the forward-biased diode in the NANSCR device between the pad and ESD path. During the pin-to-pin ESD zapping, if the 0-to-8 V voltage pulse is applied to a pad_1 and a pad_2 is connected to ground, the turn-on waveform on the pad_1 can be quickly clamped to ~3 V by the already-on NANSCR device and the forward-biased diode between the pad_1 and pad_2. The turn-on speed of NANSCR and forward-biased diode under the pin-to-pin ESD-zapping condition is almost the same as that of the stand-alone NANSCR under positive-to-ESD path ESD zapping. So, the new whole-chip ESD protection scheme in Fig. 6 can successfully protect the ultra-thin gate oxide of internal circuits in the nanoscale CMOS processes against ESD stresses.

4.2. ESD Robustness

The human-body-model (HBM), machine-model (MM), and charged-device-model (CDM) ESD tests are used to verify the ESD levels of NANSCR and LVTSCR. The comparison on the ESD robustness per layout area between NANSCR and LVTSCR is summarized in Table 1. In this ESD verification, the failure criterion is defined as the measured voltage at the current level of 1μA is shifted 30% after ESD zapping. The HBM (MM) ESD levels per layout area of NANSCR and LVTSCR are almost the same and equal to ~16 (~1) V/μm^2. However, under the socket-mode CDM ESD testing, the CDM ESD level of the NANSCR is larger than that of LVTSCR. The NANSCR with gate monitor device can sustain the positive (negative) CDM ESD level per layout area of 5 (-3.75) V/μm^2, but the LVTSCR with gate monitor device can only sustain that of 2.33 (-2) V/μm^2 in the same 130-nm CMOS process.

Table 1
Comparison on the ESD robustness between NANSCR and LVTSCR

ESD stress / ESD device	HBM (V/μm^2)	MM (V/μm^2)	CDM (+) (V/μm^2)	CDM (-) (V/μm^2)
NANSCR	16.1	1.3	5	-3.75
LVTSCR	15.9	1.1	2.33	-2

Active area: NANSCR=20 μm×8 μm, LVTSCR=20 μm×7.6 μm.

The gate monitor device is also used a NMOS capacitor in these measurements. The gate of the NMOS capacitor is connected to a pad and protected by NANSCR or LVTSCR. The leakage currents of gate monitor device are the same before and after the ESD-zapping measurements. From the CDM-zapping results, the NANSCR can be indeed triggered on faster to protect the ultra-thin gate oxide of input stage and to sustain the higher CDM ESD robustness, as compared with LVTSCR.

5. CONCLUSION

A new design concept of on-chip ESD protection with the already-on NANSCR device has been successfully verified in a 130-nm CMOS process with 1.2-V voltage supply. The NANSCR with a holding voltage of 1.6V can be used in the input, output, power-rail, and whole-chip ESD protection circuits without latchup danger in CMOS IC applications with voltage supply of 1.2V. As compared with the traditional LVTSCR, NANSCR has the lower trigger voltage, smaller turn-on resistance, lower clamping voltage, faster turn-on speed, and higher CDM ESD level to protect the ultra-thin gate oxide against ESD stresses. From the experimental results, the turn-on time of NANSCR is further reduced from ~30 to only ~10 ns, when the pulse rise time is reduced from 10 to 5 ns under 6-V voltage pulse. The NANSCR can sustain the positive (negative) CDM ESD level per layout area of 5 (-3.75) V/μm^2, but the LVTSCR can only sustain that of 2.33 (-2) V/μm^2 in the same 130-nm CMOS process. For ultra large-scale CMOS ICs with multiple power pins, the proposed whole-chip ESD protection scheme with NANSCR and ESD path is the best solution to quickly discharge all kinds of ESD stresses and to provide efficient protection for the internal circuits.

6. REFERENCES

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