Cover Page (Authors Information):

Paper Title: **Co-Design on Broadband CMOS RF Distributed Amplifier With On-Chip ESD Protection Circuit (Invited Paper)**

Authors: **Ming-Dou Ker, Bing-Jye Kuo, and Yuan-Wen Hsiao**

Corresponding Author:

Prof. Ming-Dou Ker
Nanoelectronics & Gigascale Systems Laboratory
Institute of Electronics, National Chiao-Tung University
1001 Ta-Hsueh Road, Hsinchu, Taiwan 300, R.O.C.
Tel: (+886)-3-5131573
Fax: (+886)-3-5715412
e-mail: mdker@ieee.org

Suggested Topics:

1. **Solid-State Devices and Circuits**
2. **EMI and EMC**
3. **Low-Noise Devices and Techniques**

Abstract Page :

(Invited Paper)

Co-Design on Broadband CMOS RF Distributed Amplifier With On-Chip ESD Protection Circuit

Ming-Dou Ker, Bing-Jye Kuo, and Yuan-Wen Hsiao
Nanoelectronics and Gigascale Systems Laboratory
Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan

Abstract

Two distributed amplifiers (DAs) with the equal-size distributed ESD (ES-DESD) protection scheme or the decreasing-size distributed ESD (DS-DESD) protection scheme are proposed and verified in a 0.25-μm CMOS technology. The state-of-the-art ESD robustness of broadband DA circuits with human-body-model ESD level of >8kV and machine-model ESD level of 575V has been achieved by the DS-DESD protection scheme. From the experimental chips, the DA with ES-DESD protection scheme has the flat-gain of 4.7 ± 1 dB from 1 to 10 GHz. Furthermore, the DA with DS-DESD protection scheme has the flat-gain of 4.9 ± 1.1 dB from 1 to 9.2 GHz.

Co-Design on Broadband CMOS RF Distributed Amplifier With On-Chip ESD Protection Circuit

Ming-Dou Ker, Bing-Jye Kuo, and Yuan-Wen Hsiao

Nanoelectronics and Gigascale Systems Laboratory
Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan

Abstract **--** Two distributed amplifiers (DAs) with the equal-size distributed ESD (ES-DESD) protection scheme or the decreasing-size distributed ESD (DS-DESD) protection scheme are proposed and verified in a 0.25-μm CMOS technology. The state-of-the-art ESD robustness of broadband DA circuits with human-body-model ESD level of >8kV and machine-model ESD level of 575V has been achieved by the DS-DESD protection scheme. From the experimental chips, the DA with ES-DESD protection scheme has the flat-gain of 4.7 ± 1 dB from 1 to 10 GHz. Furthermore, the DA with DS-DESD protection scheme has the flat-gain of 4.9 ± 1.1 dB from 1 to 9.2 GHz.

I. Introduction

Distributed amplifiers (DAs) employ a topology, in which the capacitance contributed by the gain stages is separated, but their output currents can be still combined together. Inductive elements are used to compensate the capacitances at the input and output of the DA circuit. The value of the characteristic impedance can be adjusted according to the terminal impedance to achieve a good match over wide bandwidths.

Early DAs were implemented by using vacuum tubes and high-speed GaAs MESFETs. Recently, DAs in CMOS were also realized and reported with the advantages of both lower cost and potential high integration [1]-[7]. The operating frequencies of DAs have been going higher, and the gains have been elevated larger. However, the ESD protection, a very important issue during IC fabrication and production, was not mentioned in those works.

In this paper, the DAs co-designed with new ESD protection schemes are proposed. By dividing one ESD protection device into several equal-size parts and placing each of them before each gain stage, the first proposed ESD protection scheme is called as the equal-size distributed ESD (ES-DESD) protection. The second proposed ESD protection scheme, the decreasing-size distributed ESD (DS-DESD) protection, divides one ESD protection device into several parts with different sizes, and allocates them from input port to the gate-line terminal with decreasing sizes. The broadband performance of the DA without any ESD protection and DAs with ES-DESD or DS-DESD protection schemes have been fabricated and compared in a 0.25-μm CMOS process.

II. Distributed Amplifier

Fabricated in a standard 0.25-μm CMOS process with five-layer Al-metal interconnects, a three-stage DA with a flat gain of 5 dB or better over 10 GHz or greater bandwidth was determined to design. The staggering technique was employed in this design [8]. Defined as the ratio of the drain-line to the gate-line cutoff frequencies, the staggering value of ~ 0.7 had been analyzed as the optimum value. Besides, the m-derived half circuit with the optimum value of m = 0.6 was applied to this DA circuit [9]. With the combination of the staggering technique and the m-derived half section, the DA with ideal inductors is given in Fig. 1. However, with consideration on the parasitics from the passive components, especially the on-chip spiral inductors, the situation will be different.

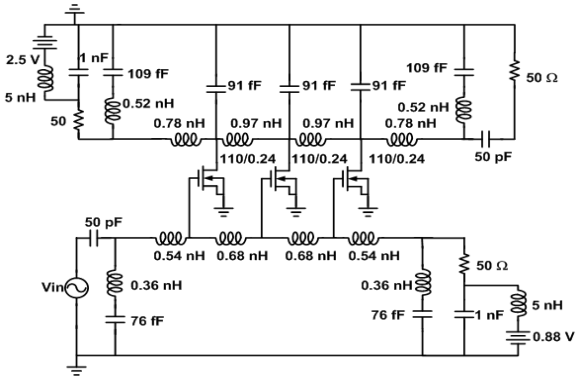


Fig. 1. Design of the distributed amplifier (DA) with ideal inductors.

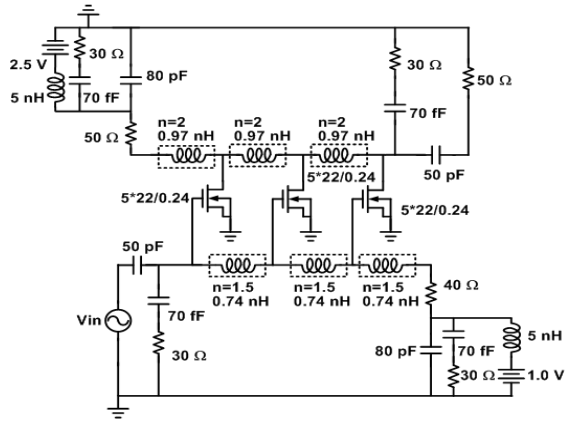


Fig. 2. Feasible DA using the on-chip spiral inductors.

With the EM simulator of ADS momentum, six on-chip spiral inductors were generated from 1 to 3.5 turns with a step of 0.5 turn. The basic structures, including the inner radius of 55 μm, top metal width of 10 μm, and the spacing between two metals of 2 μm, of these inductors were the same. After replacing the ideal inductors with the on-chip spiral inductors, the feasible DA is shown in Fig. 2. The m-derived half section was removed, due to the lack of the appropriate on-chip inductors. Without the m-derived half circuit, the S21 can not attenuate very rapidly around the cutoff frequency compared to the ideal-inductor one, as shown in Fig. 3. For the area saving and the simplicity to compare the DAs with different ESD protection schemes, the performance of the feasible DA in such a 0.25-μm CMOS process was, although not satisfactory, but acceptable.

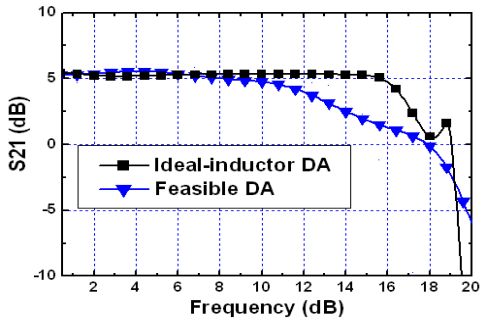


Fig. 3. Gain responses of the ideal-inductor DA and the feasible DA.

III. Distributed Amplifier with ESD Protection

Since the DA circuit is the front-end of the RF system, ESD protection is indispensable. The parasitic capacitance and resistance from the ESD protection circuit will degrade the performance of DA circuit in both matching and noise figure. To avoid these, the ESD protection components should be built with low capacitances and high Q factors. The shallow-trench-isolation (STI) diodes can fit in these two requirements [10]. Besides, they can sustain a very high ESD voltage level with the cooperation of a turn-on efficient VDD-to-VSS ESD clamp circuit [11]. However, the broadband matching over 10 GHz is still infeasible with the traditional ESD protection scheme which uses one pair of diodes close to the input pad with a VDD-to-VSS ESD clamp circuit. To achieve a comparable input broadband match of the DA after inserting the ESD protection circuit, the ESD protection components also must be separated as the MOSFETs in the DA circuit.

According to the topology discussed in [12], we proposed a DA with the equal-size distributed ESD (ES-DESD) protection circuit, as shown in Fig. 4. The STI diodes, used as ESD protection components, were divided into three sections with equal sizes to conform the gain stages of the DA. With the turn-on efficient VDD-to-VSS ESD clamp circuit, the DA with the ES-DESD protection circuit was expected to have a good ESD protection performance.

Under the ESD stress, the DA with ES-DESD protection can be approximately modeled as a simple resistive ladder, as shown in Fig. 5, where Rc represents the series resistor of the spiral inductor and Resd is the equivalent resistor of the ESD diode. The large values of Rc and Resd will degrade ESD tolerance, due to the huge power across them during ESD events. According to this consideration, the decreasing-size distributed ESD (DS-DESD) protection structure was proposed. By enlarging the area of the first pair of diodes to reduce the first Resd, usually the most possible place to be damaged by ESD, the DA with the DS-DESD protection was believed to sustain a higher ESD voltage than the DA with the ES-DESD protection.

In the ES-DESD and DS-DESD protection circuits, the total parasitic capacitance of 300 fF contributed by all the ESD diodes was chosen. The distribution on the parasitic capacitance of ESD diodes in these two ESD protection circuits are listed in Table I. Each pair of p- and n-diodes with a dimension of 5.5 × 1.2 μm^2 contributes a capacitance of 25 fF in such a 0.25-μm CMOS process with shallow trench isolation.

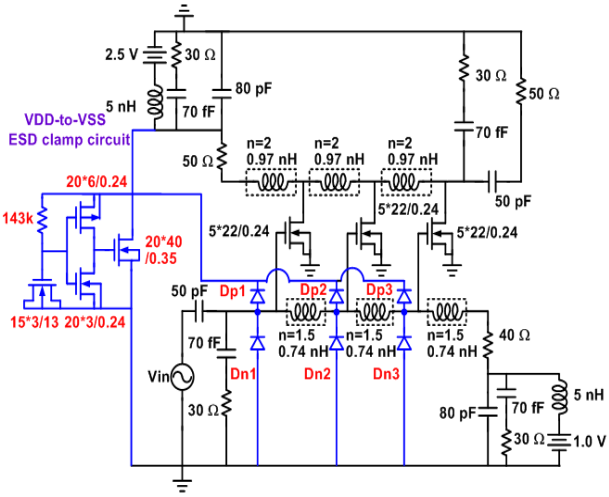


Fig. 4. DA with distributed ESD protection scheme.

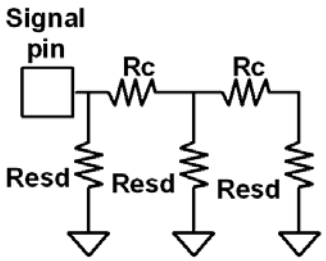


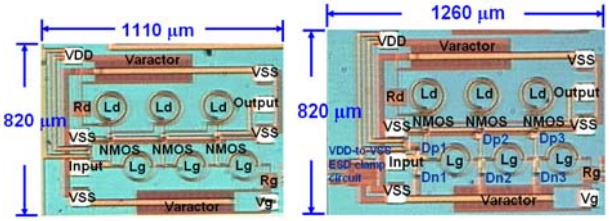
Fig. 5. The resistive-ladder model of ES-DESD protection scheme.

TABLE I
Arrangement on the capacitance distribution of ESD diodes in the DA circuits.

Circuit	Matching type	Dp1+Dn1 (fF)	Dp2+Dn2 (fF)	Dp3+Dn3 (fF)
DA1	ES-DESD	100	100	100
DA2	DS-DESD	200	75	25

IV. Experimental Results

One DA without any ESD protection and two DAs with different ESD protection schemes, listed in Table I, were implemented in a standard 0.25-μm CMOS process. The die photos of these fabricated circuits are shown in Fig. 6.



(a) (b)

Fig. 6. Die photos of (a) the DA without ESD protection and (b) the DA1 with ES-DESD protection scheme. The DA2 has a similar photo as that of DA1.

A. Broadband RF Performances

Measured on G-S-G probes with HP 85122A (high frequency modeling system) from 1 GHz to 18 GHz, the power gains (S21) of the DA without ESD protection compared to those of the simulated one, DA1 with ES-DESD protection, and DA2 with DS-DESD protection are shown in Fig. 7. The probed response of the DA without ESD protection correlates well with the response of post- simulation, but still some differences exist. The post- simulation was operated with the addition of interconnects used in the layout. The effects of interconnects were obtained from the EM simulator of ADS momentum. The simulated response of DA circuit without any ESD protection is +5 dB with a ±1-dB flatness from 1 GHz to 10 GHz and a unity-gain frequency of 15.1 GHz. However, the measured response of the fabricated DA circuit without any ESD protection is 5 dB with a ±1-dB flatness from 1 GHz to 11.4 GHz and a unity-gain frequency of 16.7 GHz. The deviation of the performance can be attributed to several reasons, including the inaccuracy of the simulated spiral inductors, the variation of the terminal resistances, and the imprecise estimation of the bond pad effects, etc.

The reason in Fig. 7 that DA2 (with the flat-gain of 4.9 ± 1.1 dB from 1 to 9.2 GHz) achieves a better gain response than DA1 (with the flat-gain of 4.7 ± 1 dB from 1 to 10 GHz) might be the decreasing parasitic capacitances of the ESD diodes compensating the miller effect in each gain stage with the increasing gain. As seen in Fig. 8, the simulated and measured phase shifts of the DA without ESD protection both present roughly linear curves from 1 to 16 GHz, but DA1 and DA2 only maintain the same situation up to 14 GHz. The noise figure was measured by HP85122A (high frequency modeling system) and ATN NP5B (noise parameters extraction software) from 1 GHz to 18 GHz. The results are shown in Fig. 9. The measured data of the DA without ESD protection achieves the lowest value of 4.4 dB at 6 GHz and the largest value of 5.6 dB at 1 GHz. The lowest value in measurement larger than that of 3.6 dB in simulation may be mainly attributed to the incomplete noise models in MOSFETs. In DA1 and DA2, the lowest noise figures are 0.5 and 0.6 dB higher than that of the DA without ESD protection, which implies that the ESD diodes indeed contribute the extra noise.

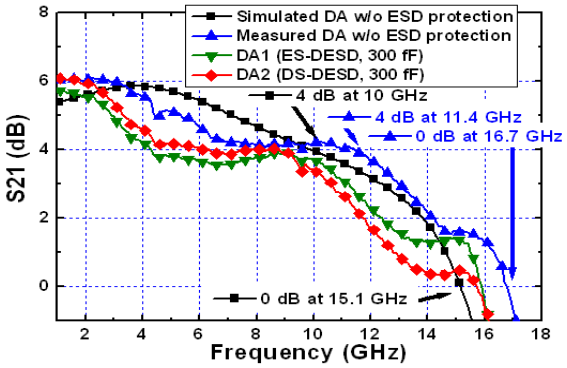


Fig. 7. Comparison of S21 among the simulated and fabricated DAs without ESD protection, DA1 with ES-DESD protection, and DA2 with DS-DESD protection.

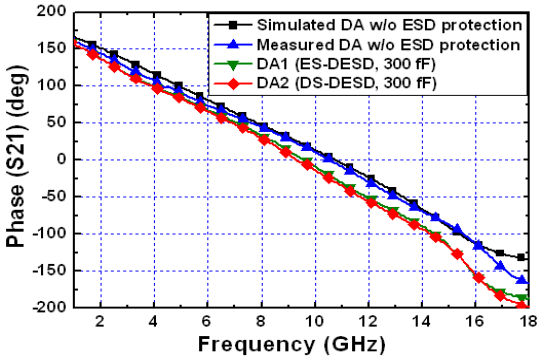


Fig. 8. Phase shifts among the simulated and fabricated DAs without ESD protection, DA1 with ES-DESD protection, and DA2 with DS-DESD protection.

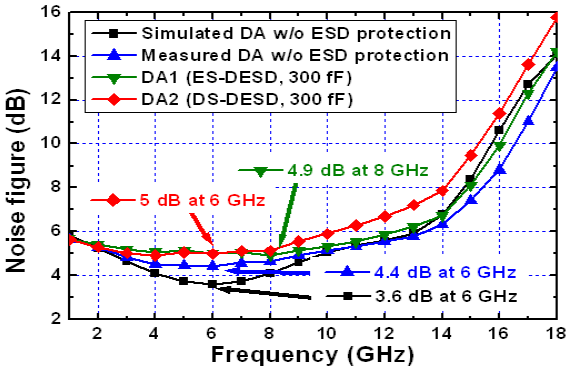


Fig. 9. Noise figures among the simulated and fabricated DAs without ESD protection, DA1 with ES-DESD protection, and DA2 with DS-DESD protection.

B. ESD Robustness

To compare ESD robustness, the DA without ESD protection, DA1 with ES-ESD protection, and DA2 with DS-ESD protection have been tested according to the ESD test standards with a failure criterion of 30% I-V curve shifting at 1-μA current. The typical I-V curves of DA2 before and after the positive-to-VSS ESD stress with a machine-model (MM) ESD voltage

of 575V are compared in Fig. 10. The human-body-model (HBM) and MM ESD test results among the DA circuits are summarized in Table II, where includes the positive-to-VSS (PS) and negative-to-VDD (ND) pin combinations during ESD stresses. I/O Pins of IC products under the PS and ND modes of ESD stresses often have the worst ESD robustness. As seen in Table II, the DA without ESD protection only can sustain a very low ESD level, which is far below the required ESD protection level, 2 kV in HBM and 200 V in MM. The ESD robustness of the DA improves after inserting the distributed ESD protection circuit into it. The enhancement of ESD robustness is very enormous that DA1 with the ES-DESD protection scheme achieves the HBM ESD level of 5.5 kV and the MM ESD level of 325 V. Furthermore, with the same total parasitic capacitance (300fF) of ESD diodes, DA2 with the DS-DESD protection scheme can tolerate the higher ESD stress. The HBM test result of DA2 can be greater than 8 kV and the MM test result of 575 V, which is the state-of-the-art record on ESD robustness of broadband RF circuits.

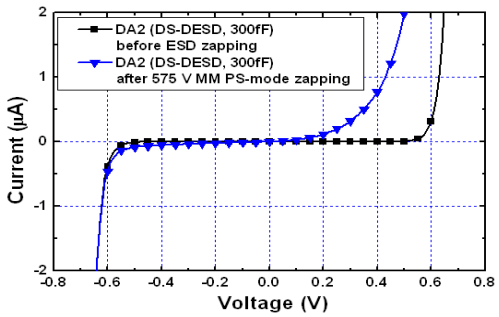


Fig. 10. I-V curve shifts of DA2 before and after positive-to-VSS MM ESD stress.

TABLE II
HBM and MM ESD test results among the fabricated DA circuits.

ESD-Stress Modes	HBM (kV)		MM (V)	
	ND mode	PS mode	ND mode	PS mode
DA without ESD protection	0.2	0.25	~20	~20
DA1 (ES-DESD, 300fF)	7.5	5.5	400	325
DA2 (DS-DESD, 300fF)	>8	>8	650	575

C. Failure Analysis

The EMMI (photon emission microscope) picture in Fig. 11 has shown that the ESD damage, indicated by the arrow, is located on the junction of the first p-diode with a large shining area after the positive-to-VSS MM ESD stress. As analyzed in the resistive ladder model in Fig. 5, the ESD current is mainly discharged through the shortest path of the first stage of ESD diodes which contributes the lowest resistance. This evidence has confirmed that the DS-DESD protection scheme to DA circuits can indeed improve ESD robustness than using the ES-DESD protection scheme.

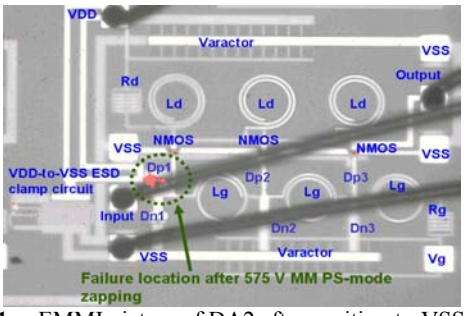


Fig. 11. EMMI picture of DA2 after positive-to-VSS ESD stress with MM ESD voltage of 575 V.

V. Conclusion

Two new broadband ESD protection schemes for DA circuits have been proposed and successfully verified in a 0.25-μm CMOS process. From the experimental results, the DA with ES-DESD protection scheme has ESD robustness of HBM 5.5kV and MM 325V. The DA with DS-DESD protection scheme has ESD robustness of HBM >8kV and MM 575V. By using this new proposed ESD protection scheme, both of RF performance and ESD robustness can be successfully co-designed in the broadband RF amplifiers.

References

[1] P. J. Sullivan, B. A. Xavier, and W. H. Ku, "An integrated CMOS distributed amplifier using packaging inductance," *IEEE Trans. on Microwave Theory Tech.*, vol. 45, pp. 1969-1975, Oct. 1997.

[2] B. M. Ballweber, R. Gupta, and D. J. Allstot, "A fully integrated 0.5–5.5-GHz CMOS distributed amplifier," *IEEE J. Solid-State Circuits*, vol. 35, pp. 231-239, Feb. 2000.

[3] H. Ahn and D. J. Allstot, "A 0.5–8.5-GHz fully differential CMOS distributed amplifier," *IEEE J. Solid-State Circuits*, vol. 37, pp. 985-993, Aug. 2002.

[4] B. Kleveland, C. H. Diaz, D. Vook, L. Madden, T. H. Lee, and S. Wong, "Monolithic CMOS distributed amplifier and oscillator," in *Dig. Tech. Papers of IEEE Int. Solid-State Circuits Conf.*, 1999, pp. 70-71.

[5] B. M. Frank, A. P. Freundorfer, and Y. M. M. Antar, "Performance of 1-10-GHz traveling wave amplifiers in 0.18-μm CMOS," *IEEE Microwave Wireless Compon. Lett.*, vol. 12, pp.327-329, Sept. 2002.

[6] R.-C. Liu, K.-L. Deng, and H. Wang, "A 0.6-22-GHz broadband CMOS distributed amplifier," in *Dig. Tech. Papers of IEEE Radio Freq. Integrated Circuit Symp.*, 2003, pp. 103-106.

[7] R.-C. Liu, C.-S. Lin, K.-L. Deng, and H. Wang, "A 0.5-14-GHz 10.6-dB CMOS cascode distributed amplifier," in *Dig. Tech. Papers of Symp. VLSI Circuits*, 2003, pp.139-140.

[8] D. G. Sarma, "On distributed amplification," in *Proc. of Inst. Elect. Eng.*, 1954, pp. 689-697.

[9] D. M. Pozar, *Microwave Engineering*. Reading, MA: Addison-Wesley, 1990.

[10] R. M. D. A. Velghe, P. W. H. de Vreede, and P. H. Woerlee, "Diode network used as ESD protection in RF applications," *in Proc. of EOS/ESD Symp.*, 2001, pp. 337-345.

[11] M.-D. Ker, "Whole-chip ESD protection design with efficient VDD-to-VSS ESD clamp circuits for submicron CMOS VLSI," *IEEE Trans. on Electron Devices*, vol. 46, pp. 173-183, Jan. 1999.

[12] C. Ito, K. Banerjee, and R. W. Dutton, "Analysis and design of distributed ESD protection circuits for high-speed mixed-signal and RF ICs," *IEEE Trans. on Electron Devices*, vol. 49, pp. 1444-1454, Aug. 2002.