NATIVE-NMOS-TRIGGERED SCR (NANSCR) FOR ESD PROTECTION IN 0.13-μm CMOS INTEGRATED CIRCUITS

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ABSTRACT

A novel native-NMOS-triggered SCR (NANSCR) is proposed for efficient ESD protection design in a 0.13-μm CMOS process. As compared with the traditional LVTSCR, the trigger voltage, turn-on resistance, turn-on speed, and CDM ESD level of NANSCR have been greatly improved to protect the ultra-thin gate oxide against ESD stresses. The proposed NANSCR can be designed for the input, output, and power-rail ESD protection circuits without latchup danger in a 0.13-μm CMOS process with VDD of 1.2 V. A new whole-chip ESD protection scheme realized with the NANSCR devices has been also demonstrated with the consideration of pin-to-pin ESD zapping. [*Keywords:* ESD, ESD protection circuit, SCR, latchup, CDM, HBM.]

I. INTRODUCTION

For CMOS IC applications with a maximum voltage level of VDD below 1.2 V, SCR can be a great candidate for on-chip ESD protection due to its highest ESD robustness, smallest layout area, and free to latchup issue, as compared with non-SCR ESD protection devices. But, the SCR still has a higher trigger voltage of ~18 V in a 0.13-μm CMOS process, which is generally greater than the gate-oxide breakdown voltage of the input stages. Furthermore, the gate oxide thickness has been scaled down to only ~25 Å, and its time-to-breakdown (t_{BD}) or charge-to-breakdown (Q_{BD}) will also be decreased in the same CMOS process. So, it is imperative to reduce the trigger voltage and turn-on time of SCR for efficiently protecting the ultra-thin gate oxide from latent damage or rupture [1], especially against the fast charged-device-model (CDM) ESD events. Some reports had presented the solutions to reduce the trigger voltage of SCR device [2]-[7] for protecting the thin gate oxide.

In this paper, a native NMOS with almost zero threshold voltage is first used to trigger on SCR device during ESD events. The novel native-NMOS- triggered SCR (NANSCR) has the lower trigger voltage, smaller turn-on resistance, lower holding voltage, faster turn-on speed, and higher CDM ESD level than those of a traditional LVTSCR, therefore it is more suitable to protect the ultra-thin gate oxide. The NANSCR can be used in the input, output, power-rail, and whole-chip ESD protection circuits without latchup danger in CMOS IC applications with voltage supply of 1.2 V.

II. DEVICE CHARACTERISTICS OF NANSCR

The native NMOS is directly built in a lightly-doped p-type substrate, whereas the normal NMOS (PMOS) is in a heavily-doped p-well (n-well) in a P-substrate twin-well CMOS technology, as shown in Fig. 1. The native NMOS is fully process-compatible with the standard CMOS process without adding extra mask. The threshold voltage of native NMOS is almost zero (~0.1V), however, that of normal NMOS is about 0.34 V in a 0.13-μm CMOS process. The native NMOS and lateral SCR are merged together to be a novel ESD protection device, native-NMOS-triggered SCR (NANSCR), which is first proposed in this literature.

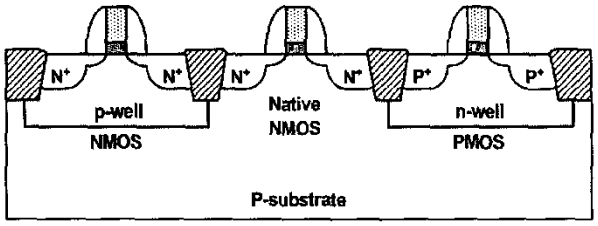

Fig. 1 The device cross-sectional views of the NMOS, PMOS, and native NMOS in a P-substrate twin-well CMOS technology.

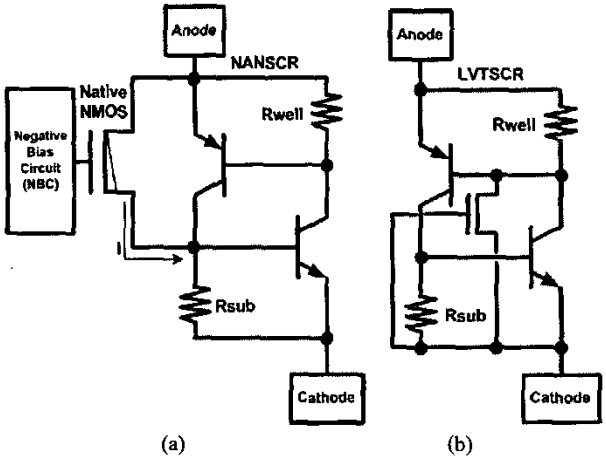

Fig. 2 The circuit schematics of (a) the proposed native-NMOS-triggered SCR (NANSCR) and (b) the traditional LVTSCR.

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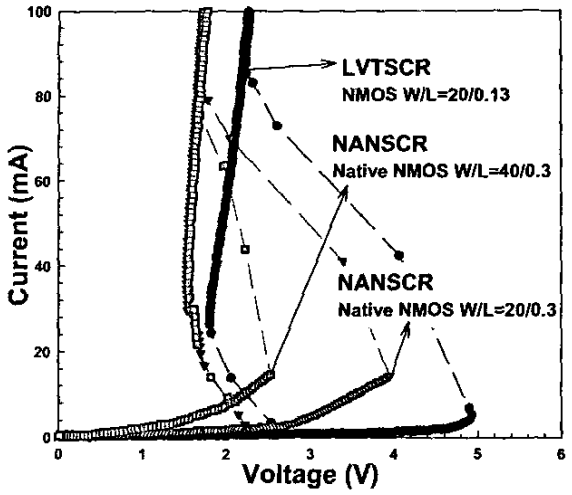

Fig. 3 The DC I-V curves of the NANSCR and LVTSCR.

The circuit schematics of NANSCR and LVTSCR are shown in Figs. 2(a) and 2(b), respectively. The drain of native NMOS in NANSCR is directly coupled to the pad of anode, but the drain of NMOS in LVTSCR is located across the n-well/p-well junction of the SCR device. The gate of native NMOS is connected to a negative bias circuit (NBC) [8] to turn off the NANSCR, but the gate of NMOS in LVTSCR is connected to VSS to ensure that LVTSCR is off, under normal circuit operating conditions.

The new proposed NANSCR device and the traditional LVTSCR device have been fabricated in a 0.13-μm salicided CMOS process. Both of them are fully-silicided devices without extra silicide-blocking mask. In the experimental test chip, the active area (without including the guard rings) of SCR in NANSCR is drawn as 20μm×8μm. The active area of LVTSCR is drawn as 20μm×7.5μm, and the W/L of NMOS within LVTSCR is 20μm/0.13μm.

The comparison of DC I-V curves between NANSCR and LVTSCR is shown in Fig. 3. The native NMOS in NANSCR structure has two different device dimensions of 20μm/0.3μm and 40μm/0.3μm for comparison. With the substrate-triggered technique [6], the trigger voltage of NANSCR with native NMOS of 20-μm channel width is about ~4 V, which is smaller than that (~5 V) of LVTSCR. So, the NANSCR can be triggered on faster than the LVTSCR. Moreover, if the channel width of native NMOS in NANSCR is increased to 40μm, the trigger voltage of NANSCR with native NMOS of 40-μm channel width can be further reduced to only ~2.5 V.

The NANSCR with lower trigger voltage can clamp ESD overstress voltage more quickly. The turn-on resistance and holding voltage of NANSCR are also smaller than those of LVTSCR in Fig. 3. Therefore, the voltage on the pad clamped by the NANSCR will be lower than that clamped by the LVTSCR under the same ESD stress. The holding voltage of NANSCR is about ~1.6 V, which is immune from latchup issue in CMOS ICs with 1.2-V voltage supply. Such a holding voltage of NANSCR is still low enough to provide higher ESD robustness, as compared with other ESD protection devices.

III. On-Chip ESD Protection With NANSCR

A. ESD Protection Circuit for I/O Pads

The ESD protection circuit for input or output pads, which is realized with NANSCR devices, is shown in Fig. 4. The n-well in NANSCR_1 is connected to VDD, but not connected to I/O pad. The gates of native NMOS in the NANSCR_1 and NANSCR_2 are connected to the same negative bias circuit (NBC). Under normal circuit operating conditions, the gates of native NMOS in all NANSCR devices are biased by the same NBC to turn off the NANSCR devices. So, the NANSCR_1 and NANSCR_2 will not interfere with the functions of I/O circuits, whenever the input/output signals are logic high (VDD) or logic low (VSS). Because the holding voltage of NANSCR (~1.6 V) is greater than the maximum voltage level (1.2 V) of input/output signals, the transient-induced latchup issue in such NANSCR devices is vanished.

Under the positive-to-VSS (PS) ESD-zapping condition (with grounded VSS but floating VDD), the gate of native NMOS in the NANSCR_1 is floating. The NANSCR_1 is triggered on quickly by the triggering current generated from the already-on native NMOS. So, the positive ESD current can be effectively discharged from the I/O pad through the NANSCR_1 to grounded VSS line. Under the negative-to-VDD (ND) ESD-zapping condition (with grounded VDD but floating VSS), the gate of native NMOS in the NANSCR_2 is floating but with an initial voltage level of 0 V. The negative ESD voltage at the I/O pad will pull down the source voltage of native NMOS through the base-emitter junction of NPN in the NANSCR_2 device. Therefore, the native NMOS in NANSCR_2 will be turned on first, resulting in the NANSCR_2 being triggered on. The negative ESD current will be discharged from the I/O pad through the NANSCR_2 to grounded VDD line.

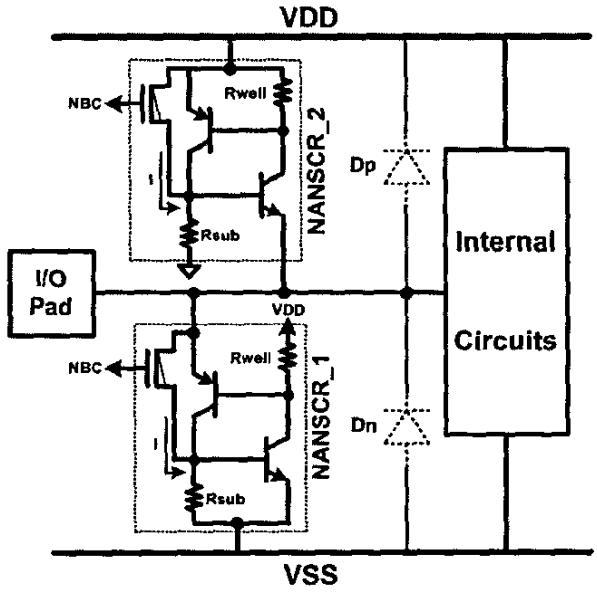

Fig. 4 Design of ESD protection circuit for the input or output pads with the proposed NANSCR devices.

B. ESD Clamp Circuit between Power Rails

The VDD-to-VSS ESD clamp circuit realized with the NANSCR device is shown in Fig. 5. Under normal circuit operating conditions, the NBC is active to turn off the NANSCR device. When a positive ESD pulse is applied on the VDD line with grounded VSS line, the NANSCR device will be quickly triggered on by the already-on native NMOS to discharge the positive ESD current to grounded VSS line. If a negative ESD pulse is applied on the VDD line with grounded VSS line, the parasitic diode (P-substrate/n-well junction) in the NANSCR structure will be forward biased to discharge the negative ESD current.

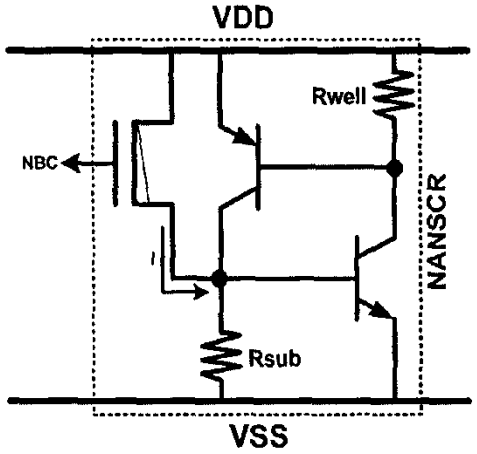

Fig. 5 The VDD-to-VSS ESD clamp circuit realized with the NANSCR device.

C. Whole-Chip ESD Protection Scheme

A new whole-chip ESD protection scheme with the proposed NANSCR devices is shown in Fig. 6. The anode terminals of NANSCR devices are all connected to the pads (including I/O, VDD, and VSS pads) and their cathode terminals are all connected to the ESD path. The ESD path indicated by the bold line in Fig. 6 can be realized with the wide and top metal line in the chip to efficiently discharge the ESD current of several amperes during ESD events. The gates of native NMOS in the NANSCR devices are biased by an on-chip NBC to fully turn off all NANSCR devices under normal circuit operating conditions.

During ESD-zapping condition, the NANSCR devices without negative bias in the whole-chip ESD protection scheme can be triggered on more quickly to effectively protect the internal circuits. Except the four modes of ESD stresses on the I/O pads with VDD or VSS grounded, all pin-to-pin ESD-zapping conditions (such as input-to-input, output-to-output, input-to-output, or VDD-to-VSS, or VSS-to-VDD can be fully protected by this whole-chip ESD protection scheme. By using this new whole-chip ESD protection scheme, the pin-to-pin ESD stress can be discharged through only a NANSCR, the ESD path, and a parasitic diode between the zapping pin and the grounded pin.

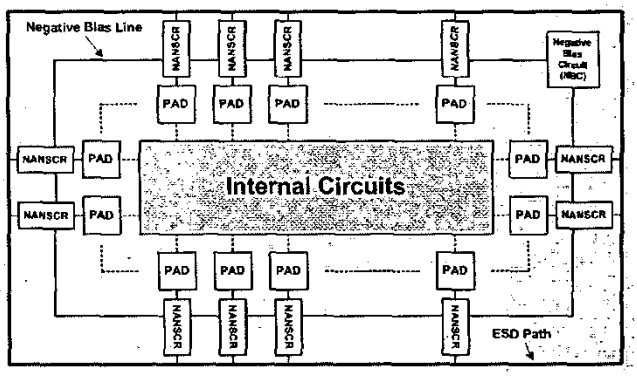

Fig. 6 The new whole-chip ESD protection scheme realized with the NANSCR devices.

IV. Experimental Results

A. Turn-On Verification

The measured voltage waveform of input signal on the pad with the NANSCR as ESD protection device under normal circuit operating condition is shown in Fig. 7. The voltage waveform has no any degradation, when a 1.2-V voltage signal is applied to the pad and the gate of native NMOS in NANSCR is biased at -0.1V. So, the proposed NANSCR device does not interfere with the functions of I/O circuits or degrade the voltage level of input/output signals under normal circuit operating conditions.

The comparison of turn-on speed between NANSCR and LVTSCR under 0-to-7 V voltage pulse with the pulse rise time of 5 ns is measured and shown in Fig. 8. The W/L of native NMOS in the NANSCR under this test is 20μm/0.3μm. In Fig. 8, the turn-on speed (~10 ns) of NANSCR is faster than that (~30 ns) of LVTSCR. In addition, NANSCR can clamp the ESD-like voltage pulse to a lower voltage level than that of LVTSCR. From the experimental results, the NANSCR is more suitable than LVTSCR to quickly discharge ESD energy and to efficiently protect the ultra-thin gate oxide.

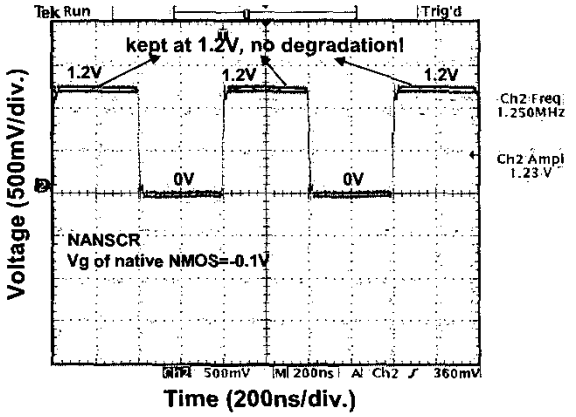

Fig. 7 The measured voltage waveform of input signal on the pad with the NANSCR device under normal circuit operating conditions, when a 1.2-V voltage signal is applied to the pad.

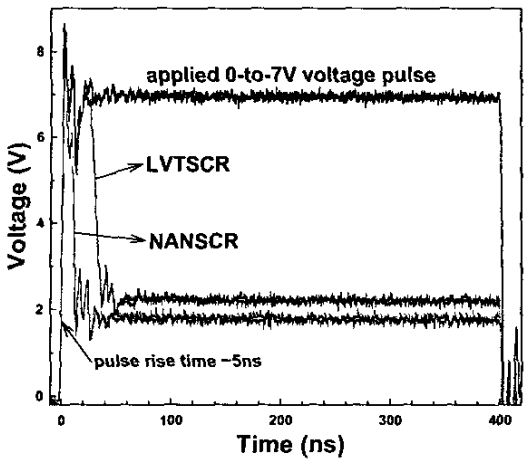

Fig. 8 The comparison of turn-on speeds between NANSCR and LVTSCR under 0-to-7 V voltage pulse with 5-ns rise time.

The dependence of turn-on speeds of NANSCR under different pulse rise times and pulse voltages are shown in Figs. 9(a) - 9(c). When a 0-to-5 V voltage pulse is applied to the pad with NANSCR, the voltage waveform on the pad is clamped to a low voltage level, as shown in Fig. 9(a). The gate-floated native NMOS in NANSCR will be first turned on to clamp the ESD-like voltage pulse. Because the native NMOS is already on, it will conduct some ESD current to trigger on the SCR device and then the SCR clamps the voltage pulse to 1.6 V. If the pulse voltage is increased to 6 V and the pulse rise time is kept at ~10 ns in Fig. 9(b), the NANSCR can be triggered into latching state more quickly due to the substrate-triggered technique [4]. Moreover, the turn-on time of NANSCR is significantly reduced from ~30 to only ~10 ns, when the rise time of 6-V voltage pulse is reduced to ~5 ns in Fig. 9(b). However, the turn-on speeds of NANSCR are the same in Fig. 9(c), when the 6-V or 8-V voltage pulses with a fixed 5-ns rise time are applied. Fig. 9(c) shows that the dominated factor on the turn-on speed of the proposed NANSCR is the pulse rise time, but not the overshoot transient voltage, if the high enough voltage pulse is applied. The turn-on time of NANSCR will trace the rise time of ESD event (even the CDM stress) to efficiently protect the ultra-thin gate oxide, if the high enough voltage pulse has been applied to the NANSCR.

Fig. 10 verifies the turn-on waveforms (magnitude) of the whole-chip ESD protection scheme with NANSCR in Fig. 6 under the positive-to-ESD path, negative-to-ESD path, and pin-to-pin ESD-zapping conditions. When a 0-to-8 V voltage pulse is applied to a pad and the ESD path is relatively grounded, the voltage waveform on the pad is clamped to ~2 V by the turned-on NANSCR device. Under the negative-to-ESD path ESD-zapping condition, the amplitude of clamped voltage waveform on the zapping pad is clamped to ~1 V by the forward-biased diode in the NANSCR device between the pad and ESD path. During the pin-to-pin ESD zapping, if the 0-to-8 V voltage pulse is applied to a pad_1 and a pad_2 is connected to ground, the turn-on waveform on the pad_1 can be quickly clamped to ~3 V by the turned-on NANSCR device and the forward-biased diode between the pad_1 and pad_2. The turn-on speed of NANSCR and forward-biased diode under the pin-to-pin ESD-zapping condition is almost the same as that of the stand-alone NANSCR under positive-to-ESD path ESD zapping. So, the new whole-chip ESD protection scheme in Fig. 6 can successfully protect the ultra-thin gate oxide of internal circuits against various ESD-zapping tests.

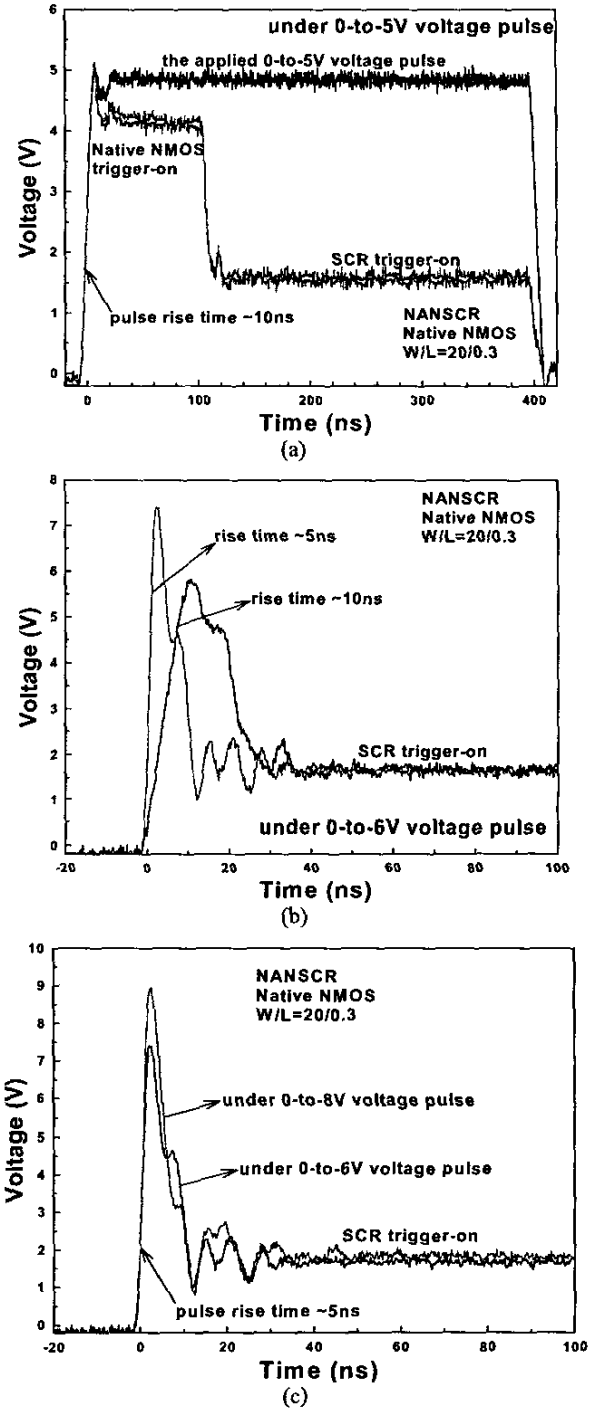

Fig. 9 (a) The turn-on waveform of NANSCR under 5-V voltage pulse with 10-ns rise time. The turn-on speeds of NANSCR (b) under 6-V voltage pulse with different rise times and (c) under different pulse voltages with the same rise time of 5ns.

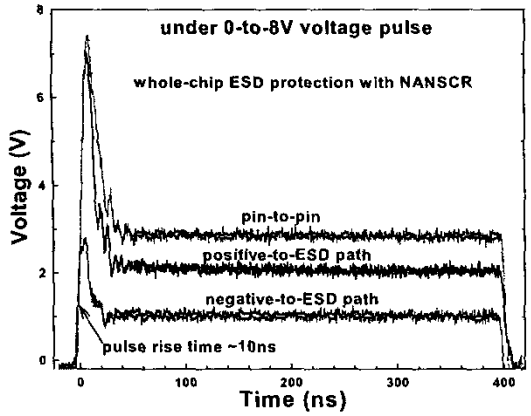

Fig. 10 The clamped voltage waveforms of the whole-chip ESD protection scheme with NANSCR under positive-to-ESD path, negative-to-ESD path, and pin-to-pin ESD-zapping conditions.

B. EMMI Photographs

The measured EMMI photographs on the turn-on behavior of NANSCR under different voltage pulses are shown in Figs. 11(a) - 11(d). Fig. 11(a) shows the initial EMMI photograph of NANSCR under the voltage pulse of 0 V, where there is no hot spot in the NANSCR structure. When the pulse voltage is increased to 5 V, the hot spots are shown to locate at the native NMOS in Fig. 11(b), which indicates the turn-on of native NMOS. When a 5.8-V voltage pulse is applied to the pad, the hot spots are located at both of the native NMOS and the SCR device in Fig. 11(c), which means that SCR has been triggered on. If the pulse voltage is further increased to 6 V, all hot spots will be located at the SCR device and the hot spot in native NMOS will vanish in Fig. 11(d). With the increase of pulse voltage, the ESD current path, as shown by the hot spots, is initially discharged from the native NMOS to trigger SCR into latching state, and then fully discharged through SCR device, as those shown in Figs. 11(b) - 11(d).

C. TLP Measurement

The It2 of fully-silicided NANSCR and LVTSCR devices under the conditions with or without gate monitor device and the corresponding measurement setups are shown in Fig. 12. The gate monitor device is a NMOS capacitor to verify the effectiveness of ESD protective device. The It2 of NANSCR is almost the same as that of LVTSCR, but the turn-on resistance of NANSCR (~3 ohm) is smaller than that of LVTSCR (~5.1 ohm) under the TLP-measured conditions, which corresponds to the DC-measured result in Fig. 3. Under the breakdown limitation of ultra-thin gate oxide of input stage, the NANSCR with smaller turn-on resistance can sustain more ESD current than that of LVTSCR with larger turn-on resistance. Moreover, the NANSCR devices have the same It2 per micron of ~80 mA/μm, under the measured conditions with or without the gate monitor device. The leakage currents of gate monitor device are the same before and after the TLP measurements. Therefore, the ultra-thin gate oxide of input stage can be fully protected by the new proposed NANSCR against ESD stress.

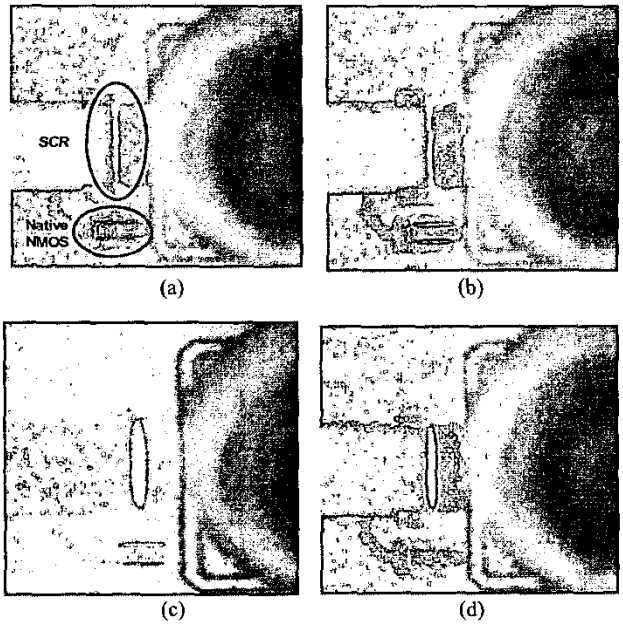

Fig. 11 The measured EMMI photographs of NANSCR device under the pulsed voltage stresses of (a) 0V, (b) 5V, (c) 5.8V, and (d) 6V.

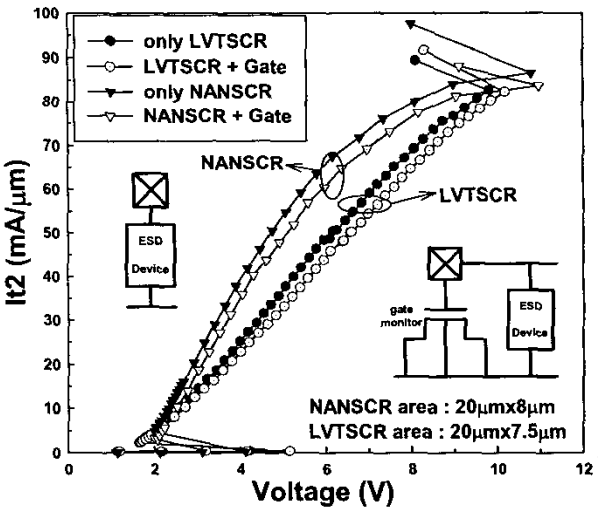

Fig. 12 The TLP-measured I-V curves of NANSCR and LVTSCR under the conditions with or without the gate monitor device.

D. ESD Robustness

The human-body-model (HBM), machine-model (MM), and charged-device-model (CDM) ESD tests are used to verify the ESD levels of NANSCR and LVTSCR. The comparison on the ESD robustness per layout area between NANSCR and LVTSCR is summarized in Table I. In this ESD verification, the failure criterion is defined as the measured voltage at the current level of 1μA is shifted 30% after ESD zapping. The HBM (MM) ESD levels per layout area of NANSCR and LVTSCR are almost the same

and equal to ~16 (~1) V/μm^2. However, under the socket-mode CDM ESD testing, the CDM ESD level of the NANSCR is larger than that of LVTSCR. The NANSCR with gate monitor device can sustain the positive (negative) CDM ESD level per layout area of 5 (-3.75) V/μm^2, but the LVTSCR with gate monitor device can only sustain that of 2.33 (-2) V/μm^2 in the same 0.13-μm CMOS process.

The gate monitor device is also used a NMOS capacitor in these measurements. The gate of the NMOS capacitor is connected to a pad and protected by NANSCR or LVTSCR. The leakage currents of gate monitor device are the same before and after the ESD-zapping measurements. From the CDM-zapping results, the NANSCR can be indeed triggered on faster to protect the ultra-thin gate oxide of input stage and to sustain the higher CDM ESD robustness, as compared with LVTSCR.

TABLE I
Comparison on the human-body-model (HBM), machine-model (MM), and charged-device-model (CDM) ESD robustness between NANSCR and LVTSCR.

ESD stress / ESD device	HBM (V/μm^2)	MM (V/μm^2)	CDM (+) (V/μm^2)	CDM (-) (V/μm^2)
NANSCR	16.1	1.3	5	-3.75
LVTSCR	15.9	1.1	2.33	-2

Active area: NANSCR=20 μm×8 μm, LVTSCR=20 μm×7.5 μm.

V. CONCLUSION

The novel native-NMOS-trigger SCR (NANSCR) has been successfully investigated in a 0.13-μm CMOS process with 1.2-V voltage supply. The NANSCR with holding voltage of 1.6 V can be designed free to latchup issue for 1.2-V CMOS ICs. As compared with the traditional LVTSCR, NANSCR has the lower trigger voltage, smaller turn-on resistance, lower clamping voltage, faster turn-on speed, and higher CDM ESD level to protect the ultra-thin gate oxide against ESD stresses. From the experimental results, the turn-on time of NANSCR is further reduced from ~30 to only ~10 ns, when the pulse rise time is reduced from 10 to 5 ns under 6-V voltage pulse. The NANSCR can sustain the positive (negative) CDM ESD level per layout area of 5 (-3.75) V/μm^2, but the LVTSCR can only sustain that of 2.33 (-2) V/μm^2 in the same 0.13-μm CMOS process. For ultra large-scale CMOS ICs with multiple power pins, the proposed whole-chip ESD protection scheme with NANSCR and ESD path is an overall solution to quickly discharge all kinds of ESD stresses and to provide efficient protection for the internal circuits.

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