ESD Protection Design for I/O Cells in Sub-130-nm CMOS Technology with Embedded SCR Structure

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***Abstract*—This paper presents a new electrostatic discharge (ESD) protection design for input/output (I/O) cells with embedded silicon-controlled rectifier (SCR) structure as power-rail ESD clamp device in a 130-nm CMOS process. Two new embedded SCR structures without latchup danger are proposed to be placed between the input (or output) pMOS and nMOS devices of the I/O cells. Furthermore, the turn-on efficiency of embedded SCR can be significantly increased by substrate-triggered technique. By including the efficient power-rail ESD clamp device into each I/O cell, whole-chip ESD protection scheme can be successfully achieved within a small silicon area of I/O cell.**

I. INTRODUCTION

On-Chip electrostatic discharge (ESD) protection circuits have to be added between the input/output (I/O) pad and VDD/VSS to provide the desired ESD robustness in CMOS integrated circuits (ICs) [1]. The typical design of on-chip ESD protection circuits in a CMOS IC is illustrated in Fig. 1. The pMOS and nMOS are used as on-chip ESD protection devices for input and output pads. To avoid the unexpected ESD damage in the internal circuits of CMOS ICs [2], the turn-on-efficient power-rail ESD clamp circuit must be placed between VDD and VSS power lines [3]. ESD stresses on an I/O pad have four pin-combination modes: positive-to-VSS (PS-mode), negative-to-VSS (NS-mode), positive-to-VDD (PD-mode), and negative-to-VDD (ND-mode). ESD current at the I/O pad under the PS-mode ESD stress can be discharged through the parasitic diode of pMOS and the VDD-to-VSS ESD clamp circuit to ground. However, due to the parasitic resistance and capacitance along the VDD and VSS power lines, ESD protection efficiency is dependent on the pin location in a chip [3].

In the traditional I/O cells, double guard rings have been often inserted between input (or output) pMOS and nMOS devices to avoid the latchup issue, as shown in Fig. 2. For CMOS IC applications, SCR can be a great candidate for on-chip ESD protection due to its highest ESD robustness, smallest layout area, and excellent clamping capabilities (low holding voltage and small turn-on resistance), which can provide efficient ESD protection to the ultra-thin gate oxide in nanoscale CMOS process [4]. However, SCR device was susceptible to latchup danger under normal circuit operating condition [5]. With the scaled-down device dimension in nanoscale CMOS technology, the power supply voltage is also scaled down to meet the circuit requirement and gate-oxide reliability. The maximum supply voltage is only 1.2V in a 130-nm CMOS technology. If the holding voltage of SCR device is greater than the power supply voltage, latchup issue will not occur in such nanoscale CMOS process.

In this paper, SCR is used as VDD-to-VSS ESD clamp device within each I/O cell in a 130-nm CMOS process without latchup issue. Two new embedded SCR structures are proposed to replace the double guard rings in the traditional I/O cells. The turn-on speed of embedded SCR structures is enhanced to quickly discharge ESD current by substrate-triggered technique [6].

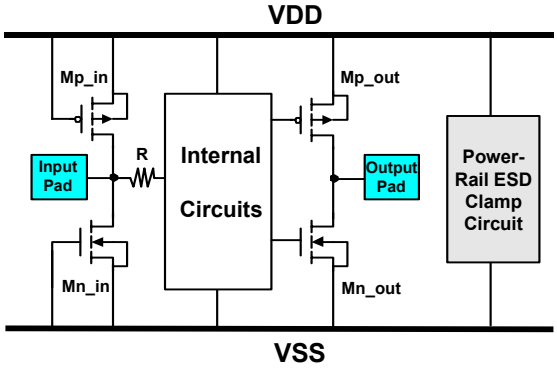

Figure 1. Typical design of on-chip ESD protection circuits in a CMOS IC.

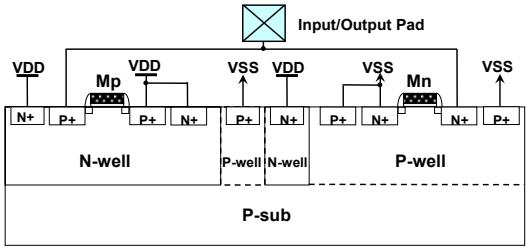

Figure 2. Device structures of the traditional I/O cell with double guard rings inserted between input (or output) pMOS and nMOS devices.

II. EMBEDDED SCR STRUCTURES IN I/O CELLS

If the holding voltage of parasitic SCR is greater than the maximum voltage level of circuit operation, the double guard rings surrounding the input (or output) pMOS and nMOS devices in the I/O cells can be removed. Thus, the parasitic SCR structure between input (or output) pMOS and nMOS devices can be used as power-rail ESD clamp device in each I/O cell. The layout view and device structures of new proposed I/O cell with embedded SCR structure I are shown in Figs. 3 (a) and (b), respectively. Keeping the single guard ring in the I/O cell, the anode and cathode of embedded SCR structure I are formed by inserting the extra p+ diffusion in n-well and the extra n+ diffusion in p-well, respectively. The p+ diffusion inserted half in n-well and half in p-well is connected out as substrate-triggered node. When a trigger current is applied into this trigger node, SCR will be triggered into its latching state quickly through the positive feedback regeneration mechanism [7]. The layout area of the I/O cell can be further reduced by the new proposed I/O cell with embedded SCR structure II, as shown in Fig. 4. Without the double guard rings, the anode and cathode of embedded SCR structure II are directly formed by the source of input (or output) pMOS and the source of nMOS, respectively. The poly gate in the layout view has a close-loop ring to increase the anode and cathode areas of embedded SCR structure II.

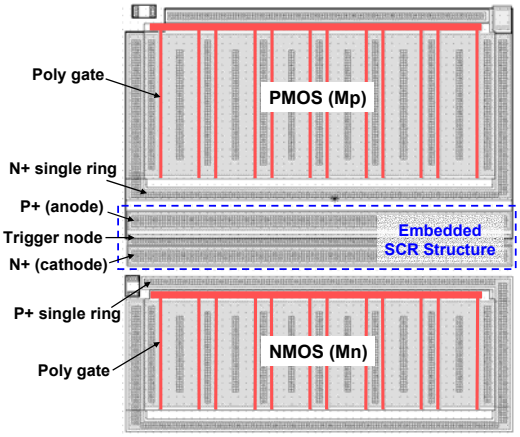

Figure 3. (a) Layout view and (b) device structures of the new proposed I/O cell with embedded SCR structure I. The anode and cathode of embedded SCR structure I are formed by inserting the extra p+ diffusion in n-well and the extra n+ diffusion in p-well, respectively.

The new proposed whole-chip ESD protection scheme with embedded SCR structure as power-rail ESD clamp device in each I/O cell is shown in Fig. 5. The substrate-triggered technique can be realized by the RC-based ESD detection circuit [6]. With the embedded SCR structure in each I/O cell, the whole-chip ESD protection efficiency is not degraded by the different pin locations in the chip. This will be more valuable for system-on-a-chip (SOC) applications with hundreds of I/O pins.

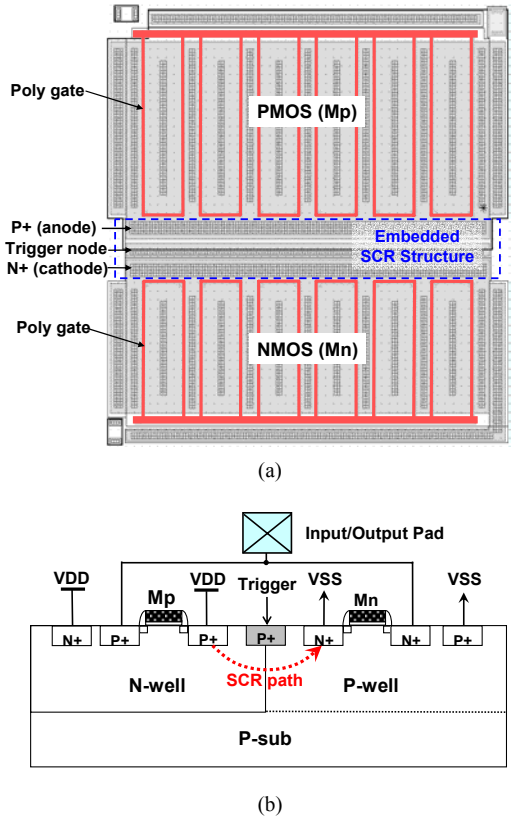

Figure 4. (a) Layout view and (b) device structures of new proposed I/O cell with embedded SCR structure II. The anode and cathode of embedded SCR structure II are directly formed by the source of input (or output) pMOS and the source of nMOS, respectively.

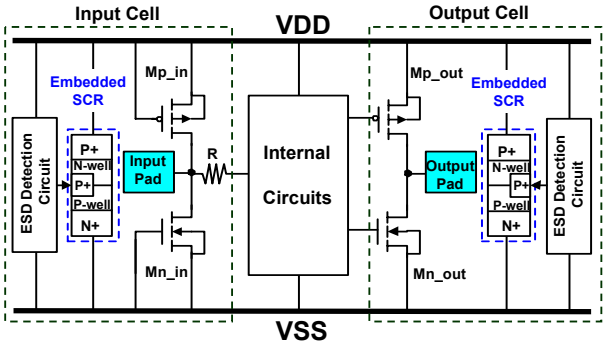

Figure 5. The new proposed whole-chip ESD protection scheme with embedded SCR structure in each I/O cell. The substrate-triggered technique was realized by the RC-based ESD detection circuit.

III. Experimental Results

The testchips with the traditional I/O cells and the new proposed I/O cells have been fabricated in a 130-nm salicided CMOS process. The input (or output) pMOS and nMOS devices are realized with the device dimensions (W/L) of 240/0.18 and 180/0.18 (μm/μm), respectively. The layout parameters of input ESD protection devices and output buffers are drawn according to the foundry's ESD rules. In the new proposed I/O cells, the embedded SCR structure I and II are fully silicided with the SCR device widths of 49.5 and 45.5μm, respectively. The spacing from anode to cathode of the embedded SCR structure is kept at 2.35μm.

A. DC I-V Characteristics

The dc I-V characteristics of embedded SCR structures I and II in the I/O cells under different temperatures (measured by a Tek370 curve tracer) are shown in Figs. 6(a) and (b), respectively. The insets in Fig. 6 are the dependences of holding voltage of the embedded SCR structures under different temperatures. The holding voltage of embedded SCR structures slightly reduces when the temperature is increased. With smaller equivalent well resistance, the holding voltage of embedded SCR structure I is larger than that of embedded SCR structure II. The holding voltages of embedded SCR structures I and II at temperature of 125°C are 1.54V and 1.27V, respectively. The measured results have verified that the embedded SCR structures can be safely applied in 1.2-V CMOS ICs without latchup issue.

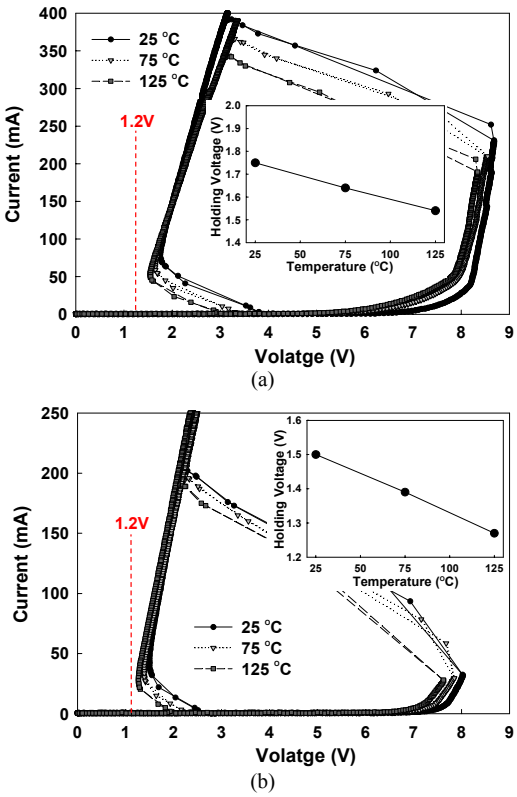

Figure 6. The I-V characteristics of the (a) embedded SCR structure I, and (b) embedded SCR structure II, in the I/O cells under different temperatures.

B. TLP I-V Characteristics

The TLP-measured (transmission line pulsing system, TLP) I-V characteristics of the I/O cells with embedded SCR structures under positive VDD-to-VSS ESD stress with or without ESD detection circuit are shown in Fig. 7(a). The enlarged view around the switching point for I/O cells with ESD detection circuit is shown in Fig. 7(b). The switching voltages of embedded SCR structures I and II can be reduced to only 2.7V and 1.74V, respectively, by the ESD detection circuit without involving the avalanche junction breakdown mechanism. Therefore, the switching voltage of embedded SCR structure can be significantly reduced by substrate-triggered technique to ensure effective ESD protection. The second breakdown current (It2) per micron of embedded SCR structure is as high as ~100mA/μm, without using the silicide-blocking process modification.

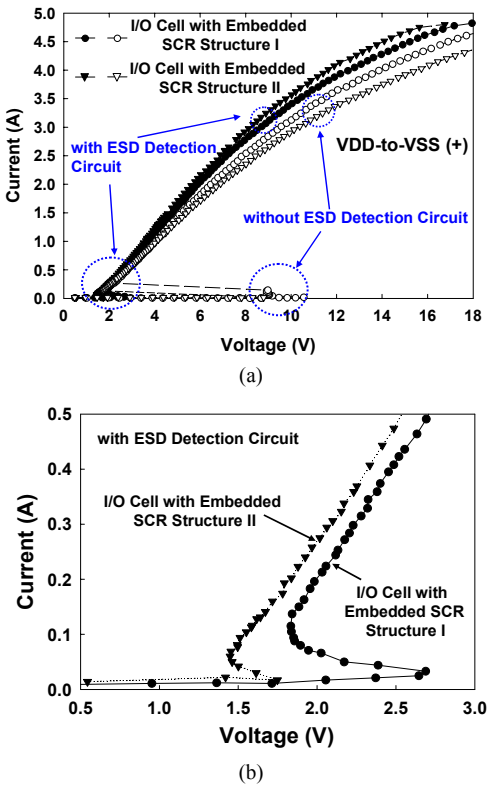

Figure 7. (a) The TLP-measured I-V curves of the I/O cells with embedded SCR structures I and II under positive VDD-to-VSS ESD stress. (b) The enlarged view around the switching point of the measured curves.

The TLP-measured I-V curves of I/O cells with or without embedded SCR structure under PS-mode ESD stress are compared in Fig. 8. From the measured results, the new proposed I/O cells with embedded SCR structure have lower switching voltage, lower clamping voltage level, smaller turn-on resistance, and higher ESD robustness, as compared with the traditional I/O cells. The It2 of I/O cell with embedded SCR structure under PS-mode ESD stress can be increased to ~3A. Therefore, the ESD level of I/O cell can be efficiently improved by inserting the embedded SCR structure in I/O cell. The TLP-measured I-V curves of the

input pad under PS-mode ESD stress with or without silicide blocking on the input pMOS and nMOS devices are shown in Fig. 9. The It2 of the input pad under PS-mode ESD stress with silicide blocking on pMOS and nMOS devices is ~3A, and that without silicide blocking is ~2A. Whereas, the embedded SCR structures are fully silicided in these I/O cells. For fully silicided process, the It2 is dropped because the input nMOS device can sustain less ESD current when the parasitic npn bipolar transistor is triggered on.

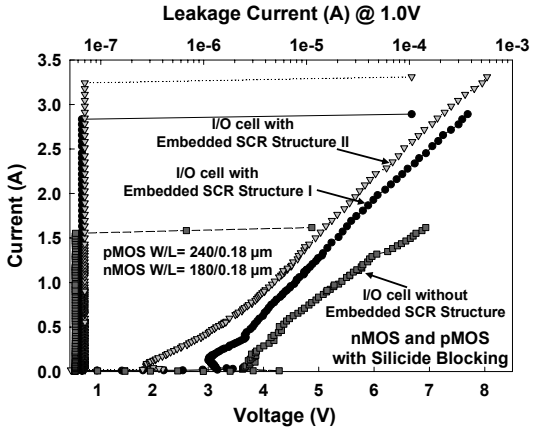

Figure 8. The TLP-measured I-V curves of the input pad under positive-to-VSS ESD stress with or without embedded SCR structure, where the embedded SCR structures are fully silicided.

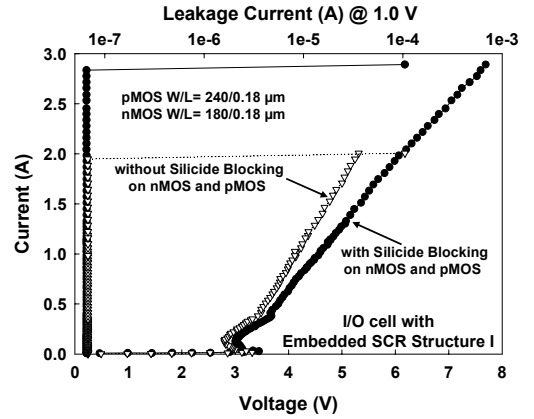

Figure 9. The TLP-measured I-V curves of the input pad under positive-to-VSS ESD stress with or without silicide blocking on the input pMOS and nMOS devices, where the embedded SCR structures are fully silicided.

C. *ESD Robustness*

To verify the ESD robustness of the new proposed ESD protection scheme, the output buffer of pMOS and nMOS in the output cell are individually controlled by the input cells. The SCR structure is embedded in each I/O cell. The human-body-model (HBM) ESD robustness of the new proposed ESD protection scheme with embedded SCR structures I and II under different pin combinations is listed in Table I. The failure criterion is defined as 30% corresponding I-V curve shifting at 1-µA current bias. With the embedded SCR structure I, the ESD level of the I/O pads is 4.5kV, which is dominated by the I/O pad under PS-mode ESD stress. With the embedded SCR structure II, the ESD level of the I/O pads is 5.0kV, which is dominated by the I/O pad under NS-mode ESD stress. From the failure analysis, the ESD damages of the I/O cells with embedded SCR structures under PS-mode and NS-mode ESD stresses are located at input or output nMOS device.

TABLE I
HBM ESD ROBUSTNESS OF THE NEW PROPOSED ESD PROTECTION SCHEME WITH EMBEDDED SCR STRUCTURE IN EACH I/O CELL

HBM ESD Stress / ESD Protection Scheme	PS-Mode VSS (+)	NS-Mode VSS (-)	PD-Mode VDD (+)	ND-Mode VDD(-)	VDD-to-VSS (+)	VDD-to-VSS (-)
I/O Cells with Embedded SCR I (Input Pad)	5.0kV	7.5kV	>8kV	>8kV	>8kV	>8kV
I/O Cells with Embedded SCR I (Output Pad)	4.5kV	7.75kV	>8kV	>8kV		
I/O Cells with Embedded SCR II (Input Pad)	5.5kV	5.5kV	>8kV	>8kV	>8kV	>8kV
I/O Cells with Embedded SCR II (Output Pad)	5.5kV	5.0kV	>8kV	>8kV		

Silicide Blocking only on nMOS and pMOS
Input/Output pMOS W/L= 240/0.18 (µm) SCR I width= 49.5 (µm)
Input/Output nMOS W/L= 180/0.18 (µm) SCR II width= 45.5 (µm)

IV. CONCLUSION

An area-efficient ESD protection design for I/O cells in a 130-nm CMOS technology with embedded SCR structures has been proposed and verified. The embedded SCR structures can be safely applied in 1.2-V CMOS ICs without latchup danger. The turn-on speed of SCR can be significantly enhanced by substrate-triggered technique. By including the embedded SCR structure as the power-rail ESD clamp device in each I/O cell, one set of high-ESD-robust and high-area-efficient I/O cells have been developed in a 130-nm CMOS technology for SOC applications.

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