# New Curvature-Compensation Technique for CMOS Bandgap Reference with Sub-1-V Operation

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***Abstract* — A new sub-1-V curvature-compensated CMOS bandgap reference, which utilizes the temperature-dependent currents generated from the parasitic NPN and PNP BJT devices in CMOS process, is presented. The new proposed sub-1-V curvature-compensated CMOS bandgap reference has been successfully verified in a standard 0.25-μm CMOS process. The experimental results have verified that, at the minimum supply voltage of 0.9 V, the output reference voltage is 536.7 mV with a temperature coefficient of 19.55 ppm/°C from 0 °C to 100 °C. With 0.9-V supply voltage, the measured power noise rejection ratio is -25.5 dB at 10 kHz.**

## I. Introduction

Reference circuit is one of the basic building blocks in many applications of analog, mixed-mode, and memory circuits. The demand for low-voltage reference is especially apparent in the battery-operated mobile products, such as cellular phones, PDA, camera recorders, and laptops [1].

In CMOS technology, the parasitic vertical bipolar junction transistors (BJT) had been used to implement the high-precision bandgap voltage references. However, the conventional CMOS bandgap reference did not work in near 1-V supply voltage. The reason, that the minimum supply voltage can not be lower than 1 V, is constrained by two factors. One is that the bandgap output voltage is around 1.25 V [2], [3], which exceeds 1-V supply. The other is that the low-voltage design of the proportional to absolute temperature current generation loop is limited by the input common-mode voltage of the amplifier [2], [4]. These two limitations can be solved by using the resistive subdivision methods [5], [6], low-threshold voltage (or native) device [5]-[7], BiCMOS process [4], or DTMOST [8]. However, the bandgap reference working in low supply voltage has a higher temperature coefficient than that of traditional bandgap reference. This has resulted in the development of new temperature compensated techniques such as quadratic temperature compensation [9], exponential temperature compensation [10], piecewise-linear curvature correction [11], and resistor temperature compensation [12]. To implement these advanced mathematical functions with high accuracy, the development of the low-voltage bandgap structure requires precision matching of current mirrors or a pre-regulated supply voltage. Cascode current mirror [9], [11], and pre-regulated circuit [12] are good methods to solve this problem. But, the minimum supply voltage is the tradeoff.

In this work, the new proposed sub-1-V curvature-compensated CMOS bandgap reference can be successfully operated with sub-1-V supply in a standard 0.25-μm CMOS process without special process technology. The new proposed bandgap voltage reference with a stable output voltage $V_{REF}$ of 536.7 mV and a temperature coefficient of 19.55 ppm/°C under $V_{DD}$ power supply of 0.9 V has been successfully proven in the silicon chip.

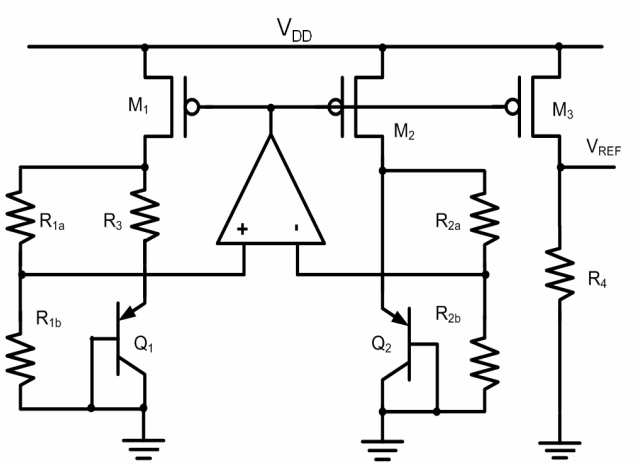


Fig. 1. The traditional sub-1-V bandgap reference circuit.

## II. Conventional Sub-1-V Bandgap Reference Circuit

A typical sub-1-V CMOS bandgap reference is shown in Fig. 1 [2]. The output reference voltage $V_{REF}$ of the conventional sub-1-V bandgap reference circuit can be written as

$$V_{REF-SUB-1-V} = \frac{R_4}{R_1}\left(V_{EB2} + \frac{R_1}{R_3}\frac{kT}{q}\ln N\right), \quad (1)$$

where $R_1$ is $R_{1a}$ + $R_{1b}$ or $R_{2a}$ + $R_{2b}$, $k$ is Boltzmann's constant ($1.38\times10^{-23}$ J/K), $q$ is electronic charge ($1.6\times10^{-19}$ C), and $N$ is the emitter area ratio between $Q_1$ and $Q_2$. The $R_{1a}$ is designed equal to $R_{2a}$, and $R_{1b}$ is designed equal to $R_{2b}$. By adjusting the resistance ratio of $R_{1b}$ over $R_{1a}$ + $R_{1b}$ ($R_{2b}$ over $R_{2a}$ + $R_{2b}$), the sub-1-V bandgap reference uses

the resistive subdivision method to reduce the input common-mode voltage of operational amplifier. This makes the p-channel input pair of operational amplifier operated in the saturation region easily, even if the supply voltage is under 1 V. However, the temperature coefficient of such sub-1-V bandgap reference is higher than that of general high- voltage bandgap reference.

## III. New Proposed Curvature–Compensated CMOS Bandgap Reference

The design concept of the new proposed curvature-compensation technique is illustrated in Fig. 2. The proposed curvature-compensation technique has two output reference currents $I_1$ and $I_2$, which are generated by two traditional current-mode bandgap references [6] of Fig. 1. Both currents act with concave up and down curves. The curves have similar shapes in the temperature region, and they are designed with the same center temperature $T_0$ where the temperature coefficient of $V_{REF}$ is zero. The only difference is that the current $I_2$ is larger than $I_1$ in magnitude. By the current mirrors, a temperature independent current generated from the difference between $K_1I_1$ and $K_2I_2$ can be produced. Hence, an output reference voltage with very low sensitivity to temperature is obtained across the resistor $R_{REF}$. Thus, the bandgap reference has the excellent curvature-compensated performance.

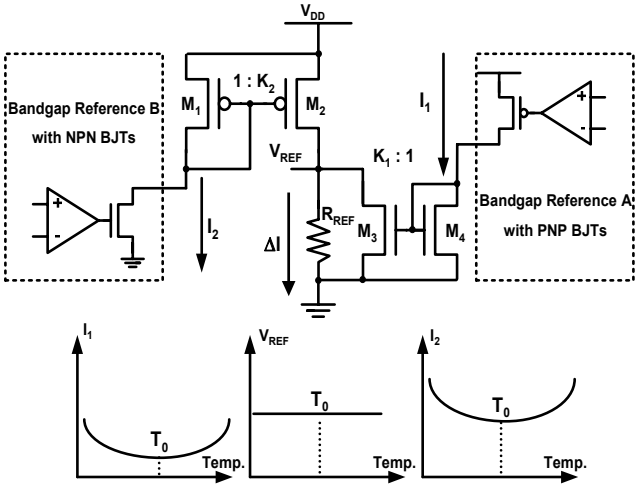


Fig. 2. The new proposed sub-1-V curvature-compensated bandgap reference circuit.

The current $I_1$ comes from a traditional current-mode bandgap reference A with PNP BJTs, while $I_2$ is produced by another traditional current-mode bandgap reference B with NPN BJTs. The parasitic vertical NPN BJT in a standard 0.25-μm CMOS process is implemented with deep n-well. The output reference current of the traditional current-mode CMOS bandgap reference of Fig. 1 is given by

$$I_{M2} = \frac{V_{BE2}}{R_1} + \frac{1}{R_3}\frac{kT}{q}\ln(\mathrm{N}). \tag{2}$$

According to (2), the $I_1$ can be written as

$$I_1 = \frac{V_{BE\_PNP}}{R_{1\_PNP}} + \frac{1}{R_{3\_PNP}}\frac{kT}{q}\ln N_{PNP}. \tag{3}$$

Similarly, $I_2$ can be expressed as

$$I_2 = \frac{V_{BE\_NPN}}{R_{1\_NPN}} + \frac{1}{R_{3\_NPN}}\frac{kT}{q}\ln N_{NPN}. \tag{4}$$

Thus, the difference current $\Delta I = K_2I_2 - K_1I_1$ is written as

$$\begin{aligned}\Delta I = &\left(\frac{K_2}{R_{1\_NPN}} - \frac{K_1}{R_{1\_PNP}}\right)(V_{BE\_NPN} - V_{BE\_PNP}) \\ &+ \frac{kT}{q}\left(\frac{K_2 \ln N_{NPN}}{R_{3\_NPN}} - \frac{K_1 \ln N_{PNP}}{R_{3\_PNP}}\right),\end{aligned} \tag{5}$$

where $K_1$ is the device ratio between $M_3$ and $M_4$, and $K_2$ is the device ratio between $M_1$ and $M_2$. If the $lnN_{NPN}$ and $lnN_{PNP}$ have the same value and the proper pairs of $R_{1\_NPN}$, $R_{1\_PNP}$, $R_{3\_NPN}$, $R_{3\_PNP}$, $K_1$, and $K_2$ are chosen, the difference current ($\Delta I$) will become a temperature-independence current. Therefore, a temperature-independence voltage can be achieved across $R_{REF}$, which has the lowest temperature coefficient. The output voltage can be expressed as

$$\begin{aligned}V_{REF} &= R_{REF}(K_2I_2 - K_1I_1) \\ &= R_{REF}\left[\begin{array}{l}\left(\frac{K_2}{R_{1\_NPN}} - \frac{K_1}{R_{1\_PNP}}\right)\left(V_{BE\_NPN} - V_{BE\_PNP}\right) \\ + \frac{kT}{q}\left(\frac{K_2 \ln N_{NPN}}{R_{3\_NPN}} - \frac{K_1 \ln N_{PNP}}{R_{3\_PNP}}\right)\end{array}\right],\end{aligned} \tag{6}$$

where $ln\ N$ is equal to $ln\ N_{NPN}$ and $ln\ N_{PNP}$. Thus, the new proposed sub-1-V curvature-compensated CMOS bandgap reference has the excellent curvature-compensated performance.

## IV. Circuit Implementation

The whole complete circuit to realize the new proposed sub-1-V curvature-compensated CMOS bandgap reference is shown in Fig. 3. The startup circuit is not shown in Fig. 3. The proposed sub-1-V curvature-compensated bandgap reference is composed by two sub-1-V bandgap cores [6] with two operational amplifiers. The current $I_1$ in Fig. 3 is produced by a traditional sub-1-V bandgap reference with two PNP transistors and a p-channel input pair of operational amplifier. The current $I_2$ is produced by another traditional sub-1-V bandgap reference with NPN transistors and an n-channel input pair of operational amplifier. The output voltage of the sub-1-V bandgap reference is similar to (6), but the $R_{1\_NPN}$ and $R_{1\_PNP}$ are set to $R_{1a\_NPN} + R_{1b\_NPN}$

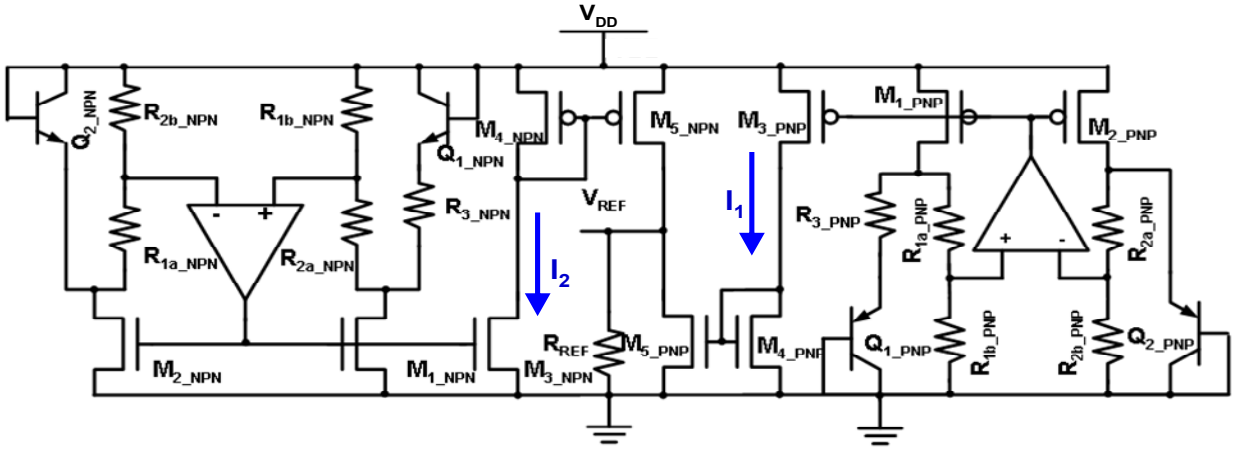


Fig. 3. Complete circuit of the new proposed curvature-compensated bandgap reference.

(or $R_{2a\_NPN} + R_{2b\_NPN}$) and $R_{1a\_PNP} + R_{1b\_PNP}$ (or $R_{2a\_PNP} + R_{2b\_PNP}$), respectively. The minimum supply voltage of the new proposed sub-1-V curvature- compensated bandgap reference is given by

$$V_{DD(Min.)} = Max\left[\begin{array}{l}\left(\frac{R_{1b\_PNP}}{R_{1a\_PNP}+R_{1b\_PNP}}V_{EB2\_PNP}+|V_{THP}|+2|V_{DSsat}|\right),\\ \left(\frac{R_{1b\_NPN}}{R_{1a\_NPN}+R_{1b\_NPN}}V_{EB2\_NPN}+V_{THN}+2V_{DSsat}\right)\end{array}\right], \quad (7)$$

where $V_{THP}$ and $V_{THN}$ are threshold voltages of PMOS and NMOS, respectively. Since the base-emitter voltage of a bipolar transistor in the equation (7) is multiplied by the resistance ratio, this circuit can work with sub-1-V supply voltage. Another important factor of the bandgap reference is the power noise rejection ratio (*PSRR*) [8]. The *PSRR* of the new proposed sub-1-V curvature-compensation bandgap reference is simply expressed as

$$\frac{V_{REF}(S)}{V_{DD\,Noise}(S)} = \frac{1}{SCr_{oM5\_NPN} + \frac{r_{oM5\_NPN}}{(R_{REF}\,//\,r_{oM5\_PNP})} + 1}, \quad (8)$$

where $r_{oM5\_NPN}$ and $r_{oM5\_PNP}$ are turn-on resistances of $M_{5\_NPN}$ and $M_{5\_PNP}$, respectively. The capacitance $C$ is $C_{DBM5\_NPN} + C_{DBM5\_PNP} + C_{DSM5\_PNP} + C_{DSM5\_NPN} + C_{GDM5\_NPN} + C_{GDM5\_PNP}$, which are the parasitic drain-bulk, drain-source, and gate-drain capacitances connected to the $V_{REF}$ node.

## V. Experimental Results

### A. Simulation

The proposed bandgap reference has been simulated during the operating temperature from 0 to 100 °C. The temperature coefficient is around 7.57 ppm/°C with the supply voltage of 1 V. The dependence of $V_{REF}$ (output reference voltage) on the operating temperature is shown in Fig. 4 under different power supply voltages (from 0.85 to 1.2 V). With the supply voltage at 0.85 V, the temperature coefficient grows sharply above 200 ppm/°C. The dependence of $V_{REF}$ on the supply voltage is shown in Fig. 5 under the temperatures of 0, 25, and 100 °C. The curves of output reference voltages under the temperatures of 0, 25, and 100 °C grow together while the supply voltage of the proposed bandgap reference is above 0.9 V. This means that the minimum supply voltage for the new proposed bandgap reference can be as low as 0.9 V.

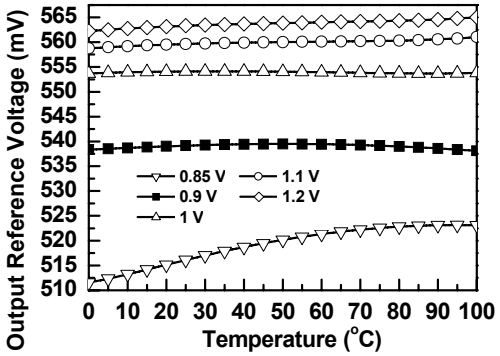


Fig. 4. Simulated reference voltage of the new proposed bandgap reference with different supply voltages.

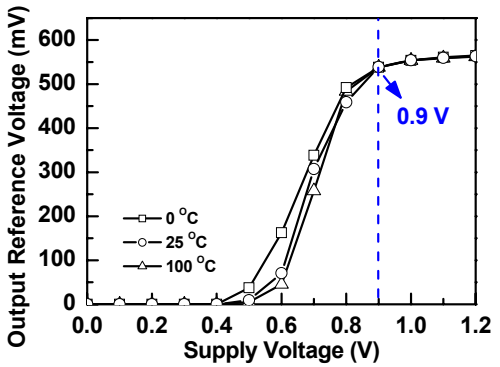


Fig. 5. Simulation to find the minimum supply voltage of the new proposed bandgap reference.

B. Silicon Verification

The proposed bandgap reference has been fabricated in a 0.25-μm single-ploy-five-metal (1P5M) CMOS technology. The proposed sub-1-V curvature-compensated bandgap reference consists of the bandgap cores, bipolar transistors, and resistors. Fig. 6 shows the overall die photo of the new sub-1-V curvature-corrected bandgap reference. The occupied silicon area of the new proposed bandgap reference is only 480 μm × 226 μm. The bandgap reference has been measured with the operating temperature varying from 0 to 100 °C. The power supply voltage was set from 0.85 to 1.2 V. The measured results are shown in Fig. 7. The temperature coefficient is around 13.49 ppm/°C with the supply voltage at 1 V. The experimental results in Fig. 8 have confirmed that the minimum supply voltage for the new proposed sub-1-V curvature-compensated bandgap reference is 0.9 V with a temperature coefficient of 19.55 ppm/°C. The measured power noise rejection ratio is -25.5 dB at 10 kHz, and output reference voltage is 536.7 mV under the $V_{DD}$ power supply of 0.9 V.

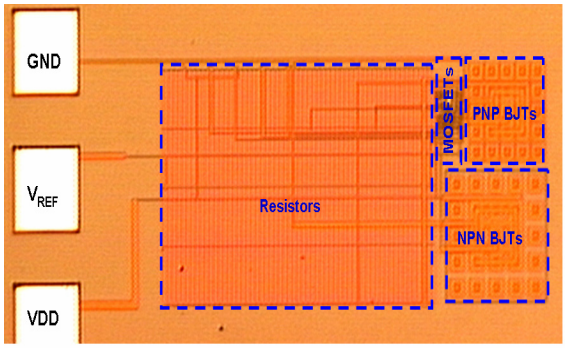


Fig. 6. Die photo of the new proposed bandgap reference fabricated in a 0.25-μm CMOS process.

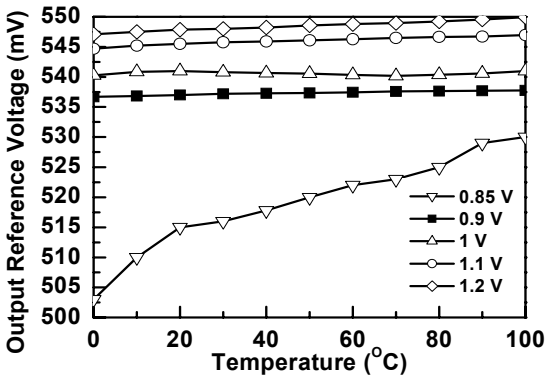


Fig. 7. Dependence of output reference voltage on the operating temperature under different $V_{DD}$ voltage levels.

## VI. Conclusion

A new CMOS bandgap voltage reference with $V_{REF}$ of 536.7 mV and temperature coefficient of 19.55 ppm/°C under the supply voltage of 0.9 V has been designed and verified, which consumes a maximum current of 50 μA at 0.9 V. The sub-1-V operation of the curvature-compensated bandgap reference has been successfully achieved in silicon chip. The proposed curvature-compensated technique used to improve the temperature coefficient of sub-1-V bandgap reference can be implemented in general CMOS technology.

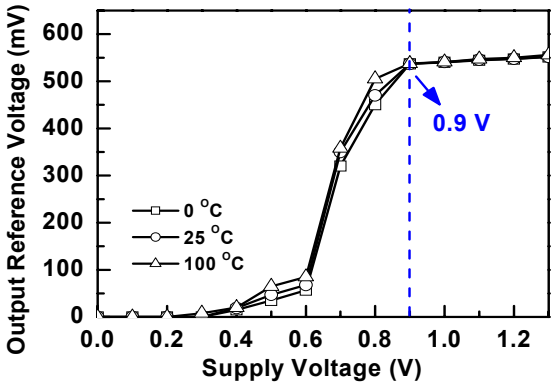


Fig. 8. Dependence of output reference voltage on the $V_{DD}$ supply voltage under different operating temperatures.

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