Design on Mixed-Voltage I/O Buffer With Blocking NMOS and Dynamic Gate-Controlled Circuit for High-Voltage-Tolerant Applications

Ming-Dou Ker, Shih-Lun Chen, and Chia-Sheng Tsai
Nanoelectronics and Gigascale Systems Laboratory
Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan

***Abstract*—A new mixed-voltage I/O buffer with a blocking NMOS and a dynamic gate-controlled circuit for high-voltage-tolerant applications is proposed. The new proposed I/O buffer can receive the input signals with the voltage swing twice as high as the normal power supply voltage (VDD), which has been fabricated in a 0.25-μm CMOS process to receive 5-V input signals without suffering gate-oxide reliability and circuit leakage issues. The new proposed mixed-voltage I/O buffer can be easily scaled down toward 0.18-μm (or below) CMOS process to serve different mixed-voltage I/O interfaces, such as 1.8/3.3-V or 1.2/2.5-V applications.**

I. INTRODUCTION

As the semiconductor process is scaled down, the thickness of gate oxide becomes thinner in order to reduce the core power supply voltage (VDD) [1]. However, some peripheral components or other ICs on the circuit boards are still operated at higher voltage level, such as 3.3 V or 5 V. Hence, some chips could be operated at different voltage levels in a microelectronics system. Several problems arise in the interfaces between these ICs, such as the gate-oxide reliability [2], the hot-carrier degradation [3], [4], and the undesired circuit leakage paths [5].

Fig. 1 shows the conventional tri-state I/O buffer in a 0.25-μm CMOS process. The power supply voltage (VDD) in Fig. 1 is 2.5 V. However, in the mixed-voltage interface, the swing of the external input signal at the I/O pad may be from 0 V to 5 V in the receiving mode (tri-state input mode). The gate voltages of the pull-up PMOS and the pull-down NMOS in the conventional I/O buffer are controlled at 2.5 V and 0 V, respectively, by the pre-driver circuit to turn themselves off in the receiving mode. However, when the input signal on the I/O pad rises up to 5 V in the receiving mode, the parasitic drain-to-well pn-junction diode in the pull-up PMOS will be forward biased. Thus, an undesired leakage current path occurs from the I/O pad to the power supply voltage (VDD) through the parasitic pn-junction diode. Besides, because the gate voltage of the pull-up PMOS is biased at 2.5 V and the voltage on the I/O pad is 5 V, the channel of the pull-up PMOS will be turned on in such receiving mode. Therefore, another undesired leakage current path also occurs from the I/O pad to VDD through the channel of the pull-up PMOS. The voltages across the thin gate oxides of the pull-down NMOS and the first input stage (INV) could be too high to cause the gate-oxide reliability problem in such receiving mode with 5-V input signals.

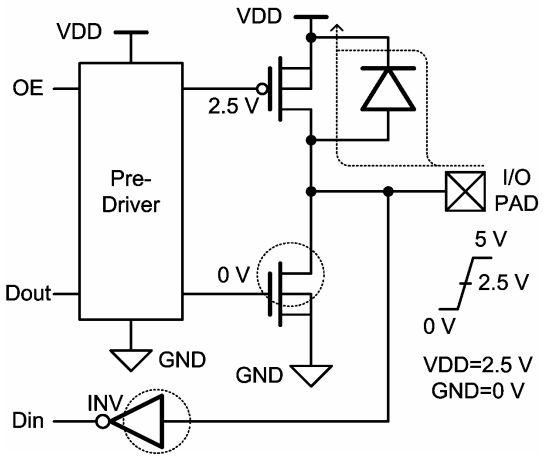

Fig. 1. Conventional tri-state I/O buffer in a 0.25-μm CMOS process.

In order to overcome these problems, several techniques were reported [6]-[11]. The dual-oxide (thin- and thick-oxide thickness) process has been developed to avoid the gate-oxide reliability problem [6]. In order to prevent the undesired leakage current path from the I/O pad to VDD through the parasitic pn-junction diode of the pull-up PMOS, the bulk (n-well) of the pull-up PMOS was connected to an extra pad that provides a higher external bias voltage. Without using the extra high bulk bias voltage, the mixed-voltage I/O buffers, using stacked thin-oxide devices and a dynamic n-well bias circuit, have been reported to receive the high-voltage input signals without gate-oxide reliability issue [7]-[11].

In this paper, a new design of mixed-voltage I/O buffer that can receive the high-voltage input signals by using only low-voltage devices is proposed. A blocking NMOS with

dynamic gate-controlled circuit is connected between the low-voltage I/O buffer and the I/O pad. This new I/O buffer can receive the input signals with the voltage swing twice as high as the normal operating voltage.

II. New Mixed-Voltage I/O Buffer With a Blocking NMOS

Fig. 2 depicts the proposed mixed-voltage I/O buffer with a blocking NMOS and a dynamic gate-controlled circuit in a 0.25-μm CMOS process. In Fig. 2, VDDH has a high voltage of 5 V, which can be generated by the on-chip charge pump circuit [12] or other high-voltage generators. Transistor MN1 is used to protect the conventional I/O buffer from the high-voltage overstress. The operations of the dynamic gate-controlled circuit in the proposed I/O buffer with blocking NMOS are listed in Table I. When the I/O buffer is in the receiving mode (tri-state input mode), the gate terminal (node 2) of MN1 is biased at VDD (2.5 V) by the dynamic gate-controlled circuit, whereas MP0 and MN0 are both turned off by the pre-driver. At this moment, if an input signal of logic 0 (0 V) is received from the I/O pad, node 1 is discharged to 0 V through the transistor MN1, and this input signal can be successfully transferred to the node Din. When a logic 1 (5 V) signal is received at the I/O pad, the gate terminal of transistor MN1 is still biased at 2.5 V, so the voltage on node 1 is pulled to VDD−V_t. In the 0.25-μm CMOS process, the threshold voltage (V_t) of devices is around 0.6 V. Thus, the voltage on node 1 is pulled to around 1.9 V (2.5−0.6=1.9) when this I/O buffer receives an input signal of 5 V. When the voltage on node 1 is 1.9 V, the signal Din has a state of logic 0. A feedback device MP1 is added to restore the voltage level on node 1 to 2.5 V, which avoids the undesired static dc current through the inverter INV. In this design, MN1, MP1, and inverter INV can convert the 5-V input signal to 2.5-V signal successfully. Therefore, MN1 can protect the I/O buffer without suffering high-voltage overstress.

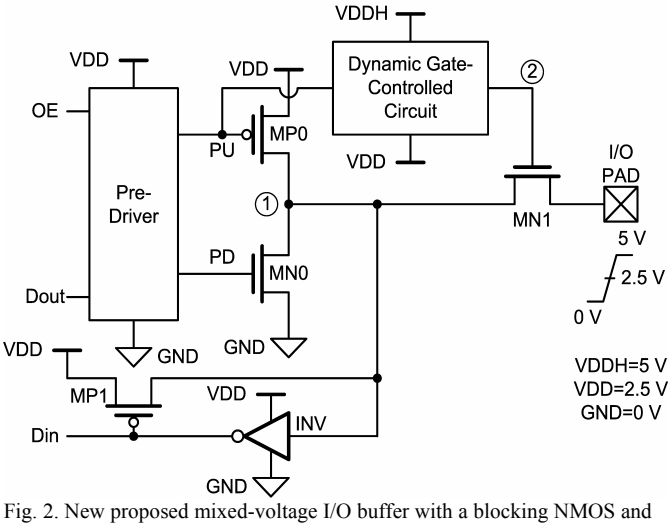

Fig. 2. New proposed mixed-voltage I/O buffer with a blocking NMOS and a dynamic gate-controlled circuit.

TABLE I

Operations of the Dynamic Gate-Controlled Circuit in the Proposed I/O Buffer With Blocking NMOS

Operating Modes	Transmitted signal	Vg of MP0 (PU)	Vg of MN1 (Node 2)
Receiving	X	VDD (2.5 V)	VDD (2.5 V)
Transmitting	Low (0 V)	VDD (2.5 V)	VDD (2.5 V)
Transmitting	High (2.5 V)	GND (0V)	VDDH (5V)

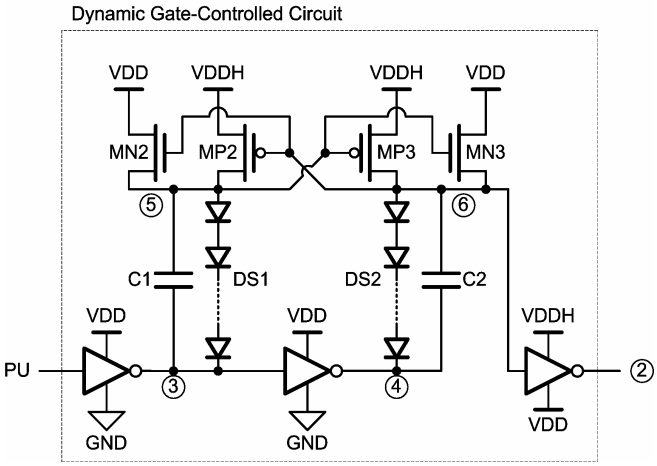

Fig. 3. Circuit implementation of the dynamic gate-controlled circuit in the new proposed mixed-voltage I/O buffer.

Fig. 3 depicts the dynamic gate-controlled circuit of the proposed I/O buffer, where MP2 and MP3 are designed with the cross-coupled structure. If the gate voltage of MP2 (or MP3) is pulled down, this transistor is turned on and pulls up the gate voltage of the other transistor to VDDH to turn it off. For example, if the voltage on node 5 is lower than VDDH−V_{tp} and the voltage on node 6 is VDDH, MN2 is turned on to keep the node 5 at VDD. Capacitors C1 and C2 are used to couple the signals from nodes 3 and 4 to nodes 5 and 6, respectively. The voltages across these capacitors are always 2.5 V, because the voltage levels on the top plate and bottom plate of capacitors C1 and C2 are either 2.5 V and 0 V or 5 V and 2.5 V. With these capacitors, when node 3 converts the voltage level from 2.5 V to 0 V, the voltage on node 5 is pulled down to 2.5 V and then the voltage level on node 6 is pulled up to 5 V by MP3. On the contrary, when the voltage level on node 4 is converted from 2.5 V to 0 V, the voltage on node 6 is pulled down to 2.5 V, and that on node 5 is pulled up to 5 V by MP2.

Initially, the voltages on nodes 3, 4, 5, and 6 could be unknown. If the voltages on nodes 5 and 6 are 5 V and 2.5 V, and the voltages on nodes 3 and 4 are 0 V and 2.5 V, the voltages across capacitors C1 and C2 are 5 V and 0 V, respectively, instead of both 2.5 V. In order to overcome this problem, diode strings DS1 and DS2 are added. The turn-on voltages of the diode strings are designed to a little higher than VDD (2.5 V) by using multiple diodes in stacked configuration. In order to prevent the leakage

current path to the grounded p-type substrate, the diode-connected MOSFET or poly diode [13] is suggested. With these diode strings, if the voltage on node 3 is at 0 V and that on node 4 is at 2.5 V, the voltage on node 5 is clamped at the turn-on voltage (~ 2.5 V) of DS1. Therefore, MP3 is turned on to pull up the voltage on node 6 to 5 V. Thus, the voltages across capacitors C1 and C2 are both 2.5 V.

In the new proposed mixed-voltage I/O buffer, the bulk of the blocking NMOS MN1 can be coupled to 0 V (GND) without any gate-oxide reliability problem, even if the gate voltage of MN1 may be as high as VDDH (5 V). The reason is that this blocking NMOS MN1 is always turned on and the voltage across the gate oxide of MN1 is from the gate to the conducting channel, but not from the gate to its bulk. The gate oxides of all NMOS devices in the dynamic gate-controlled circuit are also safe because these NMOS devices are turned on when their gates are pulled up to VDDH.

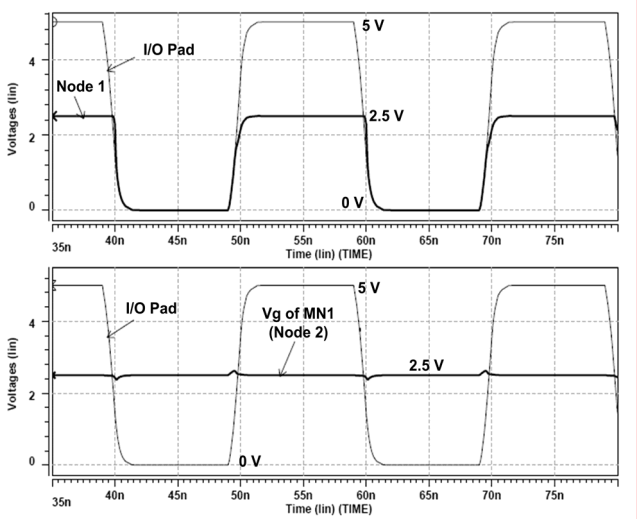

Fig. 4. Simulation waveforms of the new proposed mixed-voltage I/O buffer in the receiving mode with 5-V input signals. (f=50 MHz)

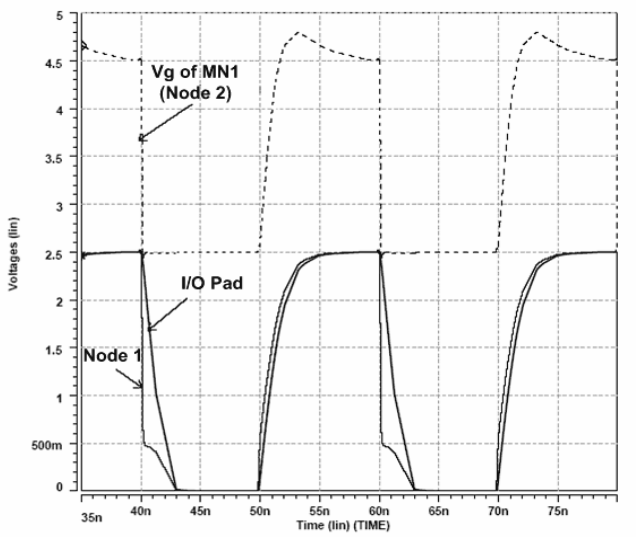

Fig. 5. Simulation waveforms of the new proposed mixed-voltage I/O buffer in the transmitting mode. (f=50 MHz)

The functions of the proposed I/O buffer with a blocking NMOS and a dynamic gate-controlled circuit has been fully verified by SPICE simulation in a 0.25-µm CMOS process. Fig. 4 shows the simulation waveforms of the proposed mixed-voltage I/O buffer in the receiving mode to receive the input signal of 0-to-5 V. As shown in Fig. 4, the gate voltage (node 2) of MN1 is always kept at 2.5 V in the receiving mode, and the voltage swing on node 1 is from 0 V to 2.5 V. Fig. 5 shows the simulation waveforms of the proposed mixed-voltage I/O buffer in the transmitting mode. When the voltage on node 1 is raised up to 2.5 V, the gate voltage of MN1 is also raised to ~5 V at the same time to turn MN1 on. Then, the voltage on the I/O pad is pulled up to 2.5 V. When the voltage on node 1 is dropped to 0 V, the gate voltage of transistor MN1 is kept at 2.5 V to prevent the high-voltage overstress on the gate oxide of the blocking NMOS MN1. The voltage on the I/O pad is therefore dropped to 0 V. With the dynamic gate-controlled circuit, the new proposed mixed-voltage I/O buffer can successfully transfer signals in full swing to the I/O pad through the blocking NMOS MN1.

III. Experimental Results

The new proposed mixed-voltage I/O buffer with a blocking NMOS and a dynamic gate-controlled circuit has been fabricated in a 0.25-µm 2.5-V 1P5M CMOS process with only thin gate oxide. The chip photograph of the new proposed I/O buffer is shown in Fig. 6. Fig. 7 shows the measured voltage waveforms on the node Dout and I/O pad of the new proposed I/O buffer in the transmitting mode. Figs. 8 and 9 show the measured voltage waveforms on the node Din and I/O pad of the new proposed I/O buffer in the receiving mode to receive 2.5-V and 5-V input signals at 100 MHz, respectively. As shown in Figs. 7, 8, and 9, the new proposed I/O buffer can be correctly operated in the 2.5/5-V mixed-voltage interface.

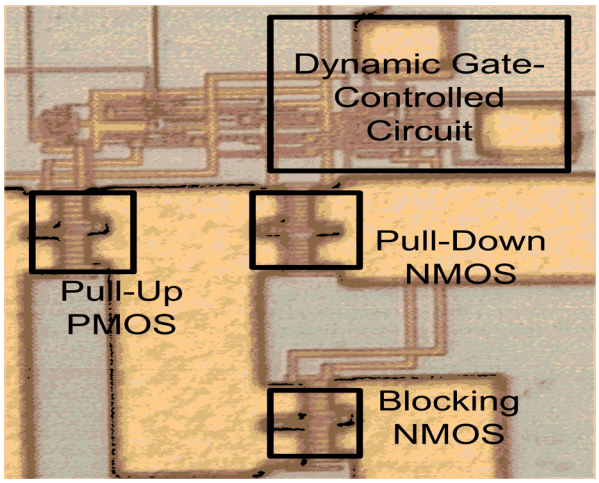

Fig. 6. Chip photograph of the proposed mixed-voltage I/O buffer fabricated in a 0.25-µm 2.5-V 1P5M CMOS process.

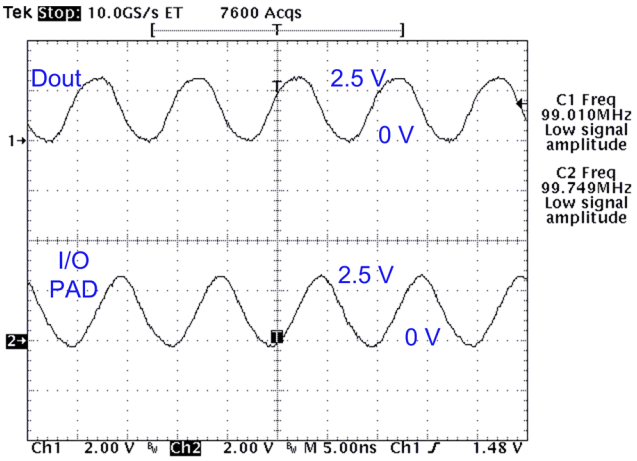

Fig. 7. Measured voltage waveforms of the new proposed mixed-voltage I/O buffer in the transmitting mode with 100-MHz output signals.

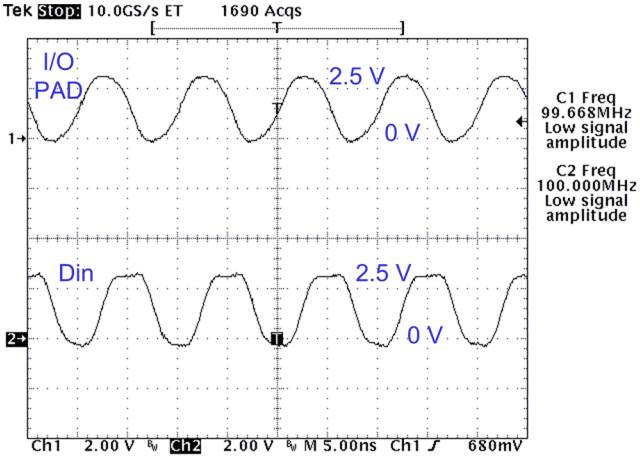

Fig. 8. Measured voltage waveforms of the new proposed mixed-voltage I/O buffer in the receiving mode with 2.5-V 100-MHz input signals.

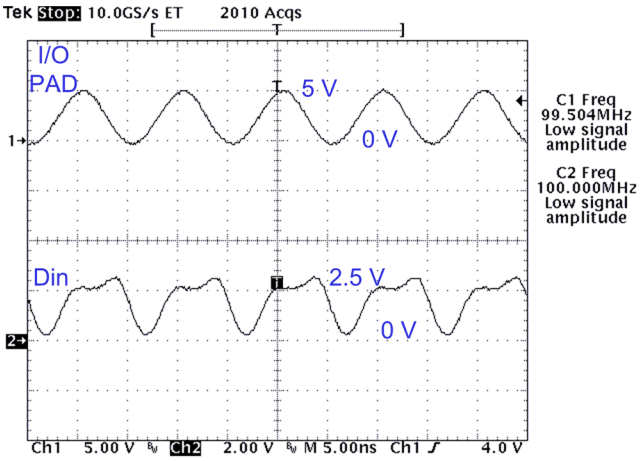

Fig. 9. Measured voltage waveforms of the new proposed mixed-voltage I/O buffer in the receiving mode with 5-V 100-MHz input signals.

IV. Conclusion

A new design of mixed-voltage I/O buffer with a blocking NMOS and a dynamic gate-controlled circuit has been proposed and verified in a 0.25-µm 2.5-V 1P5M CMOS process. The blocking NMOS is applied to protect the I/O buffer without suffering the high-voltage overstress on the thin gate oxide. With the blocking NMOS, this proposed I/O buffer can receive the input signals with the voltage swing twice as high as the normal operating voltage (VDD). The measured results have confirmed that the new mixed-voltage I/O buffer can be correctly operated in the 2.5/5-V mixed-voltage interface without suffering gate-oxide reliability and circuit leakage issues. The proposed I/O buffer can be easily scaled down toward 0.18-µm (or below) CMOS process to serve other mixed-voltage I/O interfaces, such as 1.8/3.3-V or 1.2/2.5-V applications.

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