P-17: On-Panel Design Technique of Threshold Voltage Compensation for Output Buffer in LTPS Technology

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Abstract

A class-B output buffer with threshold voltage (V_{TH}) compensation for the data driver circuit fabricated on liquid crystal display (LCD) panel in low temperature polysilicon (LTPS) technology is proposed. This output buffer can be operated at 50-kHz operation frequency with a 2-to-8 V output swing for extended graphic array (XGA) application. By employing the design technique of threshold voltage compensation, the offset voltage (V_{OS}) of the class-B output buffer under 2-to-8 V input signal can be controlled within ± 100 mV for a high resolution and quality applications in LCD panel.

1. Introduction

LTPS thin-film transistor (TFT) devices have been widely used in active matrix liquid crystal display (AMLCD), because the electron mobility of the LTPS TFT device is about 100-times larger than that of the conventional amorphous silicon (α-Si) TFT device [1]. Many small to mid-size LTPS TFT AMLCDs with integrated driver circuits have been used in portable system, such as mobile phone, digital camera, notebook, and so on. Consequently, LTPS technology is progressing toward system-on-panel (SOP) application, which is expected to integrate all control circuits and driver circuits on the glass substrate in the near future.

The LCD driver contains shifter registers, level shifter, digital-to-analog converter (DAC), and output buffer. The output buffer is a critical issue to achieve the low power dissipation, high resolution, high speed, and large output swing on LCD panel. In CMOS technology, the output buffer for LCD driving application has been studied [2]-[6]. Since the device aging and the fabrication processes cause the threshold voltage variations on the characteristics of LTPS TFT devices [7], [8], the output circuit fabricated on panel more easily suffers from an offset voltage due to the devices mismatch in differential pair stages. When the same gray levels transmit to the different pixels through data driving buffer with large offset voltage, the brightness of the pixels will be different. If the offset voltage caused by the threshold voltage variation among LTPS TFT devices can be reduced, the data driver can be promisingly integrated on glass in LTPS technology.

In this work, a class-B output buffer with threshold voltage compensation for the integrated data driver circuit fabricated on LCD panel is proposed. The threshold voltage compensation method employed on output buffer can reduce the offset voltage for high resolution applications.

2. Circuits Implementation

2.1 LTPS Process and V_{TH} Variation

In the LTPS process, a buffer oxide and an α-Si:H film were deposited on glass substrate and then XeCl excimer laser was used to crystallize this α-Si film. After active islands were defined, the ion doping was carried out. Following, the double gate insulator layer films were deposited and then the gate-metal was deposited and patterned. After all ion doping processes were completed, the doping activation was performed by rapid thermal annealing (RTA). Moreover, hydrogenation was used to improve the device performance. The output buffer circuits, including N-type and P-type TFT devices, are fabricated after contact holes and metal lines formations.

The variation on threshold voltage (V_{TH}) of 120 LTPS N-type TFT devices in different locations of a LTPS panel is shown in Fig. 1. The V_{TH} of the on-panel N-type device with a channel length of 3 μm is extracted by extrapolation of the I_{DS}-V_{GS} curve from the point of the maximum transconductance (G_{mmax}) in the linear regime (V_{DS} = 0.1 V). In this 3-μm LTPS technology, the threshold voltages of these N-type TFT devices in different panel locations vary from 0.75 V to 2.15 V, whose variation is quite large compared with CMOS technology. The inserted figure in Fig. 1 indicates a differential amplifier with the offset voltage (V_{OS}) caused by the mismatch of input devices. The offset voltage of this differential amplifier can be written as

$$\begin{aligned} V_{OS} &= V_{OS,P}\,(g_{mP}/g_{mN}) + V_{OS,N} \\ &= \{(|V_{GS}-V_{TH,P}|)/2]\,[\Delta(W/L)/(W/L)]_P + \Delta V_{TH,P}\}\,(g_{mP}/g_{mN}) \\ &\quad + [(V_{GS}-V_{TH,N})/2]\,[\Delta(W/L)/(W/L)]_N + \Delta V_{TH,N} \end{aligned} \quad (1)$$

where the Δ(W/L)/(W/L) is the dimension variation, and $V_{OS,N}$ and $V_{OS,P}$ are the offset voltages caused by the mismatch of the input N-type and P-type TFT devices, respectively.

The offset voltage of differential amplifier will be dominated by the V_{TH} variation of input devices. Therefore, when these LTPS TFT devices with large V_{TH} variation are used in operational amplifier, the offset voltage of this buffer will be increased to affect the gray level of unit pixel.

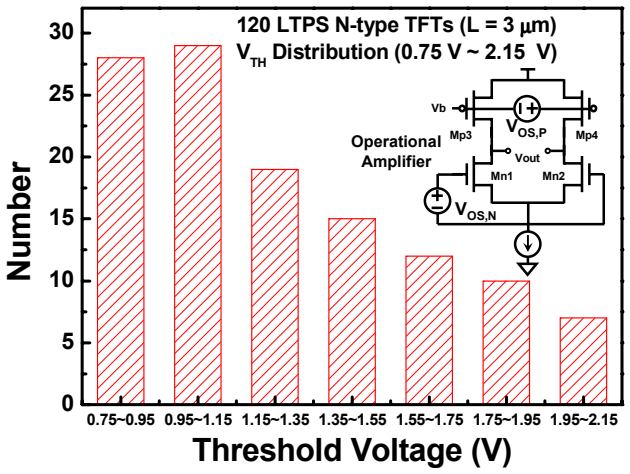

Fig. 1. The threshold voltage (V_{TH}) variation on N-type TFT devices in different locations of a LTPS panel. The inserted figure shows a differential amplifier with offset voltage.

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2.2 Class-B Output Buffer

The circuit diagram of the class-B output buffer is shown in Fig. 2. As a unit-gain output buffer, the output node (out) is connected to the inverting input node (in-) and the input signal is applied to the non-inverting node (in+). This class-B output buffer contains a differential input stage (M2-M6), two comparators (M7-M8 and M9-M10), and a push-pull output stage (M11-M12). The differential pairs (M3-M4) realized with N-type TFT devices are biased by the diode-connected constant current source M1.

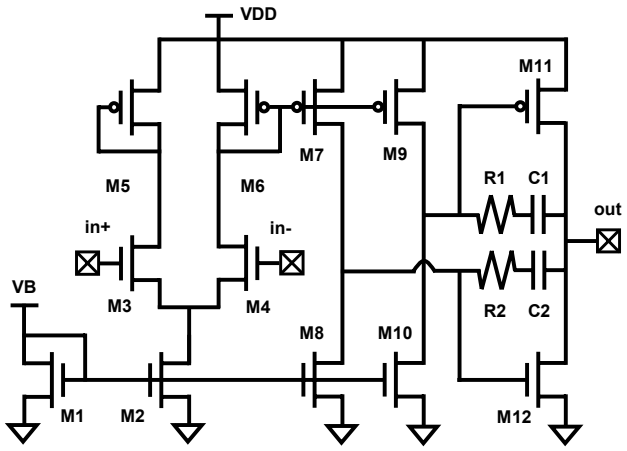

Fig. 2. The class-B output buffer.

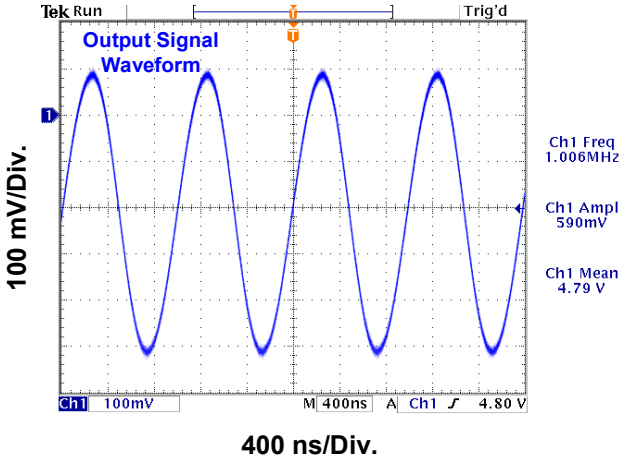

Fig. 3. The measured results of class-B output buffer under 1-MHz sine wave with a 5-V common voltage.

The comparators can sense the input signal to turn on or to turn off the push-pull transistors (M11-M12) to amplify the voltage difference of two input nodes. The device dimensions (W/L) of M5, M6, M7, and M9 are drawn the same. The device dimension of M8 is chosen to be a little larger than half of M2, but that of M10 is chosen to be a little smaller than half of M4.

$$(W/L)_8 = 1/2\ (W/L)_2 + \Delta(W/L)_{designed} \quad (2)$$

$$(W/L)_{10} = 1/2\ (W/L)_2 - \Delta(W/L)_{designed} \quad (3)$$

Since the $(W/L)_8$ is designed to be a little greater than half of $(W/L)_2$, it makes M8 operate in the triode region. Therefore, the gate voltage of M12 will be forced near to the value of GND. Similarly, M9 will be in the triode region to make the gate voltage of M11 be forced near to the value of VDD. That is why M11 and M12 are almost cut off when no signal is applied on the two input nodes (in+ and in-). Since M11 and M12 are almost "off" at the stable state, the power consumption is low while the operational speed of the buffer maintain relatively high. The output waveform of the class-B output buffer fabricated on LTPS panel is shown in Fig. 3. The VB is set to 1 V to provide a constant current source for this buffer. The total power consumption of this buffer is 6.7 mW under VDD of 10 V, expect the constant current source. The fabricated class-B output buffer can be operated at least 1 MHz, and it has an offset voltage of 200 mV under input common-mode voltage of 5 V.

2.3 Output Buffer With V_{TH} Compensation

In order to reduce the offset voltage (V_{OS}), the on-panel class-B output buffer with threshold voltage compensation is proposed in Fig. 4. As a unit-gain output buffer, the output node is connected to the inverting input node and the input signal is applied to the non-inverting node. The output node of the unity-gain buffer is also connected to an RC ladder output loading for simulation of driving condition on LCD panel [9]. The voltage swing of input signal (Vin) applied to the input node is 2 V to 8 V. The different amplitudes of input signals (Vin) indicate different gray levels of the pixel. The operation frequency of input signal in this class-B output buffer is 50 kHz for XGA application. Here, the operation frequency of input signal is defined as the frequency of every driving datum transferring into the output buffer.

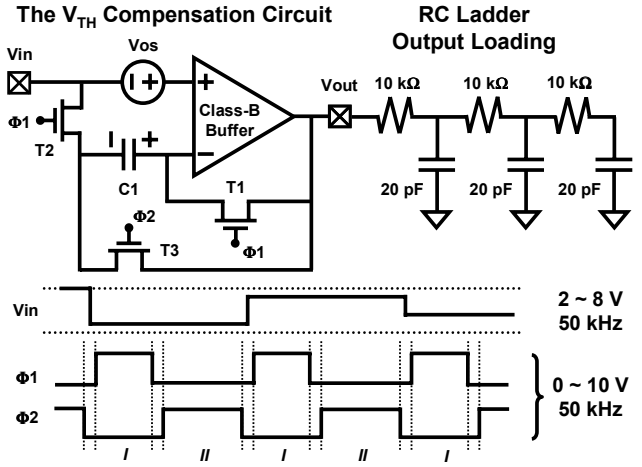

Fig. 4. The circuit and the signal-timing diagram of the proposed class-B output buffer with the threshold voltage compensation to drive an RC ladder output loading.

The threshold voltage compensation circuit contains three switch transistors (T1, T2, and T3) and one offset-holding capacitor (C1). The Φ1 and Φ2 are two complementary signals with amplitudes of 0 to 10 V used to control the gates of T1, T2, and T3. The frequency of these two complementary signals, Φ1 and Φ2, is designed to 50 kHz. Besides, the duty cycle of Φ1 is set 49 % to have a 100-ns non-overlapping period on Φ2, which can avoid three switch transistors being turned on at the same time during their switching period.

The operation sequence of the proposed threshold voltage compensation circuit is described in the following. During the

period I, the voltage level of Φ1 is 10 V to turn on T1 and T2, and the voltage level of Φ2 is 0 V to turn off T3. The offset voltage of buffer, which is the voltage difference between output and input signals ($V_{OS}(I)$ = Vin(I) – Vout(I)), can be detected through the paths of T1 and T2 during the period I. Then, the offset voltage of buffer is pre-stored in C1 ($V_C(I) = V_{OS}(I)$). During the period II, the voltage level of Φ1 is 0 V and the voltage level of Φ2 is 10 V. The paths of T1 and T2 are broken, and the path of T3 is shorted to the inverting input node (in-) through C1, respectively. The detected offset voltage of buffer pre-stored in C1 during the period I ($V_{OS}(I)$) is added to the input node through T3. Then, the output voltage in the period II can be written as

$$\text{Vout(II)} = \text{Vin(II)} + [V_{OS}(II) - V_{OS}(I)] \quad (4)$$

where the $V_{OS}(II)$ is the offset voltage of buffer during the period II. Because the offset voltages of buffer during the period I and the period II, $V_{OS}(I)$ and $V_{OS}(II)$, are almost the same, they can be almost canceled with each other. Therefore, the output voltage can be approached to input voltage, as identical as possible.

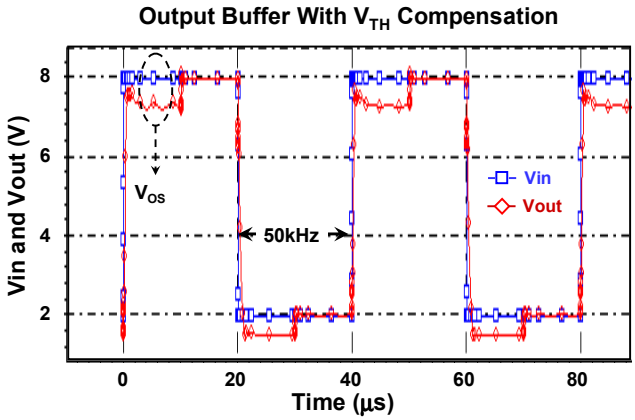

Fig. 5. The simulated output waveform of the proposed class-B output buffers with threshold voltage compensation to drive an RC ladder output loading under 50-kHz square input wave with a swing of 2 V to 8 V.

The simulated output waveform of the proposed class-B output with threshold voltage compensation is shown in Fig. 5. One of the input LTPS N-type TFT device is set with a large threshold voltage shifting of 0.6 V in the simulation. The input node of this buffer is applied by a 2-to-8 V square wave with an operation frequency of 50 kHz for XGA application. Two complementary signals, Φ1 and Φ2, with a frequency of 50 kHz are also applied on the gates of three switch transistors, T1, T2, and T3. In the 0-to-10 µs duration, a signal with amplitude of 8 V is applied on input node, and then the output presents an offset voltage V_{OS} of this buffer. However, in the 10-to-20 µs duration, the offset voltage of this buffer can be compensated. The threshold voltage compensation circuit can cancel the offset voltage of unity-gain buffer through these two durations.

3. Circuits Implementation

The proposed class-B output buffer with threshold voltage compensation has been designed and fabricated in a 3-µm LTPS technology. The photograph of this buffer on glass substrate is shown in Fig. 6. There are seven pads in this test panel, including VB, Vin, VDD, GND, Vout, Φ1, and Φ2. The VDD is set to 10 V and VB is set to 1 V. All results were measured on panel by using probe station in this work.

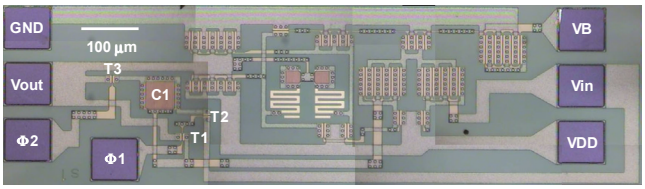

Fig. 6. The photograph of the proposed class-B output buffer with threshold voltage compensation.

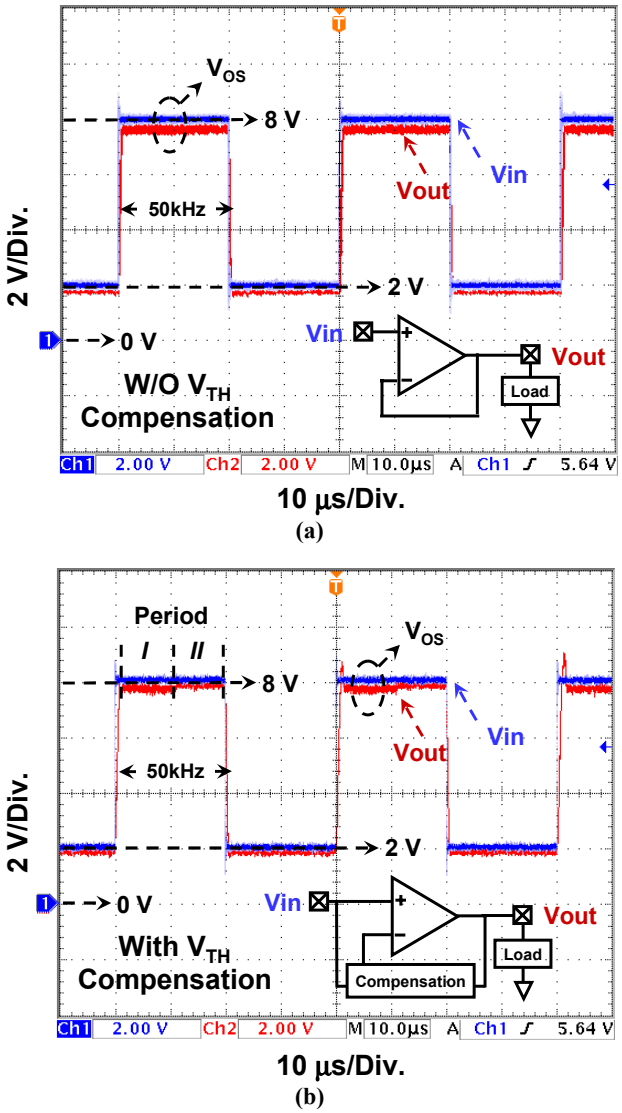

Fig. 7. The measured results of the class-B output buffers (a) without, and (b) with, threshold voltage compensation to drive an RC ladder output loading under 50-kHz square input wave with a swing of 2 V to 8 V.

The function of threshold voltage compensation circuit is verified by the measured waveforms. The measured output waveforms of class-B output buffers without and with threshold voltage compensation are

shown in Figs. 7(a) and 7(b), respectively. The buffer without threshold voltage compensation has an apparent offset voltage of ~ 200 mV on the output pad when the 8-V input signal is applied on the input pad, as shown in Fig. 7(a). During the period I, the buffer with threshold voltage compensation has the same offset voltage as that without threshold voltage compensation dose. However, the offset voltage of this buffer can be canceled by threshold voltage compensation circuit during the period II, as shown in Fig. 7(b), which is consistent to previous simulated waveform.

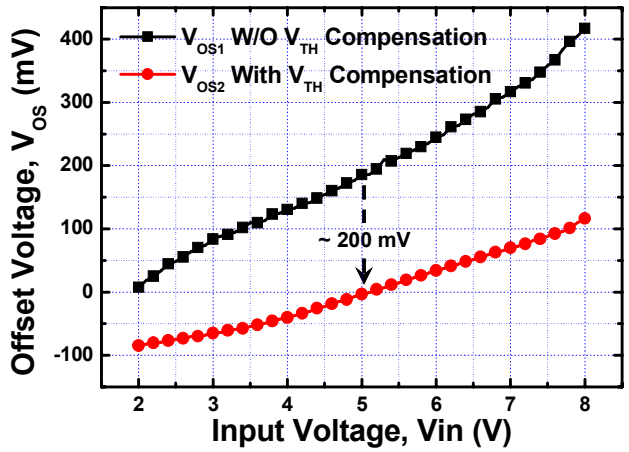

Fig. 8. The offset voltages of the class-B output buffers without and with threshold voltage compensation to drive an RC ladder output loading under different input signal levels.

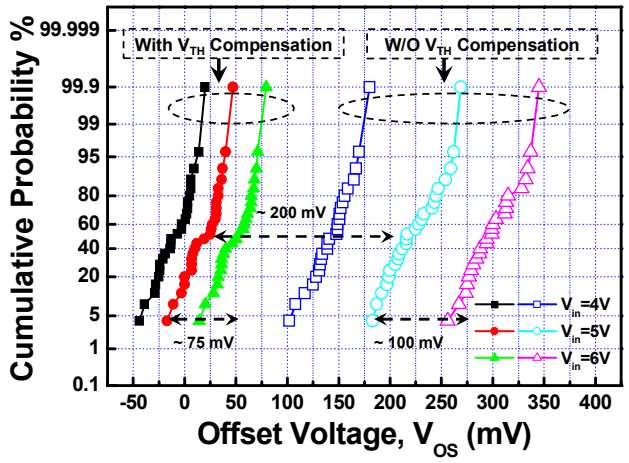

Fig. 9. The variation on offset voltages of the class-B output buffers without and with threshold voltage compensation to drive an RC ladder output loading on panel.

The offset voltages of class-B output buffers without and with threshold voltage compensation measured by HP4156B under different input voltage levels from 2 V to 8 V are shown in Fig. 8. When a 5-V signal is applied on the input pad, the offset voltages of buffer with threshold voltage compensation can be decreased from ~ 200 mV to ~ 0 V. The higher input voltage has a higher offset voltage of buffer because the transconductance of TFT device on the non-inverting node is increased. The threshold voltage compensation circuit in the output buffer can successfully cancel the offset voltage, especially on the large input voltage level. By the way, the slope of offset voltage of buffer without threshold voltage compensation has about twice higher than that with threshold voltage compensation. The variation on offset voltage of the class-B output buffers without and with threshold voltage compensation in different locations on a LTPS panel is shown in Fig. 9. Total number of the measured buffers is 25. The variation of offset voltages in different locations can be reduced from ~ 100 mV to ~ 75 mV (reduced 25 %) by the threshold voltage compensation during different input voltages applied to the buffer. By employing the threshold voltage compensation method, the offset voltage of the buffer and its variation on panel location can be successfully reduced.

4. Conclusion

A class-B output buffer with threshold voltage compensation in LTPS technology has been proposed and verified. By using the threshold voltage compensation circuit, the offset voltage of output buffer can be detected during the period I, and it can be canceled during the period II. The offset voltage can be reduced and controlled within ± 100 mV under input voltage from 2 V to 8 V. The variation on offset voltages of the output buffers at different panel locations can be reduced 25 %. Therefore, the class-B buffer with threshold voltage compensation can be used in the on-panel data driver circuit to provide a high resolution and quality display.

5. Acknowledgment

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6. References

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