Investigation on ESD Robustness of P-type TFTs under Different Layout Structures in LTPS Process for On-Panel ESD Protection Design*

Authors: Ming-Dou Ker [1], Jie-Yao Chuang [1], Chih-Kang Deng [1], Chun-Huai Li [2], and Chung-Hong Kuo [2]

[1] National Chiao-Tung University, Hsinchu, Taiwan.
mdker@ieee.org

[2] AU Optronics Corporation, Science-Based Industrial Park, Hsinchu, Taiwan.

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Biography of Presenter

The Presenter, Ming-Dou Ker, is now a Full Professor in National Chiao-Tung University, Hsinchu, Taiwan.

His current research topics include reliability and quality design for nanoelectronics and gigascale systems, high-speed and mixed-voltage I/O interface circuits, and on-glass circuits for system-on-panel applications in TFT LCD display.

With outstanding achievements in reliability and quality design for circuits and systems, he has been selected as one of the *Distinguished Lecturers* in IEEE Circuits and Systems Society.

Abstract

- System-on-panel (SOP) application has been a major trend for panel development with Low Temperature Poly-Si (LTPS) TFT devices. When more circuits integrated into display panels, the on-panel ESD protection design should be provided against ESD stress to improve reliability and yield of panel manufacturing and assembly.
- P-TFTs have been demonstrated to be more cost-effective than the N-TFTs in the LTPS process with less variation on device characteristics. In this work, ESD robustness of P-TFTs with different layout structures are investigated by measuring secondary breakdown current (It2) with Transmission-Line-Pulsing (TLP) system.

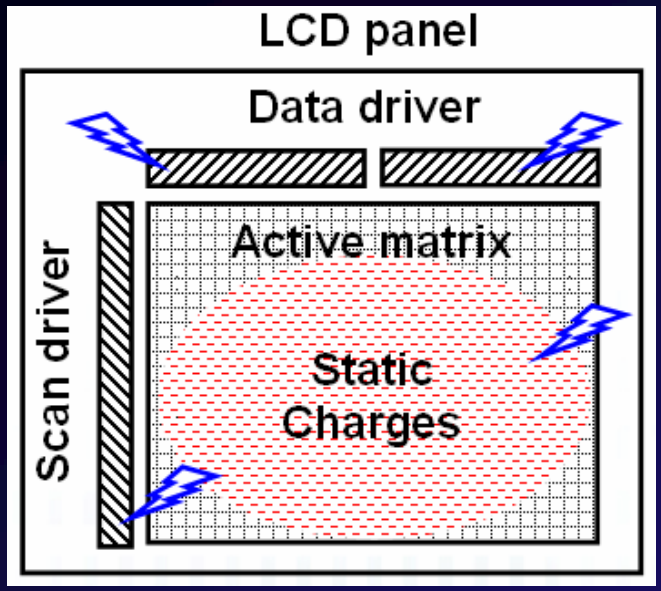
Purpose of This Work

The heat generated by ESD current cannot be dissipated easily on glass substrate, as comparing with Si substrate.

➔ cause damage on panel and lower production yield.

	Material	Thermal Conductance (W/cm-K)
CMOS	Si	1.48
LCD	α-Si	0.018274
	SiOx	0.01
	SiNx	0.0187

Ref.: N. T. Golo *et al.*, "Zapping thin film transistor," *Microelectronics Reliability*, vol. 42, pp. 747-765 (2002).



➡ To develop a good ESD protection design for LCD panel.

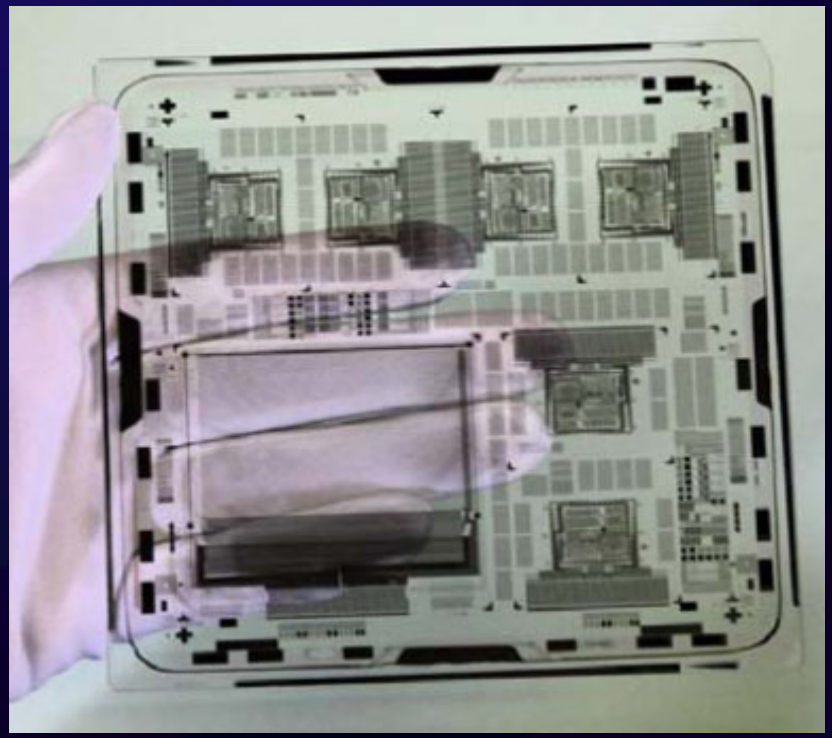
Outline

- Introduction
- Test structures of on-glass P-TFT devices
- Configuration of TLP (Transmission Line Pulsing) system for on-panel devices
- Experimental results
- On-Panel ESD Protection Design With Power Clamp
- Conclusions

System on Panel in LTPS TFT Process

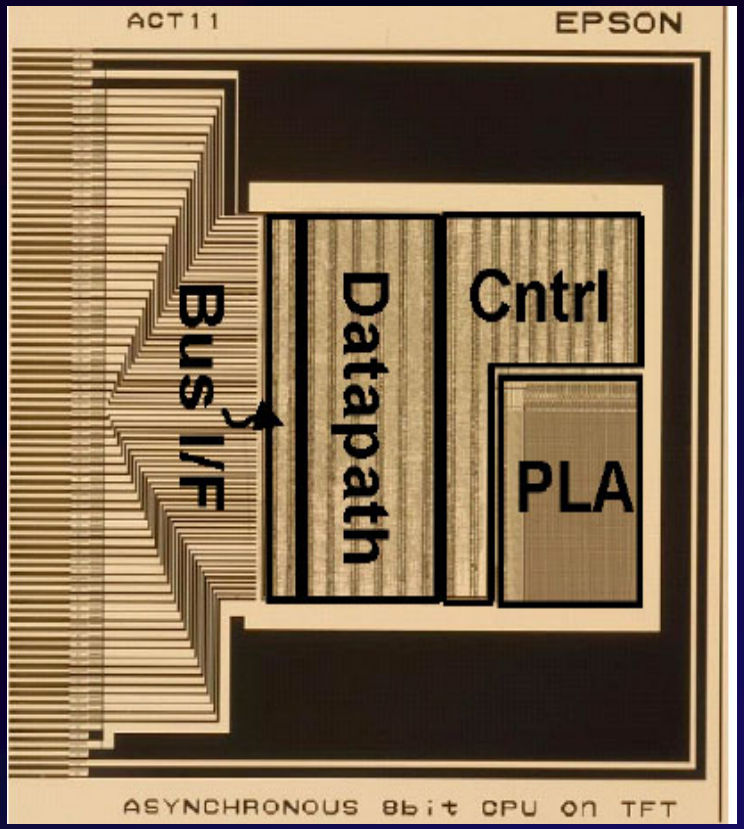
CPU on Glass Substrate

3-MHz Z80 CPU (8 bits)



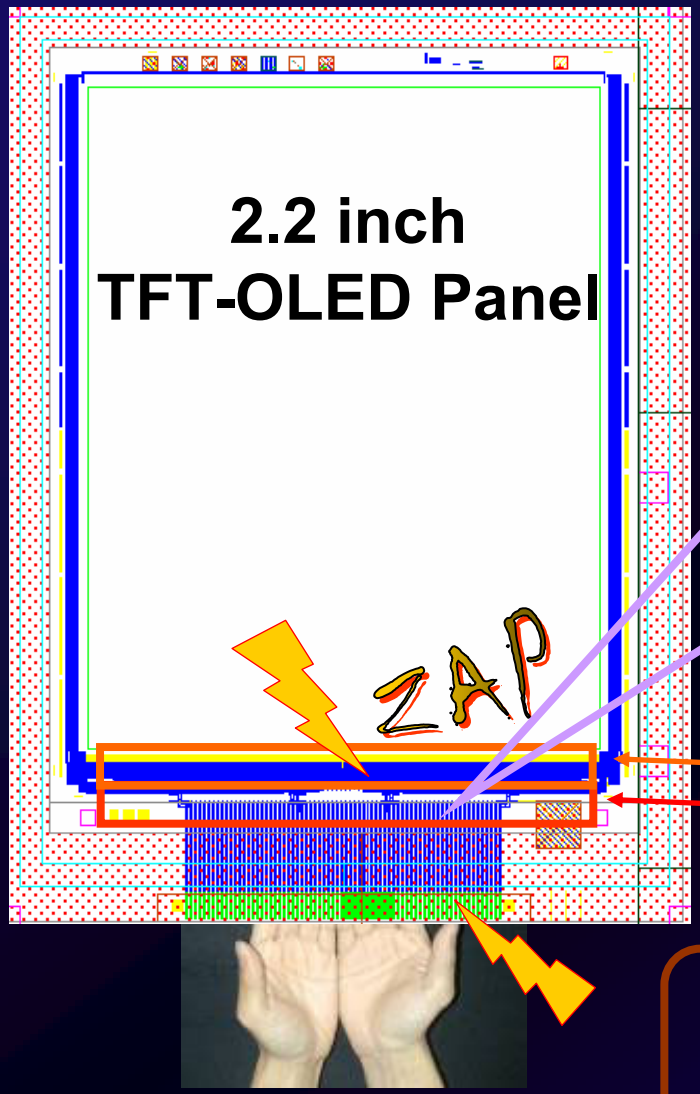
Ref.: B. Lee *et al.*, "A CPU on a glass substrate using CG-silicon TFTs," *ISSCC* 2003. (Sharp)

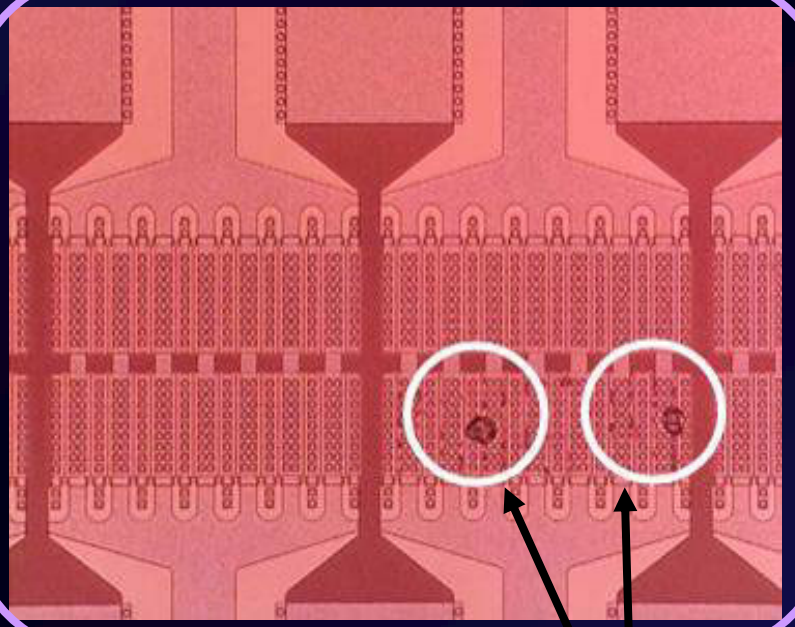
Asynchronous Microprocessor (8 bits) with 80 I/O Pins



Ref.: N. Karaki *et al.*, "A flexible 8b asynchronous microprocessor based on low-temperature poly-silicon TFT technology TFTs," *ISSCC* 2005. (Seiko Epson)

ESD Events to On-Panel TFT Circuits





Shift Register / Switches

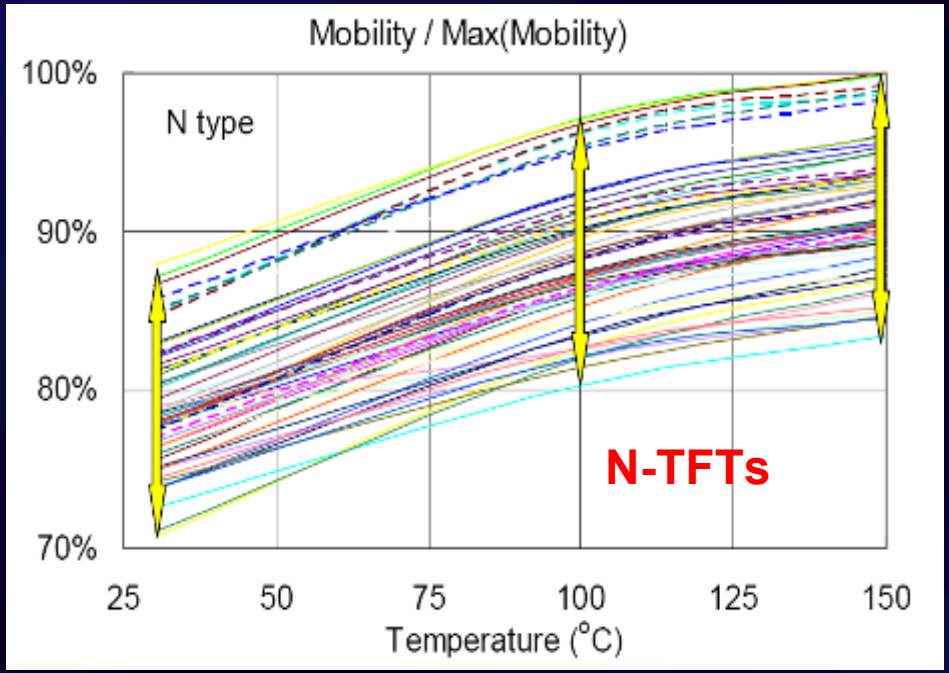
ESD Protection circuits

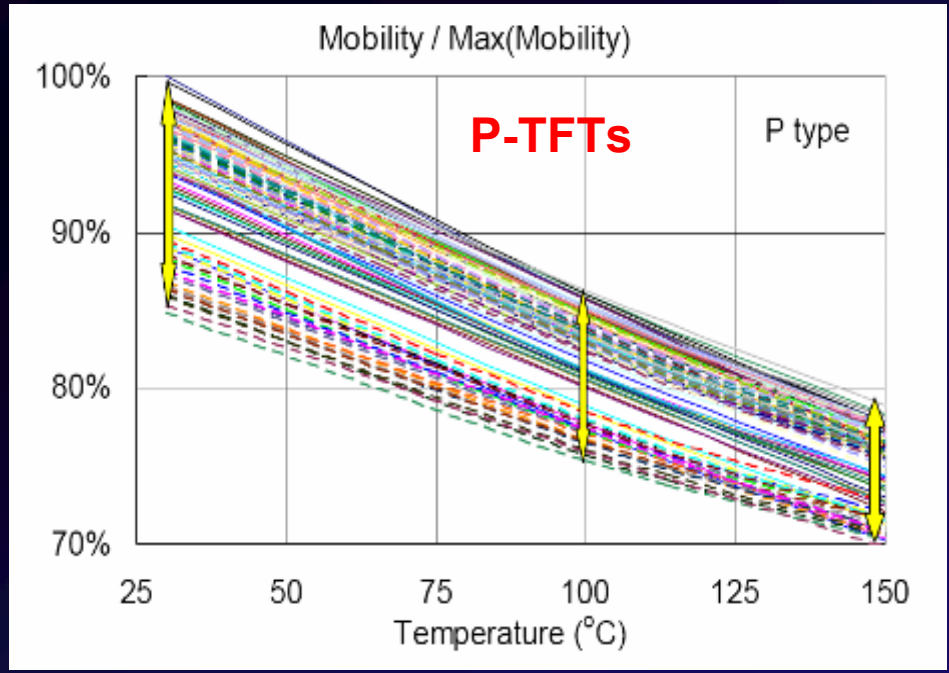
ESD damages

The more TFT circuits integrated on a panel, the more ESD protection should be provided.

Design Consideration of On-Panel TFT Circuits in LTPS Technology

- **P-TFTs** have been found to be more **cost-effective** than the **N-TFTs** in the LTPS process, as well as the **variation** on device characteristics among N-TFT devices is more **serious** than that of P-TFT devices.

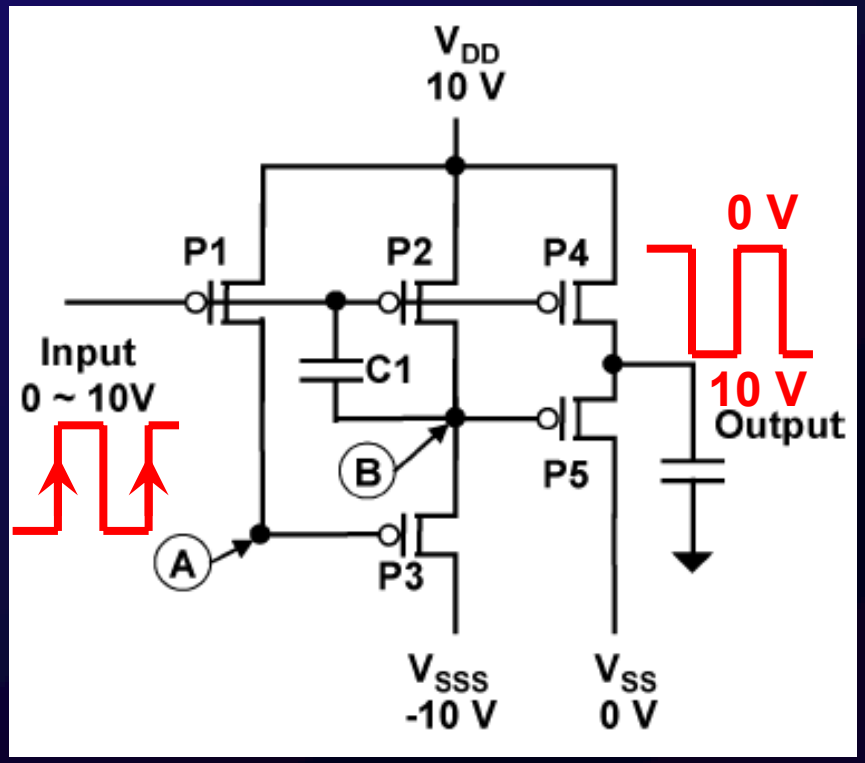




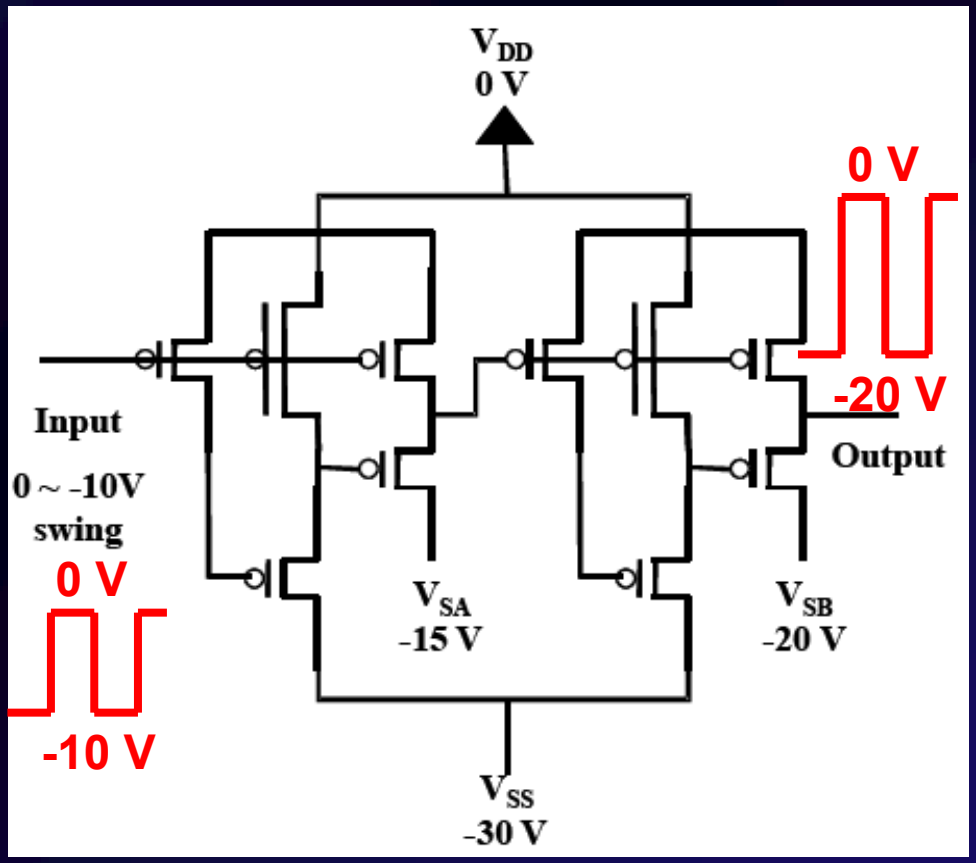
Ref.: Y. H. Tai, "Device Variation and Its Influences on the LTPS TFT Circuits, " *International TFT Conference* (2005).

Circuits Realized with Only P-TFT Devices

Inverter with only P-TFTs

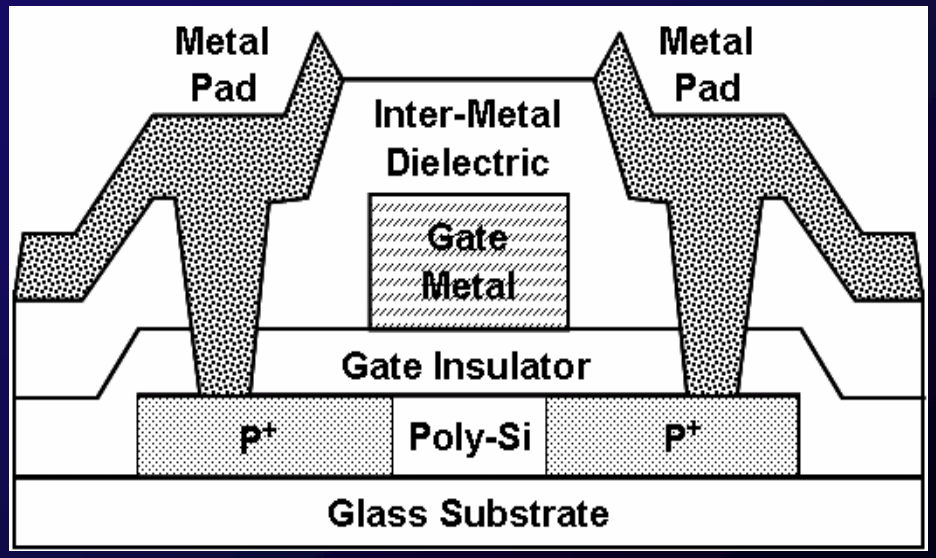


Level Shifter with only P-TFTs



Ref.: S.-H. Jung et al., "A new low power PMOS poly-Si inverter and driving circuits for active matrix displays," in *SID Tech. Dig.*, 2003, pp. 1396-1399.
S.-H. Jung et al., "A new low-power PMOS poly-Si inverter for AMDs," *IEEE Electron Device Lett.*, vol. 25, pp. 23-25, Jan. 2005.

P-TFT Device Structure in a LTPS Process

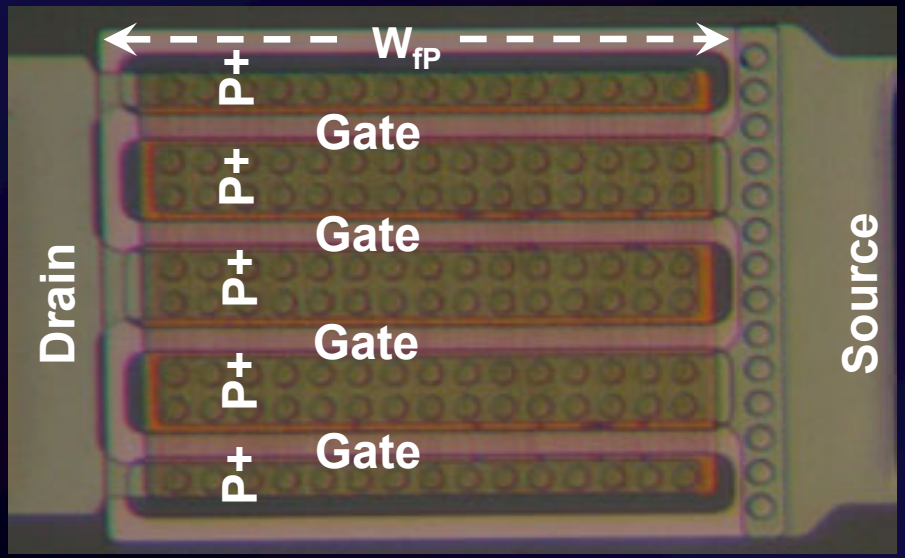


Split Conditions:

(1) Channel length: L = 5 ~ 20 μm

(2) Channel width: W = 100 ~ 500 μm

(3) Fixed W/L ratio but different device dimensions

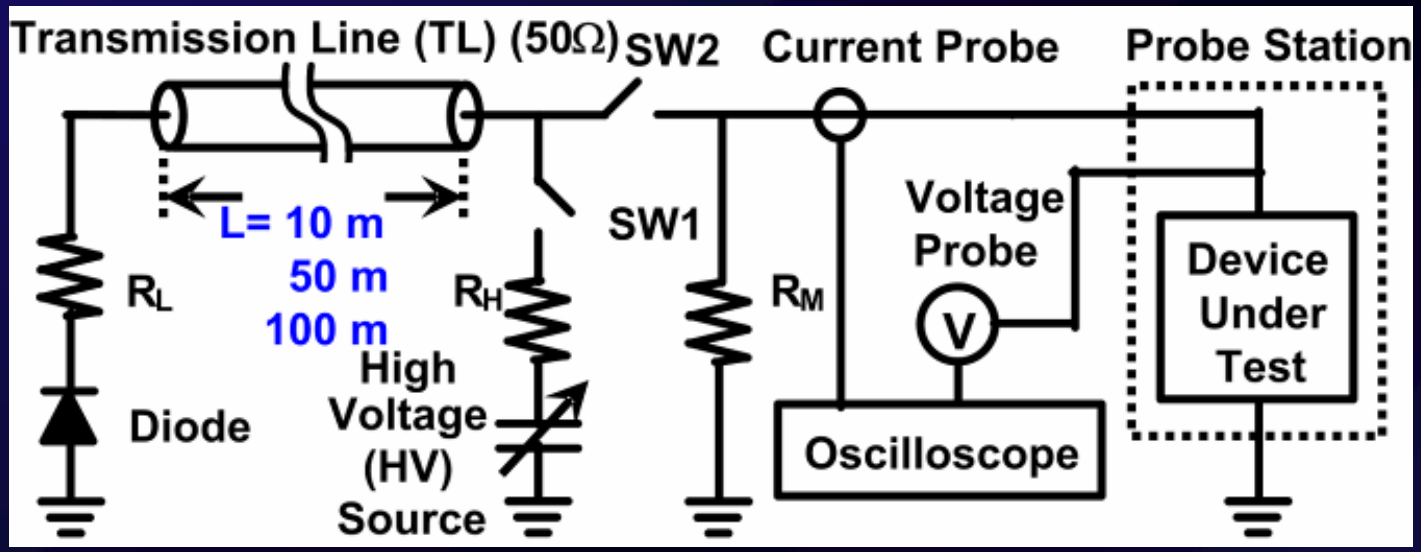


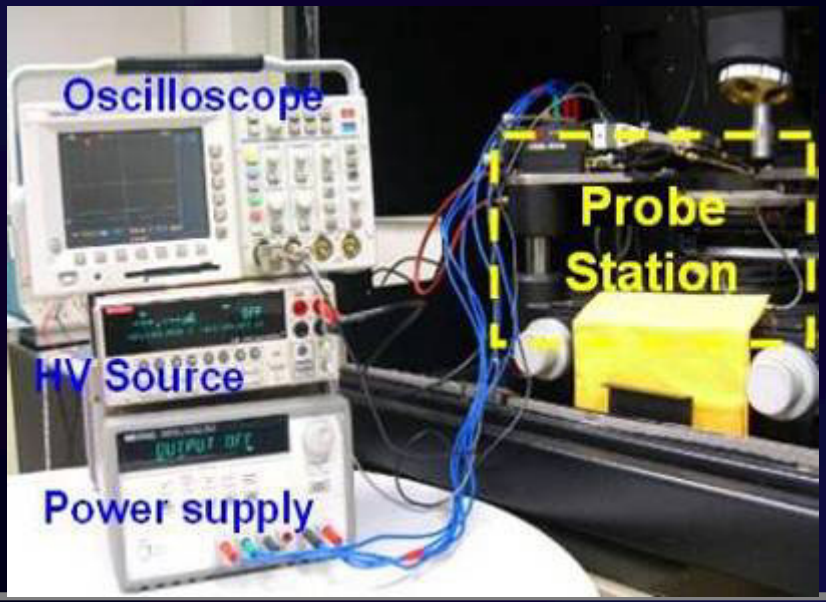
Unit finger Width: W_{fP}

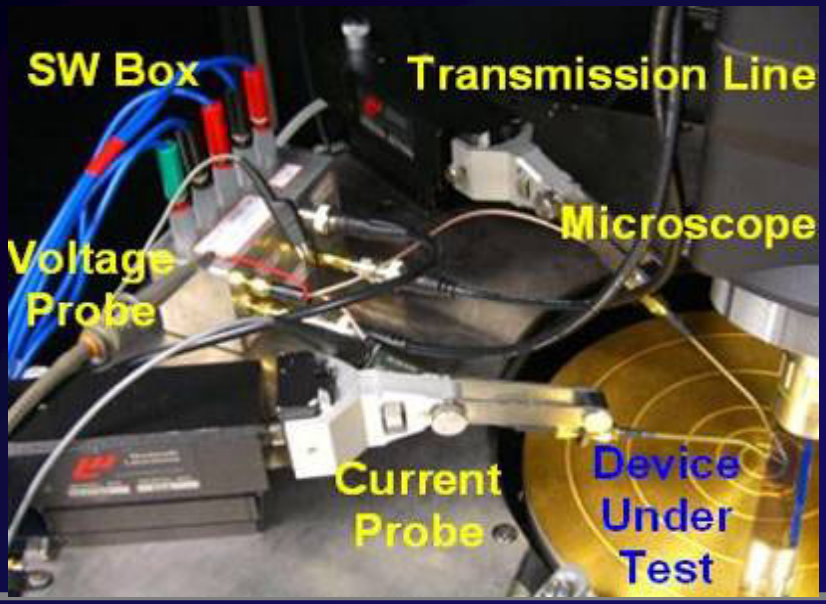
Finger number: N_{fP} = 4 (fixed)

Total width: $W = W_{fP} \times N_{fP}$

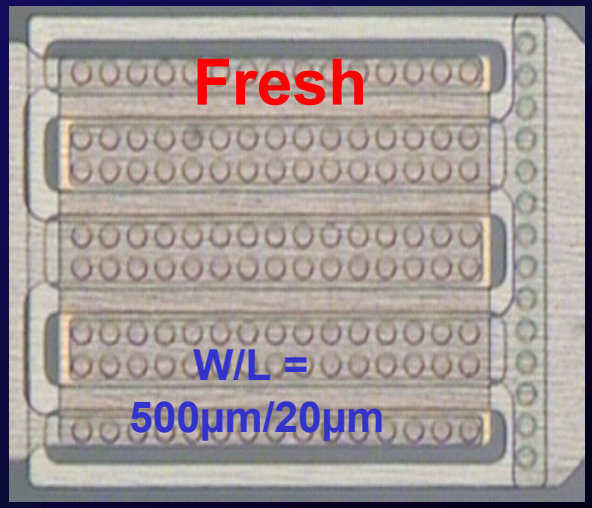
Wafer-Level TLP System with Different Current Pulse Widths (100ns, 500ns, 1000ns)

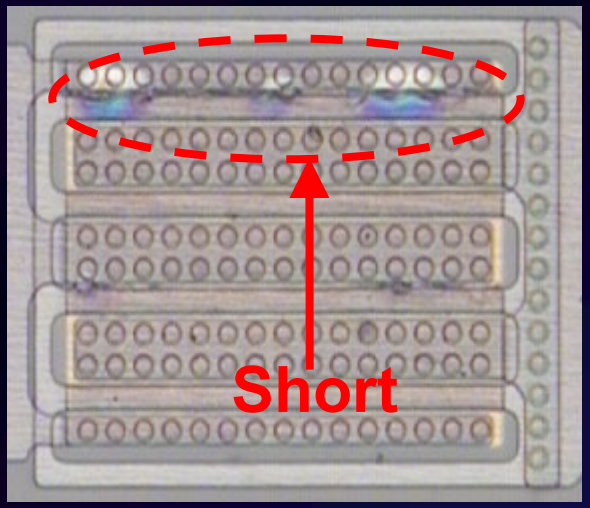


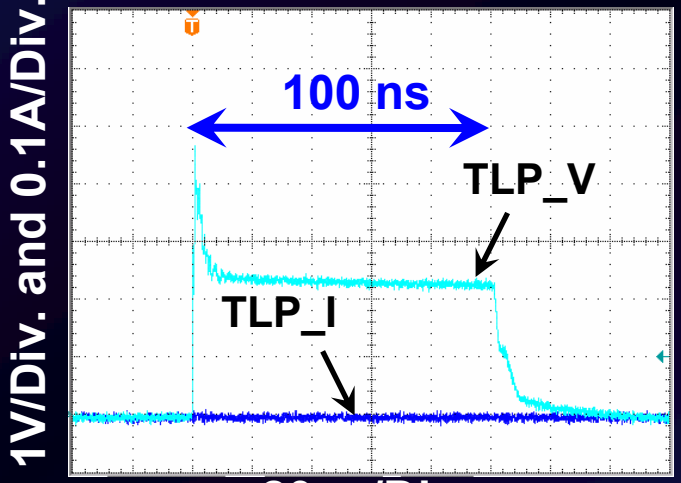


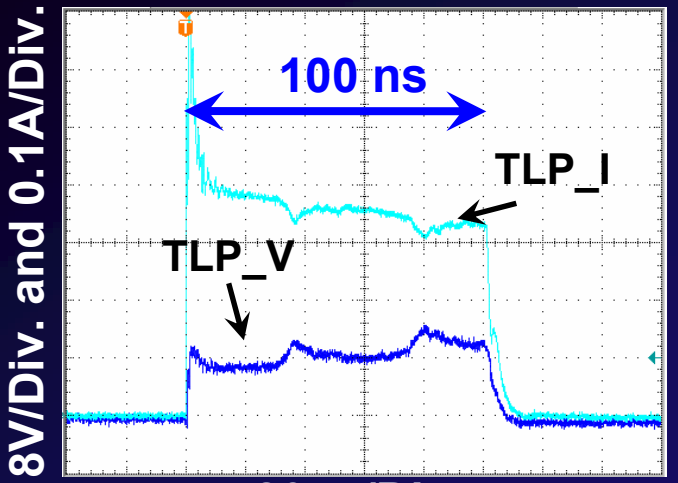


P-TFT under TLP Stress With 100-ns Current Pulse

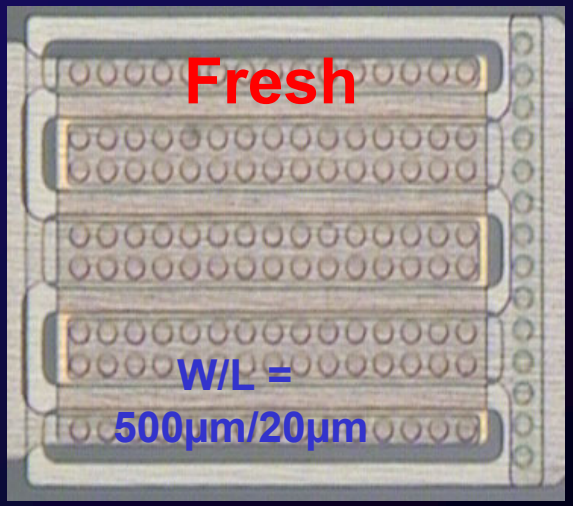


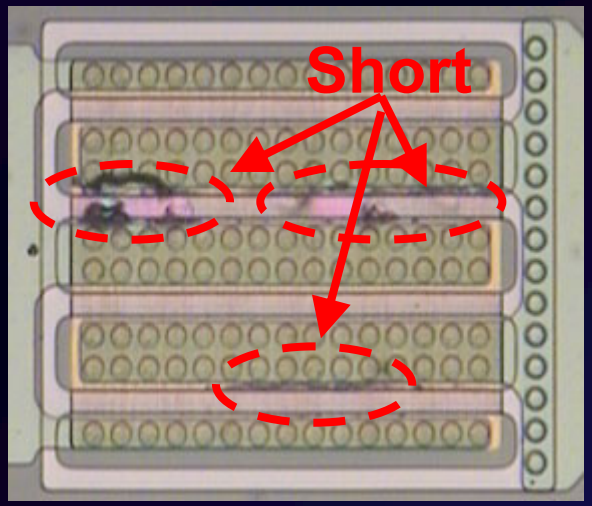


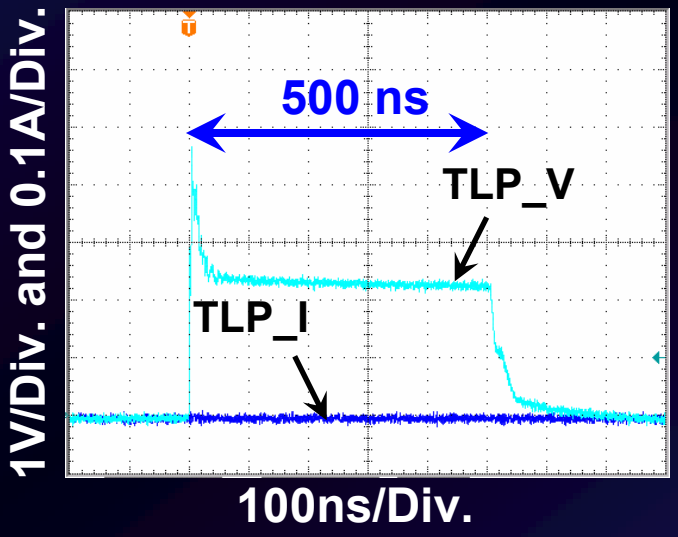


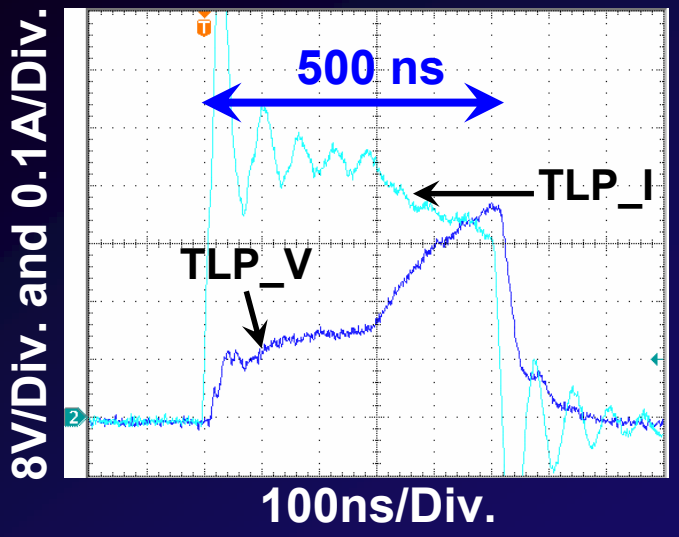


P-TFT under TLP Stress With 500-ns Current Pulse

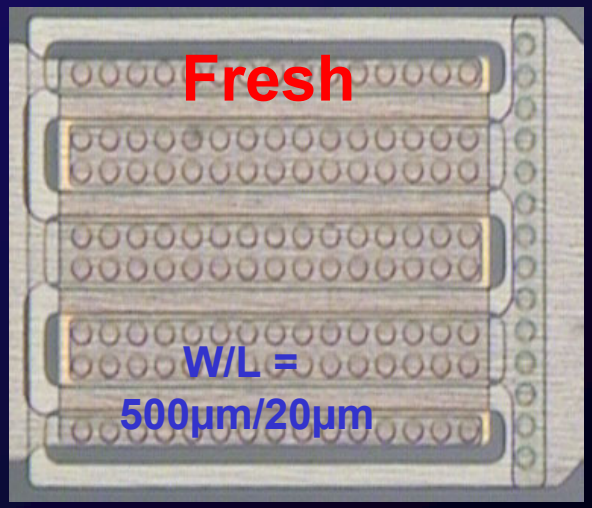


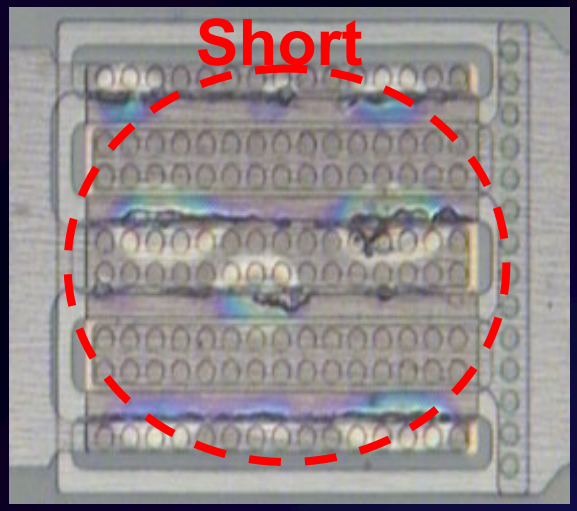


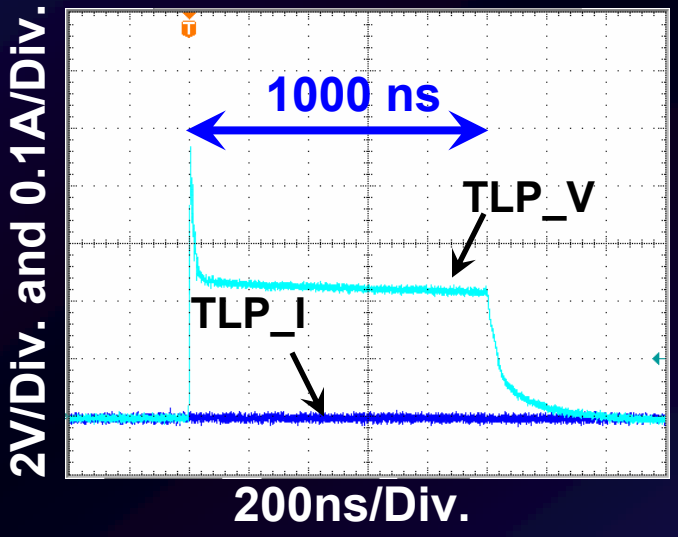


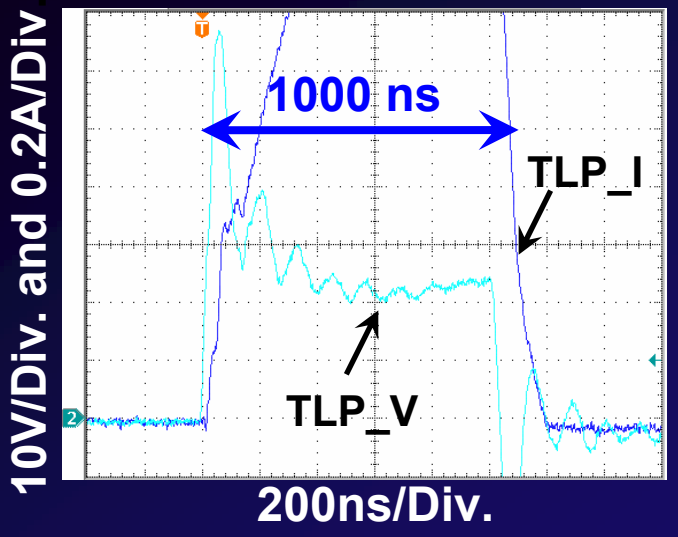


P-TFT under TLP Stress With 1000-ns Current Pulse

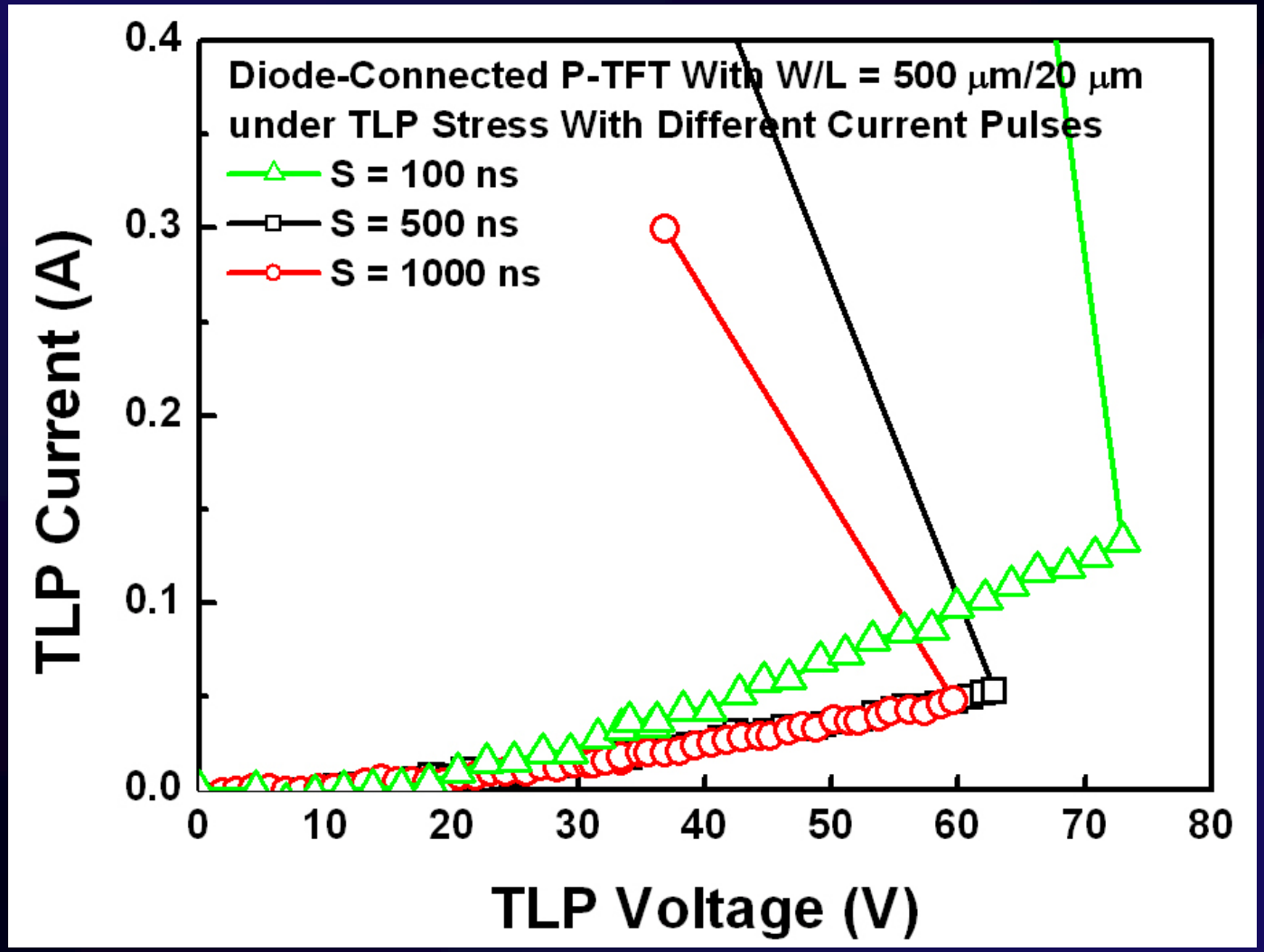






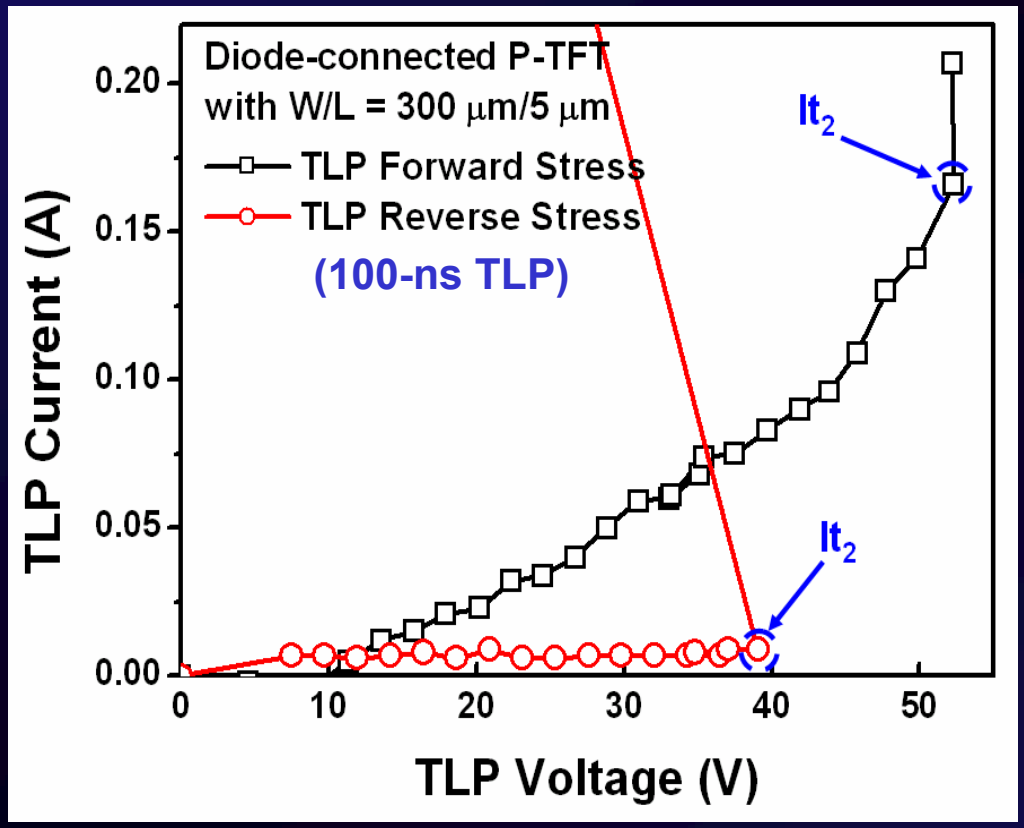


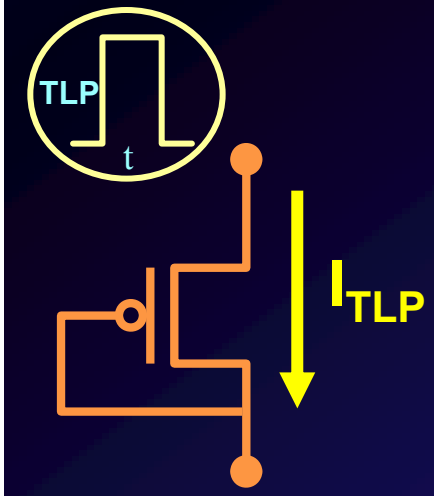
P-TFT under forward TLP Stress with Different Current Pulse Widths



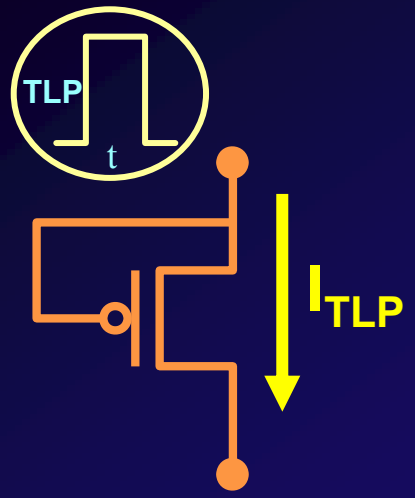
TLP I-V Curve of LTPS TFT Device under Forward and Reverse Stresses

The It2 of LTPS P-TFT device under forward TLP stress is much better than that under reverse TLP stress.



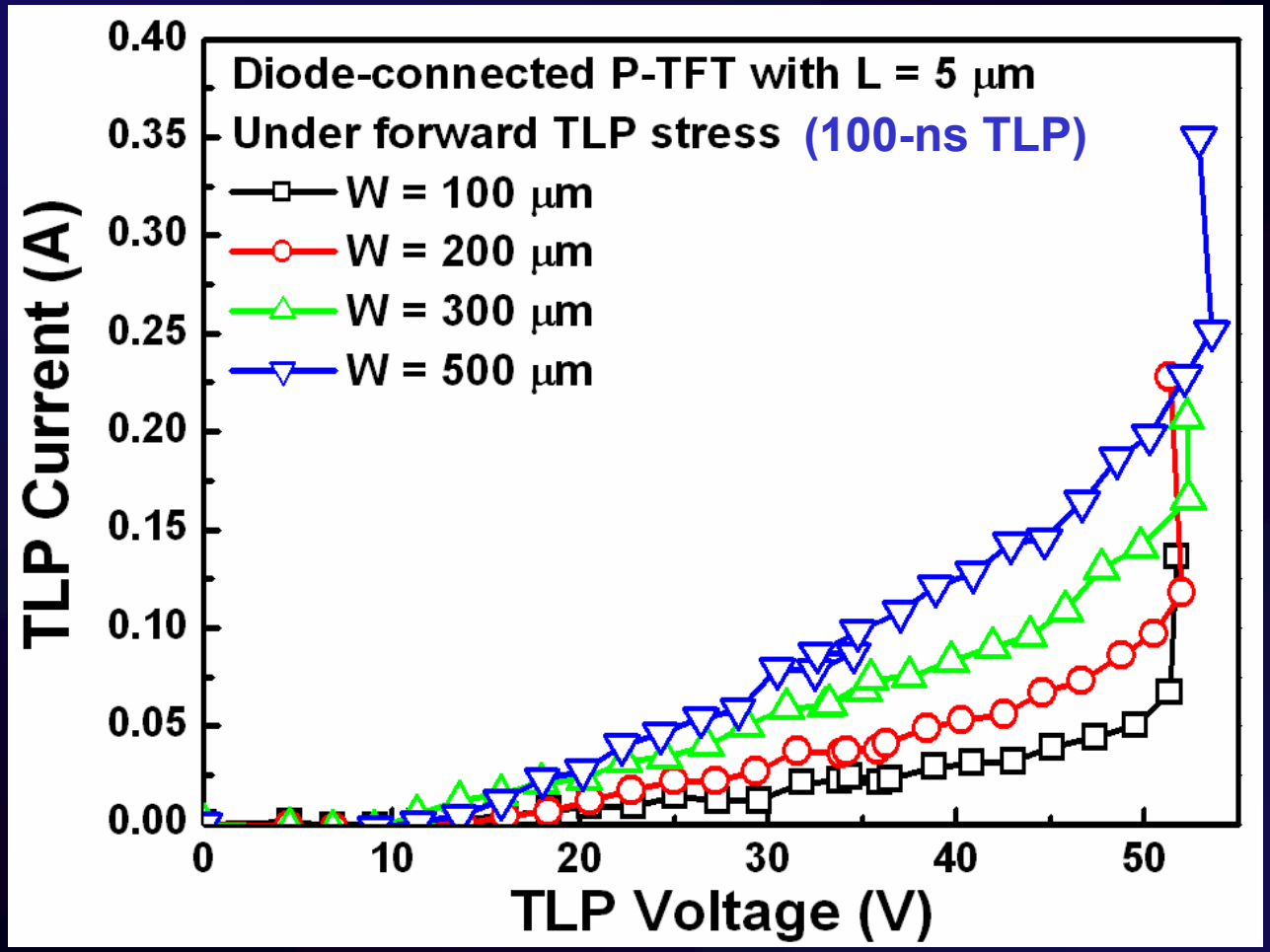


Forward Stress



Reverse Stress

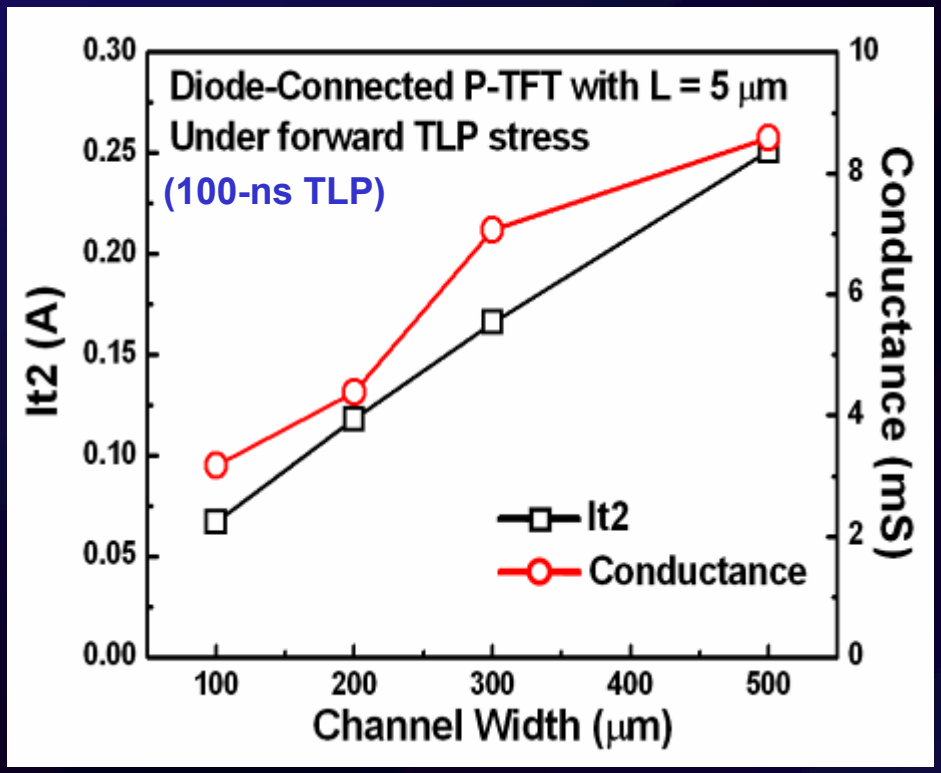
Dependence of It2 on P-TFT Channel Width

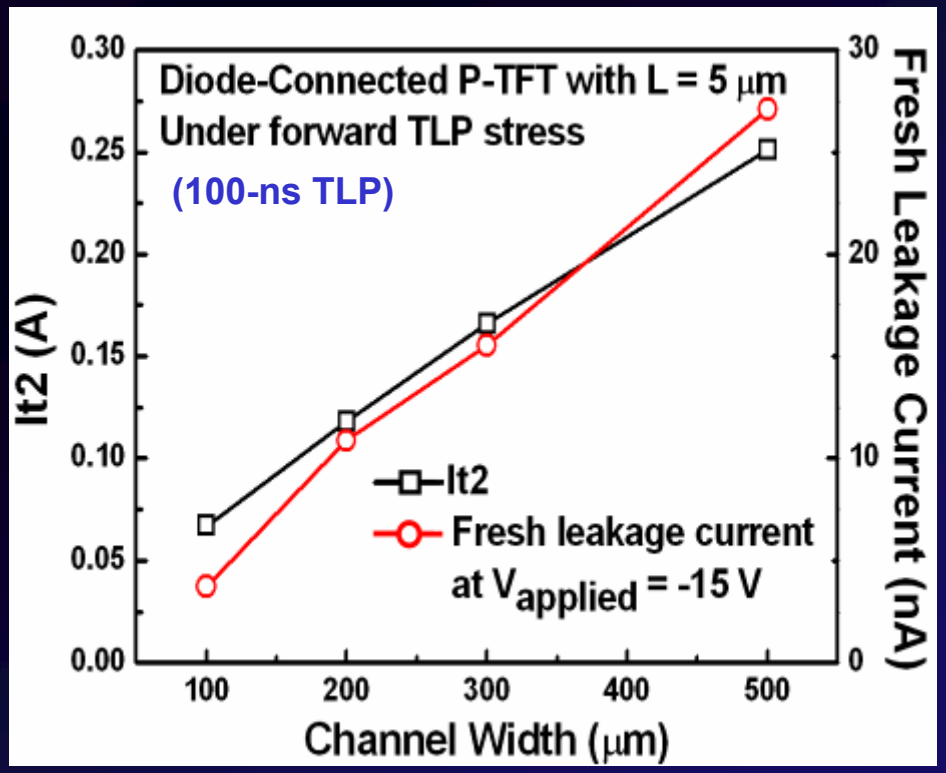


- Increasing channel width, the diode-connected P-TFT can sustain higher It2 current under forward TLP stresses.
- The It2 of diode-connected P-TFT is increased from 0.06 A to 0.26 A, when the channel width is increased from 100 μm to 500 μm.

Dependence of It2 on P-TFT Channel Width

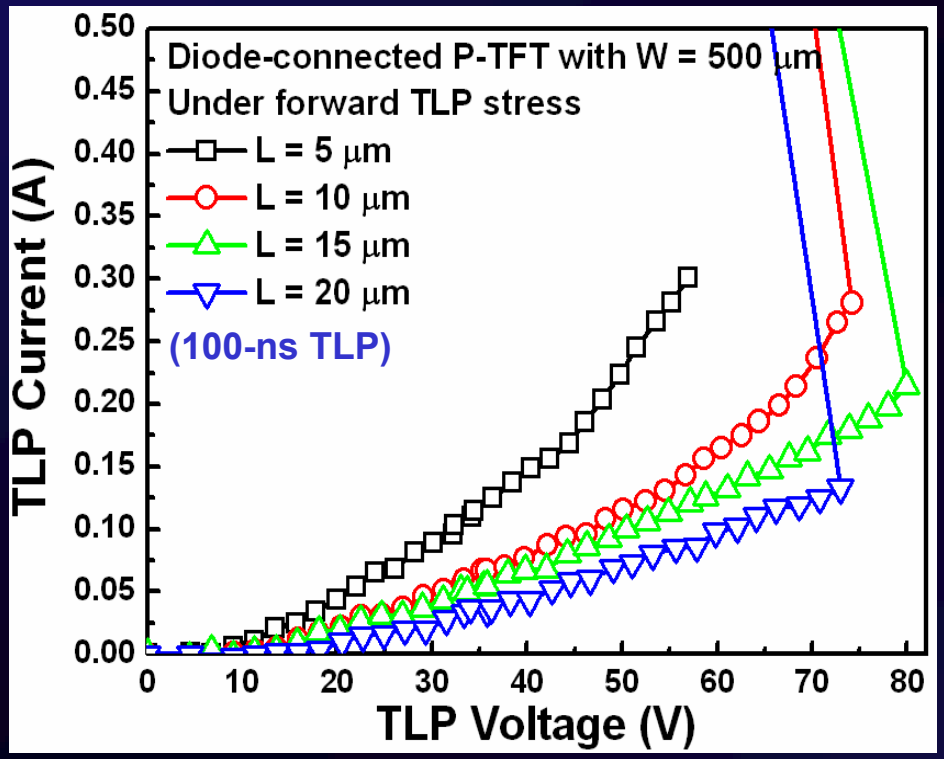
- The fresh leakage current and the turn-on conductance of diode-connected P-TFT are increased with the increase of channel width.

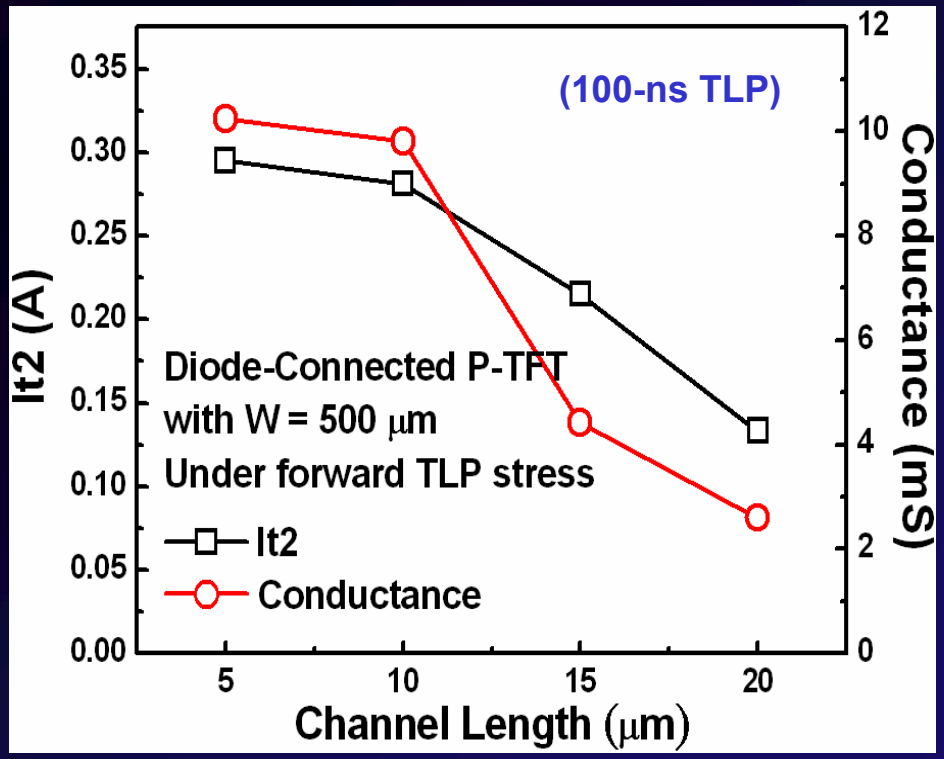




Dependence of It2 on P-TFT Channel Length

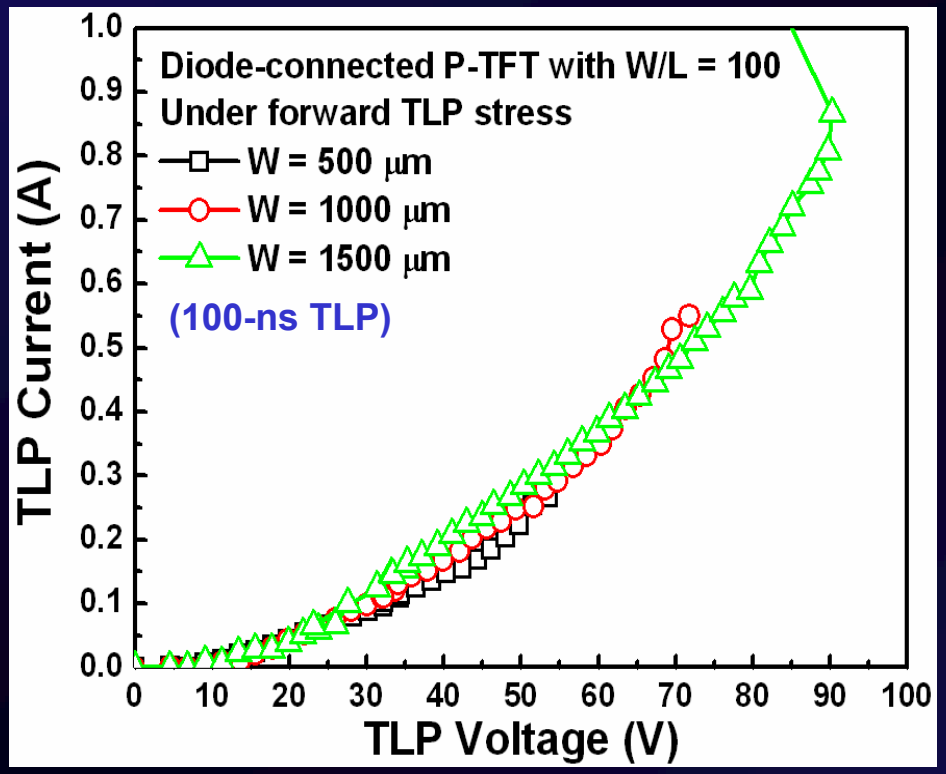
- Enlarging the channel length of P-TFTs (under the same channel width) will decrease its It2.
- The estimated HBM ESD level of diode-connected P-TFT with W/L = 500μm/5μm is only ~ 0.45 kV.

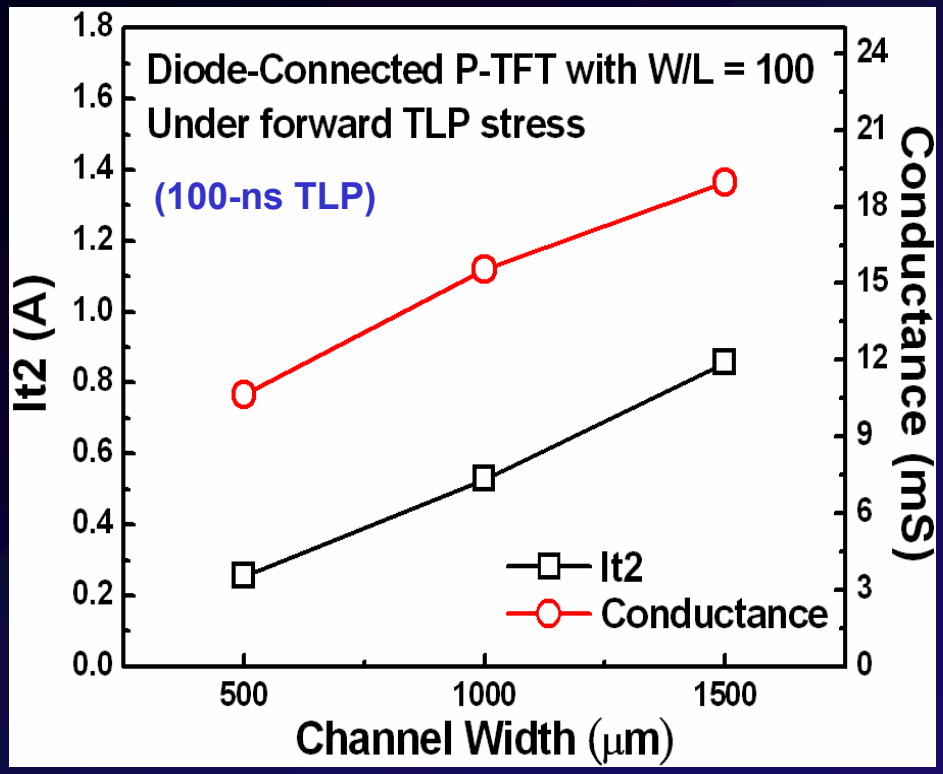




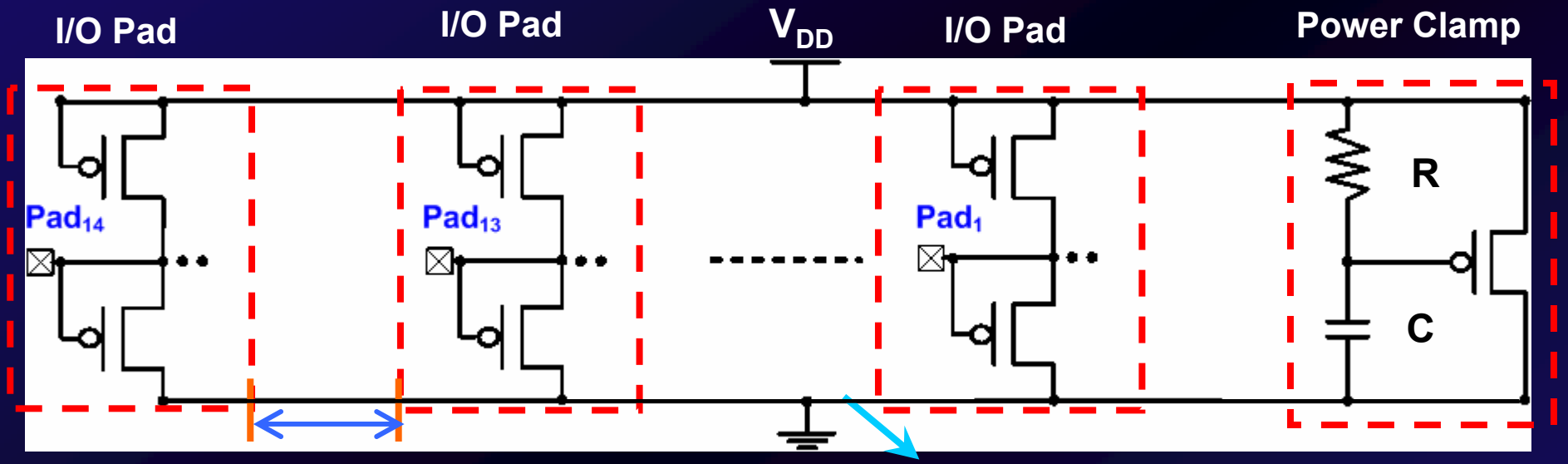
Dependence of It2 on P-TFT Device Dimension under fixed W/L Ratio (W/L=100)

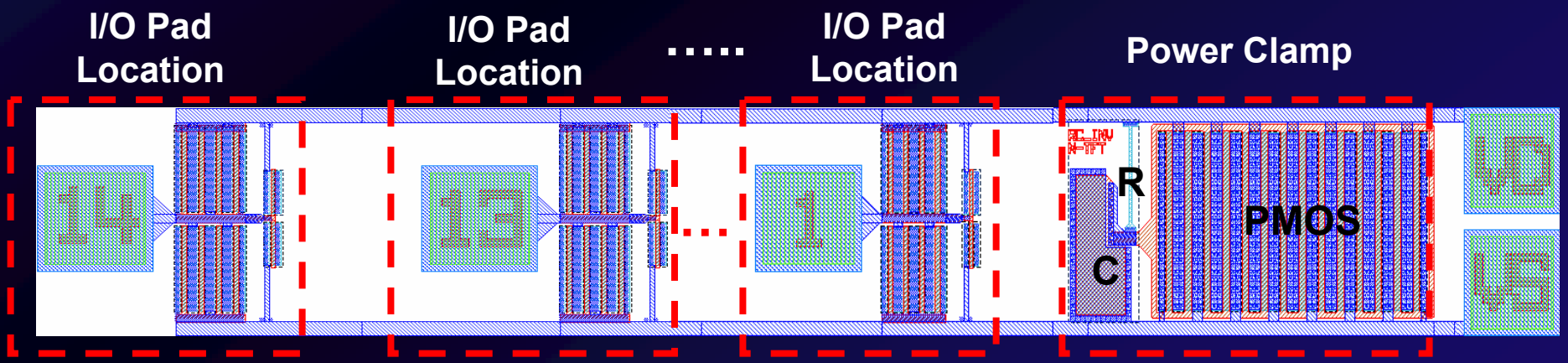
- P-TFT drawn with a larger device size has the more area for heat dissipation to sustain a higher It2 level.
- The estimated HBM ESD level of diode-connected P-TFT with W/L = 1500μm/15μm is about ~1.3 kV.





On-Panel ESD Protection Design with Power Clamp in a LTPS Process with P-TFTs





Conclusions

1. TFT device under forward-stress condition can sustain much higher It2 current than that under reverse-stress condition.
2. Enlarging the channel width of P-TFTs can improve It2 level, but accompanies the increased fresh leakage current.
3. Increasing the channel length under the same channel width, the turn-on conductance of the diode-connected P-TFT are decreased to cause a lower It2 level.
4. The diode-connected P-TFT drawn in the same W/L ratio with the increased device size can greatly improve It2 level, due to the larger area for heat dissipation.
5. On-Panel ESD protection design with active power-rail ESD clamp circuit should be added on the panel to operate P-TFT devices under forward-stress condition and therefore to achieve higher ESD robustness for System-on-Panel applications.

References

[1] S. H. Yeh *et al*., “A 2.2-inch QVGA system-on-glass LCD using p-type low temperature poly-silicon thin film transistors,” in *SID Tech. Dig*., pp. 352-355 (2005).

[2] F. R. Libsch *et al*., “ESD: how much protection is need for AMLCDs,” in *SID Tech. Dig*., pp. 255-258 (1994).

[3] S.-C. Lee *et al*., “Electrostatic discharge effects on poly-silicon TFTs for AMLCD,” in *SID Tech. Dig*., pp. 212-215 (2002).

[4] Y. M. Ha, “P-type technology for large size low temperature poly-Si TFT-LCDs,” in *SID Tech. Dig*., pp.1116-1119 (2000).

[5] S. C. Huang *et al*., “Statistical investigation on the variation behavior of low-temperature poly-Si TFTs for circuit simulation,” in *SID Tech. Dig*., pp. 329-332 (2006).

[6] M.-D. Ker *et al*., “Successful electrostatic discharge protection design for LTPS circuits integrated on panel,” in *SID Tech. Dig*., pp. 1400-1403 (2003).

[7] Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM), EIA/JEDEC Standard EIA/JESD22-A114-A (1997).