BOARD LEVEL ESD OF DRIVER ICS ON LCD PANELS

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ABSTRACT

A method utilizing Charged Device Model (CDM) discharging to emulate real-world Charged Board Model (CBM) discharging was proposed and successfully addressed the weakest spot of whole chip. In order to extract the correlation between CDM pre-fail voltage V_{CDM} and CBM pre-fail voltage V_{CBM}, the capacitance and discharging waveforms of output pin on an IC and Printed Circuit Board (PCB) were measured. The results showed that the CBM evaluation board (EB) was not a must for large-size chip, as LCD driver ICs. CDM discharging can be used to direct investigate the weak point of design/layout for large-size chip. Besides, this paper addresses the guidelines about chip-level ESD cell design and layout optimization against CBM ESD damage. [*Keywords*: ESD, CBM, HBM, CDM, PCB.]

1. INTRODUCTION

IC's robust to HBM & CDM damage at the chip-level may be susceptible to CBM damage at the board-level. Some publications have addressed these issues and solutions [1-5].

To look for the weakest point of whole-chip on chip-level, the PCB simulation proposed by Andrew et al. [5] and CDM simulation were performed to duplicate the CBM ESD damage.

Per FA results and the follow-up layout optimization, the chip-level CBM ESD immunity is greatly improved. The guidelines about ESD cell design and layout optimization are proposed.

2. EXPERIMENTAL

The chip sizes of TCS0001, TCG0001, and TCG0002 were 12000um×1600um, 6500um×1400um, and 6500um×1400um and the parasitic capacitance values mounted on the EB were about 300pF, 700pF, and 700pF, respectively, measured by HP4284 LCR meter at high frequency (1MHz). CDM testing was done on the commercial ThermoKeyTek ZapMaster 7/4 with maximum CDM +/-2kV discharging, and I-V characteristic measured by HP4155. The discharging waveforms were measured by Tektronix TDS7104 oscilloscope with 1 GHz bandwidth.

Two approaches to duplicate the CBM failure and evaluate the CBM immunity are presented as follows.

2.1 PCB to Simulate

The CBM test method described in [5] was used for verifying the CBM-like ESD damage.

2.2 CDM to Simulate

To simplify the process described in [5], the CDM simulation test method for duplicating the CBM failures was proposed and described as follows:

(1) Without mounting the TCP/COF sample on EB, measure the I-V characteristics of the PUT and the leakage current between power and ground after CBM test.

(2) Put the TCP/COF sample on the center of the JEDEC-standard charging plate. Then the PUT was discharged.

(3) Measure the I-V characteristics of the PUT and the leakage current between power and ground after CBM test to check any degradation.

In 2.1 and 2.2, the PUT was zapped in 200V or 250V increments until degradation was observed in the I-V characteristics. The pre-fail voltage level V_{CDM} before degradation was recorded.

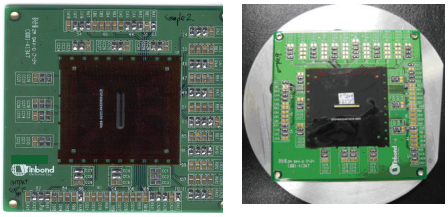


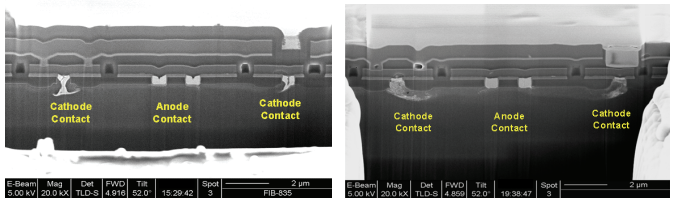
Fig. 1 (a) A Tape Carrier Package (TCP) sample was mounted on the high-capacitance Evaluation Board (EB). (b) The EB was put on the center of the charging plate.

3. RESULTS AND DISCUSSIONS

3.1 Duplicate CBM damages

TCS0001 was fabricated by 0.6um 10V HV-CMOS process. It was the source driver of LCD products that packaged by TCP and passed HBM 4KV, MM 200V, CDM +/-500V, and Latch-Up +/- 200mA test criteria. However, customer's return shows the Pad-to-V_{SUPPLY} ESD protection diode of output pin was destroyed with CDM-like damage. To verify the ESD damage, the CBM test method described in [5] was adopted, see Fig. 1.

The pull-up ESD protection diodes of output pin "VS<5>" were damaged after CBM +1000V and -1500V discharging. Both I-V measurement and SEM cross-section experiment results can successfully duplicate the same failure as customer's returns, as shown in Fig. 2. Therefore, the root cause is considered as the CBM damage.



(a) (b)

Fig. 2 The SEM cross section view of the pull-up ESD protection diodes of output pin "VS<5>." (a) Customer's returns. (b) After CBM +1000V simulation. The same contact spiking at cathode as customer's returns was successfully duplicated by the CBM simulation.

3.2 Correlation between PCB and CDM Simulation

TCG0001 was fabricated by 0.6um 40V HV-CMOS process and passed HBM 2KV, MM 200V, CDM +/-500V, and Latch-Up +/-100mA test criteria. It was the gate driver of the LCD panel that packaged by COF. The LV input pin was tested by CBM emulation (zapped in +/-200V charge voltage increments) and the results showed that it just passed CBM +600V/-400V, possibly the weakest point of whole chip.

Fig. 3 showed the SEM top-view of failure site after +800V/-600V discharging from LV input pin. The gate of internal PMOS was damaged, no matter positive or negative discharging.

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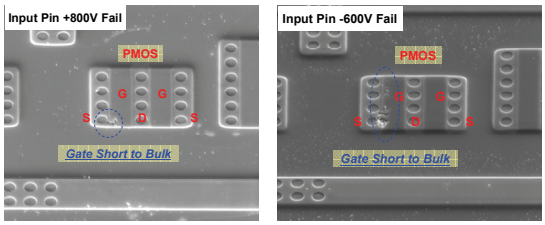
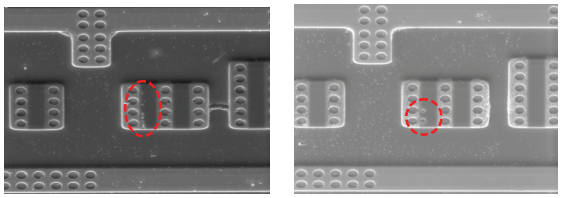
The LV input pin of TCG0001 was also tested by CDM emulation and passed CDM +/-750V but failed +/-1000V discharging. Fig. 4 showed the SEM top-view of failure site after CDM +1000V/-1000V discharging from LV input pin, which is the same as the one for CBM simulation. This important observation hints that one can utilize CDM discharging to address the weakest spot of whole chip during CBM discharging.



(a) (b)

Fig. 3 The SEM top-view of failure site after **CBM** emulation (a) +800V and (b) -600V discharging from LV input pin of TCG0001.



(a) (b)

Fig. 4 The SEM top-view of failure site after **CDM** emulation (a) +1000V and (b) -1000V discharging from LV input pin of TCG0001. Compared to Fig. 3, one can utilize CDM discharging to look for or anticipate the weakest spot of whole chip if it actually suffers from CBM discharging.

As reported [5], CBM discharging waveform has much higher I_{PEAK} and a faster T_{RISE} than the corresponding CDM for the same coupling voltage, due to lower inductance and resistance of the board discharge path and larger effective capacitances at board-level in comparison with the chip-level. Therefore, the pre-fail voltage V_{CDM} needs to be much higher than the corresponding pre-fail voltage V_{CBM} to obtain the same damage.

We've found the parasitic capacitance of I/O pins mounted on EB was ~10 times the parasitic capacitance of I/O pins without EB ($C_{CBM}/C_{CDM} \fallingdotseq 10$), but $V_{CDM}/V_{CBM} \neq 10$. The inconsistency was because during CBM discharging the parasitic resistance of discharging path on EB would lower the peak voltage of ESD, thus the pre-fail V_{CBM} was larger than expected. Fig.5 showed the test results. The voltage waveforms of CBM 100V discharging on the golden pad (point A) and on the TCP/COF IC direct (point B) show the peak voltage values of CBM discharging were different due to the parasitic resistance between A and B. The factor was ~2. So, the parasitic resistance of the path on EB shown in Fig.5 must be minimized to achieve higher peak voltage.

TCG0002 was modified from TCG0001 and fabricated by the same HV-CMOS process. Since the low-voltage input pin was the weakest point of whole chip in TCG0001, both primary and secondary ESD protection devices were re-designed to enhance the CBM/CDM immunity. All pins were tested by CDM discharging (zapped in +/-250V increments). The results were listed in Table.1. (The CDM tester has reached its maximum testing limit of 2KV capability.)

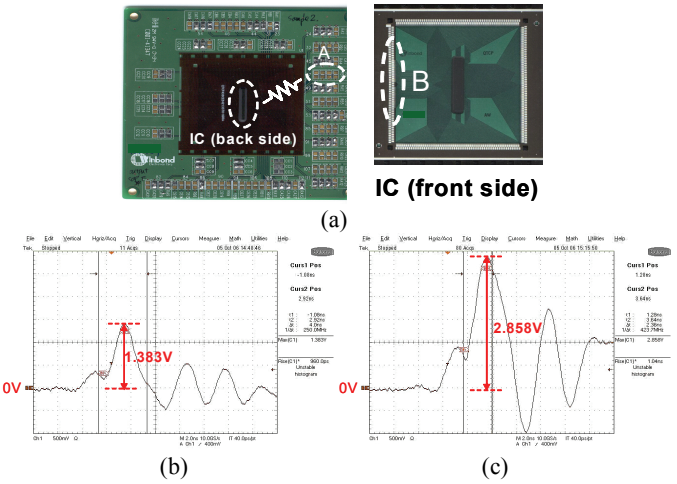
3.3 Chip- Level Guidelines to Minimize the CBM Failure

The guidelines to improve CBM immunity for (a) source driver and (b) gate driver ICs are summarized as follows:

(1) Select protection device with low turn-on resistance, low turn-on voltage, and high second breakdown current.

(2) Avoid current crowding and local high electric field.

(3) Enhance the capability of power clamp cells as much as possible because the power pad can become the major CBM discharging path during post-assembly final test.



(a) (b) (c)

Fig. 5 (a) The waveforms of CBM +100V discharging on the golden pad (point A) and on the TCP/COF IC direct (point B) were measured by voltage probe. (b) The peak voltage of discharging measured on A was about 1.383V. (c) The peak voltage of discharging measured on B was about 2.858V. The factor B/A was ~2.

Pin	Type	TCG0001	TCG0002
VCOM	HV Power	Pass **CBM** +/-2kV	Pass **CDM** +/-2kV
VDD	LV Power	Pass **CBM** +/-2kV	Pass **CDM** +/-2kV
VSS	LV Ground	Pass **CBM** +/-2kV	Pass **CDM** +/-2kV
VEE	HV Ground	Pass **CBM** +/-2kV	Pass **CDM** +/-2kV
Input	LV	Pass **CBM** +600V/-400V	Pass **CDM** +/-2kV
output	HV	Pass **CBM** +2kV/-800V	Pass **CDM** +2kV/-1250V

Table.1

4. CONCLUSION

A method utilizing CDM discharging to emulate real-world CBM discharging was proposed in this paper. This technique successfully duplicated the same failure resulted from CBM discharging for large-size chip such as LCD driver ICs. Thus one can use CDM discharging to direct locate the weakest spot of whole chip. The parasitic resistance of the path on EB must be minimized to achieve higher and more accurate CBM discharging peak voltage. Finally, the guidelines about chip-level ESD cell design and layout optimization against CBM ESD damage were proposed and the immunity against CBM is greatly improved.

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