Automation of Synchronous Bias Transmission Line Pulsing System

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ABSTRACT

Synchronous Bias Transmission Line Pulsing (SB-TLP) system is able to provide a synchronous bias voltage to transmission line Pulse. It's a more useful test bench to evaluate actual circuit characteristics of electrostatic discharge (ESD) protection design with gate-driven mechanism than traditional Transmission Line Pulsing (TLP) system. It's important to set up an automatic SB-TLP system and be able to immediately analyze measured data which is more convenient to engineers. All of the instruments are controlled by a software written in LabVIEW environment to create a smart and friendly test workbench.

INTRODUCTION

ESD reliability has become a serious issue in deep submicron CMOS ICs. Furthermore, ESD protection needs to be optimized to protect the ultra thin gate oxide MOS devices. The traditional Transmission Line Pulsing (TLP) system [1]-[4] is able to evaluate second breakdown characteristic of It2, turn-on resistance (R*on*), trigger voltage (Vt1) and snapback holding voltage (Vh) due to its unique technique in test on ESD protection devices. Also, the ESD level is directly proportional to the second breakdown current (It2). The influence of ESD protection devices with triggered mechanism on Vt1, Vh, R*on* and It2 are researched to optimized the ESD protection designs, such as gate-driven NMOS/PMOS and substrate-triggered field-oxide device...etc. [5]-[12]. In whole ESD protection circuit, the whole ESD protection devices are shown in Fig. 1. In order to improve the ESD robustness in I/O cells, the gate terminals of the NMOS and PMOS transistors were connected to the resistors to enhance the turned-on uniformity by the gate couple technique. The power-rail ESD clamp device is also designed with the active triggered mechanisms, such as gate-driven technique and substrate-triggered technique, to enhance the turned-on characteristics, as shown in Fig. 2. Traditional TLP system is designed to provide a dc gate-bias voltage sourcing for testing ESD protection devices during TLP test. The dc gate-bias voltage arrives faster at gate terminal than transmission line pulse stresses about 80 microseconds with several hundred nano-seconds dc gate-bias voltage pulse width. The gate-driven ESD protection design has been researched to improve ESD robustness. As shown in Fig. 3, the NMOS device is under TLP test, but the dc gate-bias voltage is not simulating the actual circuit characteristics of gate-driven MOS devices during TLP test. In order to simulate reality, the Synchronous Bias Transmission Line Pulsing (SB-TLP) is first proposed and evolved from traditional TLP system to meet actual circuit characteristics.

SB-TLP system involves the use of Laboratory Virtual Instrument Engineering Workbench (LabVIEW) environment by National Instruments to provide a low-cost solution for automatic connectivity of controlled instruments [13]. The virtual Graphical User Interface (GUI) [14] allows users to integrate the instruments in SB-TLP system and set measurement parameters via Personal Computers (PCs) monitor easily and conveniently. The automatic SB-TLP is able to shorten measurement cycles.

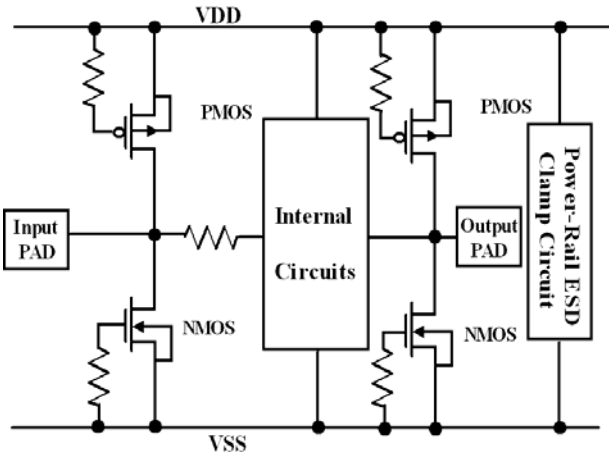


Figure 1: The whole ESD protection circuit.

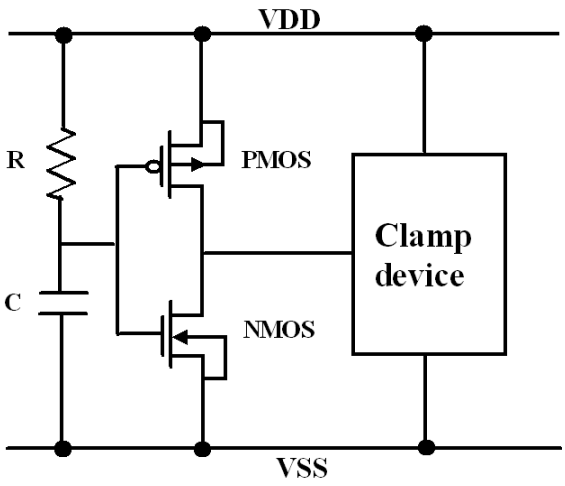


Figure 2: The power-rail ESD clamp circuit.

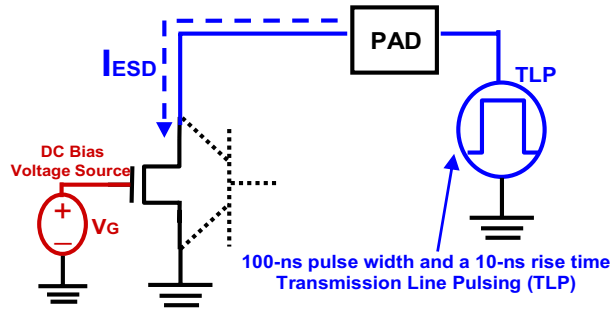


Figure 3: Traditional Transmission Line Pulsing (TLP) system with dc bias voltage sourcing to drive gate terminal.

SYNCHRONOUS BIAS TRANSMISSION LINE PULSING SYSTEM

The testing equipments connectivity scheme of Synchronous Bias Transmission Line Pulsing (SB-TLP) system is shown in Fig. 4 and its corresponding circuit is shown in Fig. 5.

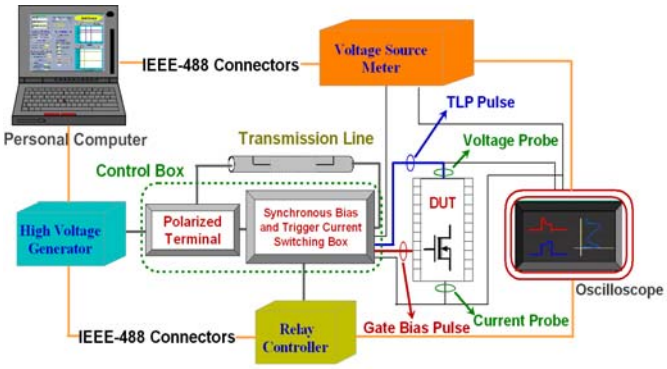


Figure 4: Synchronous Bias Transmission Line Pulsing (SB-TLP) system setup.

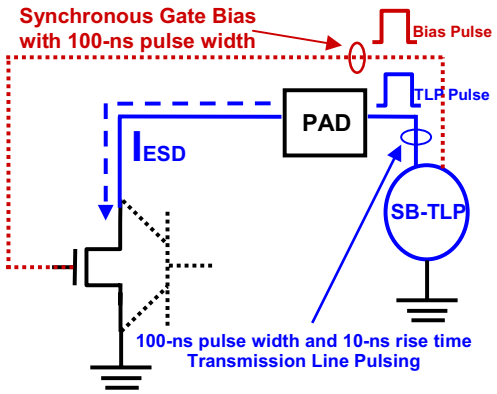


Figure 5: Corresponding measurement circuit for Synchronous Bias Transmission Line Pulsing system.

A .Basic operation of SB-TLP system

In Fig. 4, to start with SB-TLP system, high voltage generator (*Keithley 2410*) is first used to measure leakage current to check failure criteria of Devices Under Test (DUT). Next, it provides a dc-bias voltage (called the dc pre-charge voltage) charges to transmission line, and finally, the dc pre-charge voltage stresses the DUT and digital oscilloscope (*TDS 3054*) measure the I-V data at the same time. During the failure criteria stage, voltage source meter (*Keithley 2410*) is able to provide a dc-bias voltage, and during stress stage, it's also able to provide a dc-bias voltage, and synchronizes to transmission line pulse. Among leakage measurement, charging the transmission line and stress stages, control box follows with each stages controlled by relay controller (*HP 3631A*).

B. Setup of SB-TLP system

In the Fig. 6, high voltage generator generates dc-bias voltage charges to the transmission line with a step increment, and the supply voltage range of high voltage generator from -1100V to +1100V, it's adequate to accomplish general ESD protection devices measurement. The control box controls the energy pulse, which is stored in transmission line, to apply to the DUT. The relay controller is a multi-channel voltage source for controlling relays to switch on or off inside the control box sequentially.

The synchronous bias switching box must be able to sense transmission line pulse, and provide a synchronous bias transmission line pulse biasing to the DUT with exactly 100-ns pulse width and equal rising slope. The voltage source meter is used to provide a stable dc-bias voltage to the synchronous bias switching box to generate an accurate synchronous bias voltage. Under the SB-TLP stress, the gate-bias voltage pulse synchronously biases the gate node of the NMOS device with desired gate-bias voltage, which can be controlled by the additional voltage source, as shown in the Fig. 3. The inside of control box is merged with synchronous bias switching box and polarized terminal, in order to save system volume, and shorter connected line for decreasing noise effect.

In measuring the I-V behavior of ESD protection devices with SB-TLP system, the digital oscilloscope is applied with a current probe (CT1) and a voltage probe (P6139A) manufactured by Tektronix, with spec. of 500MHz bandwidth and 5GS/s sample rates that are enough to measure the SB-TLP pulse with 100-ns pulse width and rise time between 2 and 10ns precisely Prototyping with Labview Environment

PROTOTYPING WITH LABVIEW ENVIRONMENT

LabVIEW has not only mainly been used by Test Engineer (TE) to develop a rapid prototype of an automatic measurement system but also been used to produce emulations in systems for real hardware/software implementations. Via its flexible instrumentation and software environment match with PCs running Microsoft Windows, a main part for setting measurement parameters Graphical User Interface (GUI) was created. In the preceding chart of Fig. 4, all instruments are connected by General Purpose Interface Bus (GPIB) interface through a cable equipped with IEEE-488 connectors. Each instrument has its own GPIB address and Standard Commands for Programmable Instruments (SCPI) command subsystems for unique communication protocol. In Fig. 4, it needs to enter each numbers in the items of Instrument GPIB Address. In the items of Gate Bias/Sub-Trigger setup, if users want to bias a dc voltage during the process of failure criteria stage, it needs to set a parameter of Bias Voltage. Comparatively, it also needs to set a parameter of synchronous voltage during SB-TLP stress.

To define automatic stop measuring is when the measured leakage current bigger than leakage limitation in the final stage. From setting the leakage limitation in the items of failure criteria in GUI, in general ESD protection devices, if leakage limitation is over 1 microamp under operation voltage that means DUT was failed. After SB-TLP stressed DUT, one point I-V datum is acquired then back to PCs and shown on TLP I-V plot virtual interface, all I-V data have been acquisition after the end of a test cycle, and then shown on TLP I-V plot virtual interface for users to analyze high current characteristics of ESD protection devices correctly and completely.

For users to set up an automatic SB-TLP system, a flower chart of measurement process fluently is useful to direct programmer before writing LabVIEW. As shown in Fig. 6, each of the instruments follows with each stage. The stage of Applying Gate Bias/Sub-Trigger is designed for SB-TLP system and is different from traditional TLP system.

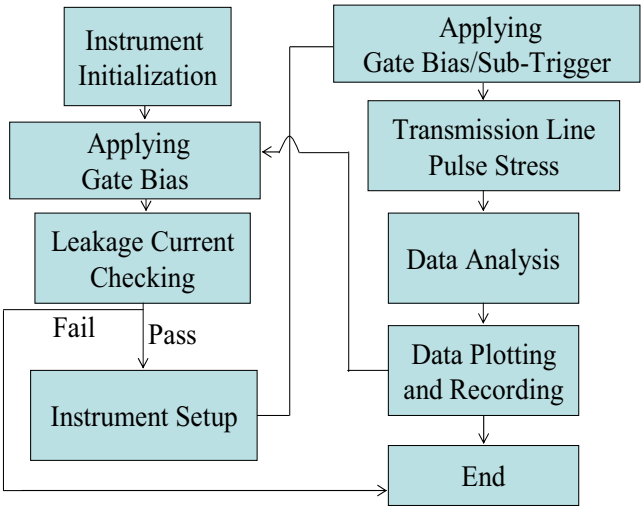
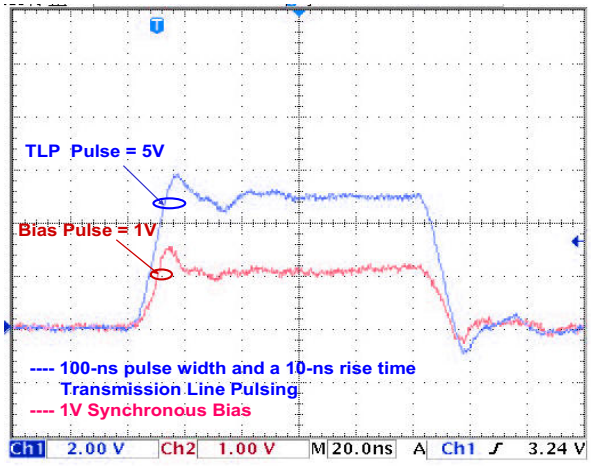


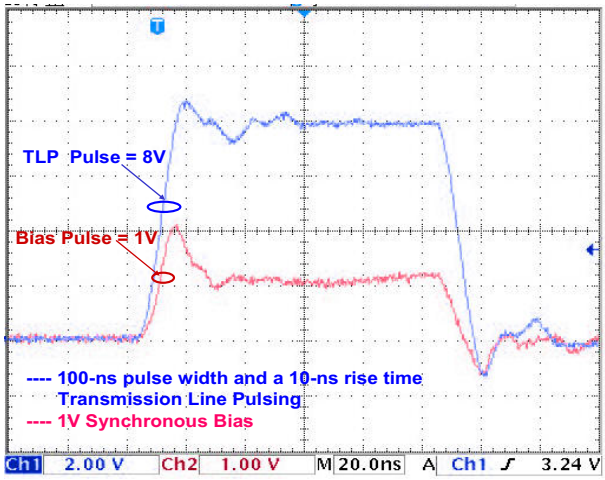
Figure 6: The program flower chart for prototyping SB-TLP system.

VERIFICATION OF SB-TLP SYSTEM

Before testing the DUT of SB-TLP system, it's necessary to verify synchrony between transmission line pulse and synchronous bias pulse with rising slope and pulse width. In addition, verification ensure stability during measurement cycles. The digital oscilloscope with two voltage probes of Tektronix P6139A is used to measure these two pulses generated in SB-TLP system in time domain. When a 5-V, 8-V, and 10-V transmission line pulses are generated, the synchronous bias switching box will sense the waveforms and a stable 1-V gate-bias pulse is synchronous generated at the same time, as shown in Fig. 7(a), Fig. 7(b), and Fig. 7(c), respectively. A stable gate-bias voltage pulse can be generated independently in many kinds of voltage orders by user's demand while the transmission line pulse increased. and both of them have 100-ns pulse width.



(a)



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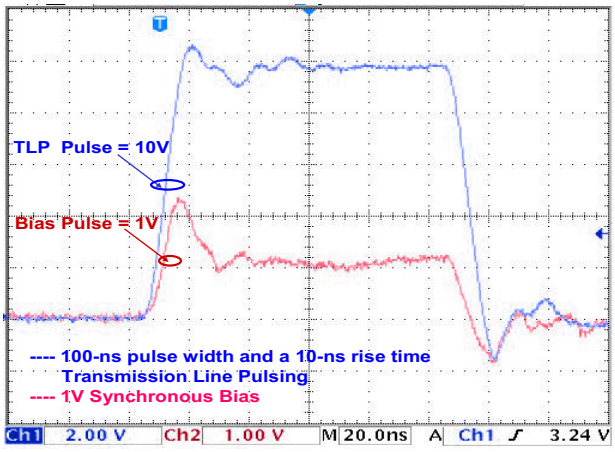

(c)

Figure 7: (a) 5-V, (b) 8-V, and (c) 10-V transmission line pulse with a synchronous 1-V gate-bias voltage pulse.

INVESTIGATION OF NMOS DEVICE

In this work, the structure of multi-finger NMOS device with device dimension (W/L) of 240μm/0.18μm and fabricated in a 130-nm salicided CMOS process, analysis of NMOS device I-V characteristic with different synchronous gate-bias voltages of 0, 0.2, and 0.5V under SB-TLP system test are shown in Fig. 7.

The turn-on resistance (R*on*) is defined as the slope of voltage variation over current variation between second breakdown and parasitic lateral N-P-N BJT is turned on via the SB-TLP system measured I-V data, as shown in Fig. 8. The second breakdown current (It2) and turn-on resistance (R*on*) are compared and shown in Fig. 9. The It2 of the NMOS device without gate-bias voltage is only 1.57 A, On the contrary, it can be increased up to 2.42 A, while the NMOS device with the synchronous gate-bias voltage increased to 0.5 V. Moreover, the turn-on resistance (R*on*) of the NMOS device with different synchronous gate-bias voltages is decreased from 3.49 to 2.36, when the synchronous gate-bias voltage is increasing from 0 V to 0.5 V. With a higher It2, the NMOS can sustain a higher ESD level.

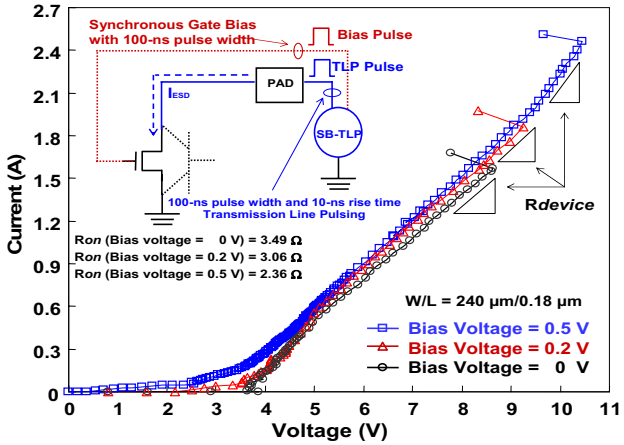

Figure 8: SB-TLP measured I-V curves and turned on resistance (R*device*) of the NMOS devices with different gate-bias voltages.

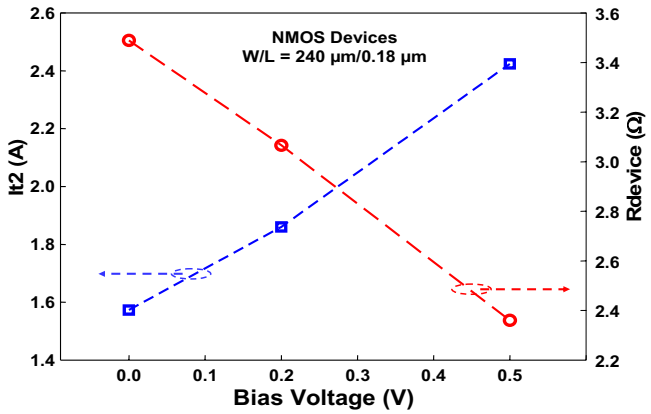

Figure 9: Dependence of It2 level and turn-on resistance (R*device*) on different gate-bias voltage of the NMOS device.

The parasitic lateral N-P-N BJT trigger voltage (Vt1), and the snapback holding voltage (Vh) of NMOS device with different gate-bias voltages are measured and compared in Fig. 10. The Vt1 is reduced from 3.87 V to 0.55 V and the snapback holding voltage (Vh) is seldom reduced to 3.5 V when the gate-bias voltage is increased from 0 to 0.5V. With a lower trigger voltage (Vt1), ESD performance of NMOS devices is greatly improved when the gate-bias voltage is increased.

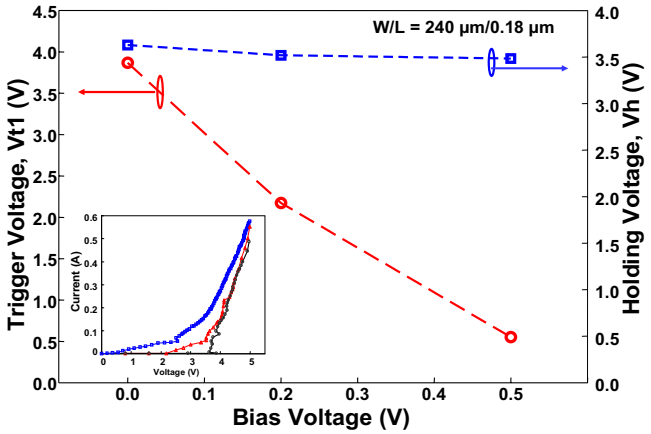

Figure 10: Dependence of the trigger voltage (Vt1) and the snapback holding voltage (Vh) of NMOS device on different gate-bias voltage.

CONCLUSION

SB-TLP system is automated by LabVIEW environment and GPIB interface successfully, it's conveniently, needs shorten operation cycles to control SB-TLP system and easier to analyze measured data by GUI from personal computers monitor for users. According to the SB-TLP system, the measured results with different synchronous gate-bias voltages of 0, 0.2, and 0.5V, the It2 values are obviously improved by the increments of the gate-bias voltage. Therefore, the SB-TLP system can provide actual circuit characteristics of the ESD protection design with gate-driven technique to optimize the gate-biased voltage in gate-driven ESD protection design.

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