Design on Mixed-Voltage I/O Buffers with Consideration of Hot-Carrier Reliability

Ming-Dou Ker and Fang-Ling Hu
Nanoelectronics and Gigascale Systems Laboratory
Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan

Abstract — **A new circuit design for mixed-voltage I/O buffers to prevent hot-carrier degradation is proposed. The mixed-voltage (2xVDD tolerant) I/O buffer is designed with hot-carrier-prevented circuits in a 0.18-μm CMOS process to receive 3.3-V (2xVDD tolerant) input signals without suffering gate-oxide reliability, circuit leakage issues, and hot-carrier degradation. In the experimental chip, the proposed mixed-voltage I/O buffer can be operated with signal speed of up to 266 MHz, which can fully meet the applications of PCI-X 2.0.**

I. Introduction

With new generations of CMOS technologies, the transistors' dimensions have been scaled down to reduce the silicon cost, as well as, to increase circuit performance and operating speed. The thickness of gate oxide becomes much thinner in order to reduce the core power supply voltage (VDD) for resulting in lower power consumption. In the meanwhile, the maximum tolerable voltage across the transistor terminals (drain, source, gate, and bulk) should be correspondingly decreased to ensure lifetime.

Some standardized protocols or ICs designed and fabricated with the previous CMOS generations, however, may communicate in a microelectronics system with the chips fabricated in advanced CMOS processes. Therefore, the chips in advanced CMOS processes will face to the interface of input signals with voltage levels higher than their normal supply voltage (VDD). Such mixed-voltage I/O interfaces must be designed to overcome several problems, such as gate-oxide reliability [1], hot-carrier degradation [2], and undesired circuit leakage paths [3].

A design technique with two-stacked transistors has been typically used in 2xVDD-tolerant I/O buffers without using thick gate oxide [4]-[6]. Such prior designs can successfully handle the input voltage levels higher than their normal supply voltages without suffering the gate-oxide degradation. But, such 2xVDD-tolerant I/O buffers still suffer the reliability issue of hot-carrier degradation, when the I/O signal has a transition from high (2xVDD) to low (0V).

A method with three-stacked transistors for 2xVDD-tolerant circuit was reported in [7] to eliminate both gate-oxide degradation and hot-carrier effect. According to logic transistor sizing, each of the three stacked transistors should be 1.5 times larger in device size than that of the two-stacked transistors to keep the same driving ability of the circuit as that of original circuit. Therefore, it results in a larger parasitic capacitance to slow down the speed of the signal at I/O pad.

In this paper, a novel circuit design (called as hot-carrier-prevented circuit) is proposed to solve hot-carrier reliability issue in the 2xVDD-tolerant I/O buffers with two-stacked transistors. The driving ability of the new proposed 2xVDD-tolerant I/O buffer can be kept the same as that of the original mixed-voltage I/O buffer with the same device dimensions.

II. Hot-Carrier Preveneted Circuit

A. Hot-Carrier Issue in Traditional Mixed-Voltage I/O Buffer

Fig. 1 shows the brief schematic of 2xVDD-tolerant I/O buffer with two-stacked transistors (MN0 and MN1) to implement the pull-down function, where the pull-down signal (PD) and the pull-up signal (PU) are controlled by the pre-driver. The 2xVDD-tolerant I/O buffers can typically receive 0V-to-2xVDD input signals and transmit 0V-to-VDD output signals. The hot-carrier degradation or the gate-oxide degradation may exist in the following two states: (1) the state of receiving 2xVDD input signal and (2) the transition from receiving 2xVDD input signal to transmitting 0-V output signal.

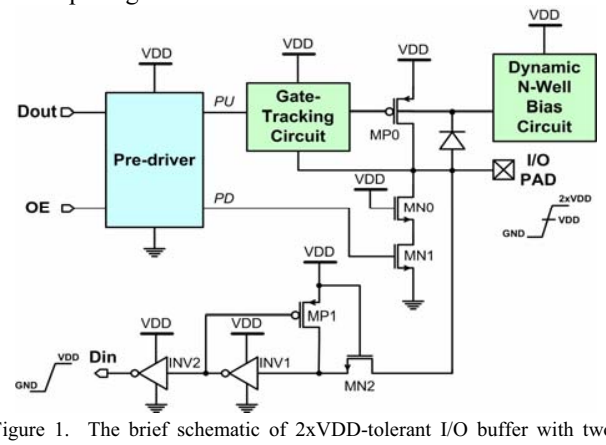


Figure 1. The brief schematic of 2xVDD-tolerant I/O buffer with two-stacked transistors (MN0 and MN1) to implement the pull-down function.

When such 2xVDD-tolerant I/O buffer receives 2xVDD input signals, PU and PD signals are kept at VDD and 0V, respectively, to disable the output circuit. Since the transistor MN1 in Fig. 1 is turned off, the transistor MN0 is weakly "on". This results in a voltage of about VDD at the source of MN0. The voltages drop across the gate-oxide and the drain-source voltage of MN0 and MN1 are both lower than or

equal to the supply voltage (VDD). There is neither hot-carrier degradation nor gate-oxide overstress issues in this circuit to receive 2xVDD input signal.

However, when the 2xVDD-tolerant I/O buffer has the transition from receiving 2xVDD input signal to transmitting 0-V output signal, the I/O PAD originally has a voltage of 2xVDD before being pulled down. At this transition moment, the transistor MN1 is turned on by PD signal from pre-driver, and the transistor MN0 is subsequently switched on when its source is pulled down by the MN1. The voltage at the drain of MN1 can be approximated as the saturation drain voltage (V_{DSAT}) [8]. Thus, the voltage at the source of the transistor MN0 is about ~0.5V. Since the original 2xVDD voltage at I/O PAD is not pulled down immediately, the drain-source voltage of MN0 would be larger than the normal supply voltage (VDD) during this transition, which results in the significant hot-carrier degradation on the transistor MN0. From this point, the traditional I/O buffer with two-stacked transistors in Fig. 1 is difficult to build a reliable 2xVDD-tolerant I/O buffer with only 1xVDD devices in a given CMOS technology, unless an additional circuit is provided to prevent such hot-carrier degradation during signal transition.

B. Hot-Carrier Prevented Circuit

A circuit using three-stacked transistors in Fig. 2 is reported in [7] to suppress hot-carrier degradation for the 2xVDD-tolerant I/O buffer. According to logic transistor sizing, each of the stacked transistors is 1.5 times larger in device size than that of the two-stacked transistors in Fig. 1 for equal driving capacity. As a result, the 2xVDD-tolerant I/O buffer with three-stacked transistors can solve the hot-carrier effect with the extra penalty of increased silicon area and longer propagation delay.

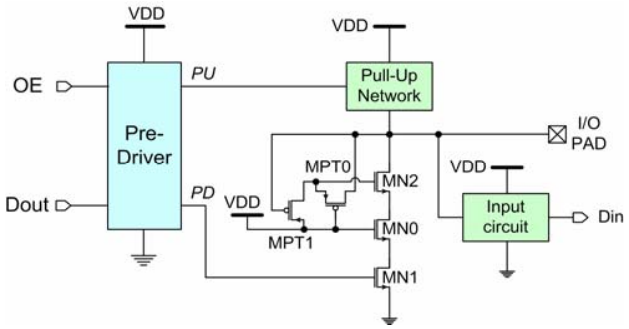


Figure 2. The brief schematic of 2xVDD-tolerant I/O buffer with three-stacked transistors to overcome hot-carrier issue.

The new design concept to prevent hot-carrier effect in 2xVDD-tolerant I/O buffer with only two-stacked transistors is proposed in Fig. 3. The gate-controlled signal on MN1 has a delay of PD signal from the pre-driver. During the transition from receiving 2xVDD input signal to transmitting 0-V output signal, the switch SW0 will be turned on by the control signal V_{CTRL} to pull down I/O PAD to VDD. The delay should be long enough to have I/O PAD pulled down to VDD before the MN1 is switched on. Thus, the drain-source voltage of MN0 during such transition is not larger than its maximum normal operation voltage range (VDD) in a given CMOS process. The switch SW0 must be kept off in all states except the high-to-low transition, so that this 2xVDD-tolerant I/O buffer can be operated correctly in both receive mode and transmit mode. Hence, the 2xVDD-tolerant I/O buffer with the new proposed circuit in Fig. 3 does not suffer the hot-carrier degradation.

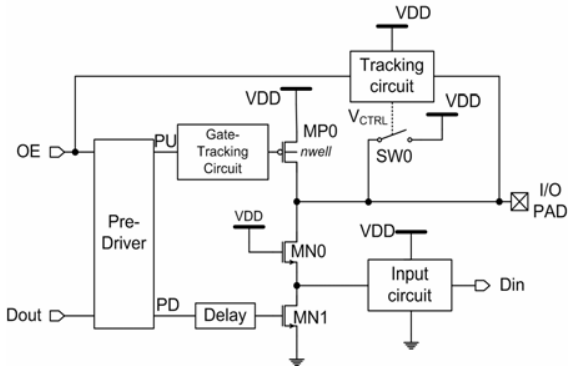


Figure 3. The new design concept to overcome the hot-carrier issue in the 2xVDD-tolerant I/O buffer with only two-stacked transistors.

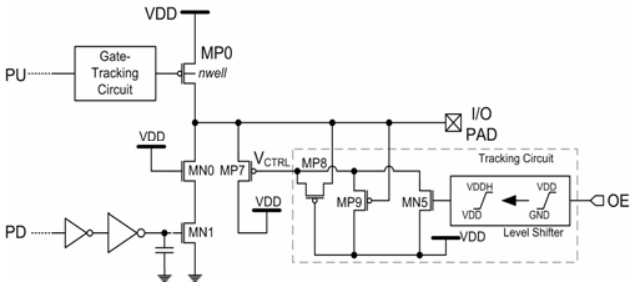


Figure 4. The implementation of the new proposed hot-carrier-prevented circuit for 2xVDD-tolerant I/O buffer with two-stacked transistors.

Table I Operations of the proposed hot-carrier-prevented circuit in 2xVDD-tolerant I/O buffer.

Modes	OE	I/O PAD	V_{CTRL}
Receive	0 V	0V	VDD
Receive		2xVDD	2xVDD
Transmit	VDD	X	VDD

The implementation of the new proposed hot-carrier-prevented circuit is shown in Fig. 4, where the input circuit is omitted. The delay cell can be implemented simply by inverter chain. The switch SW0 in Fig. 3 is realized by the PMOS transistor MP7 with a tracking circuit. A small capacitor can be inserted into the output of the inverter chain to meet the desired delay time, which can be estimated by the following equation:

$$\Delta Q = C_L \Delta V = I_{MP7} \Delta t \ , \quad (1)$$

where the C_L is the output loading at I/O PAD, ΔV=2xVDD-VDD, and I_{MP7} is the saturation current of transistor MP7. The tracking circuit comprises two PMOS transistors, MP8 and MP9, a NMOS transistor, MN5, and a level shifter which shifts a voltage level of 0/VDD to VDD/2xVDD [5]. The corresponding voltages in two operating modes

(transmit and receive modes) of the proposed hot-carrier-prevented circuit in Fig. 4 are listed in Table I.

When the 2xVDD-tolerant I/O buffer has the transition from receiving 2xVDD input signal to transmitting 0-V output signal, the gate voltage of MN1 originally stays at 0V while the PD signal is changing from 0V to VDD by the pre-driver. In the meanwhile, the V_{CTRL} is set to VDD by switching on the MN5, and consequently the MP7 is turned on to discharge the initial voltage of 2xVDD at the I/O PAD. After hundreds of picoseconds, the voltage at I/O PAD has been pulled down to about VDD, and the gate voltage of MN1 increases to VDD after the delay from the inverter chain. Therefore, the drain-source voltage of MN0 can be kept within the range of maximum normal operating voltage (VDD) during the transition, that resulting in no hot-carrier degradation. The 2xVDD-tolerant I/O buffer with new proposed hot-carrier-prevented circuit does not suffer the problems of gate-oxide reliability and hot-carrier degradation in both the steady states of receive mode and transmit mode and the transition from high to low.

III. Whole 2xVDD-Tolerant I/O Buffer With Hot-Carrier-Prevented Circuit

The whole 2xVDD-tolerant I/O buffer with the new proposed hot-carrier-prevented circuits is shown Fig. 5, which is designed to meet the operation speed of 266MHz for PCI-X 2.0 applications in a given 0.18-μm CMOS process. This 2xVDD-tolerant I/O buffer transmits 0V-to-1.5V output signals and receives 0V-to-3.3V input signals. In Figs. 6(a) ~ 6(c), three hot-carrier-prevented circuits with the corresponding nodes in Fig. 5 are designed to solve the hot-carrier reliability issues on MN0, MN3, MN2, and MP2 in the 2xVDD-tolerant I/O buffer. Note that all the bulks of PMOS transistors in hot-carrier-prevented circuits are connected to the self-biased n-well (*nwell*) marked in Fig. 5 to avoid leakage paths.

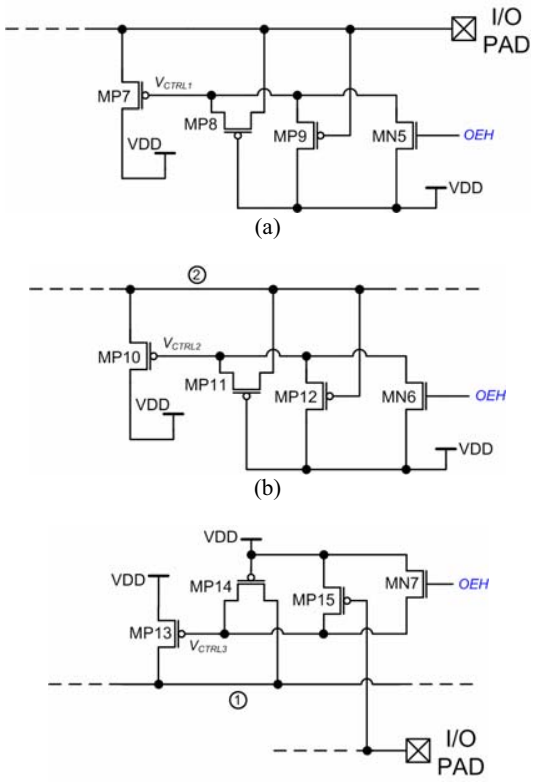


Figure 6. The corresponding hot-carrier-prevented circuits in Fig. 5. (a) The hot-carrier-prevented circuit for the MN0. (b) The hot-carrier-prevented circuit for the MN3. (c) The hot-carrier-prevented circuit for the MN2 and MP2.

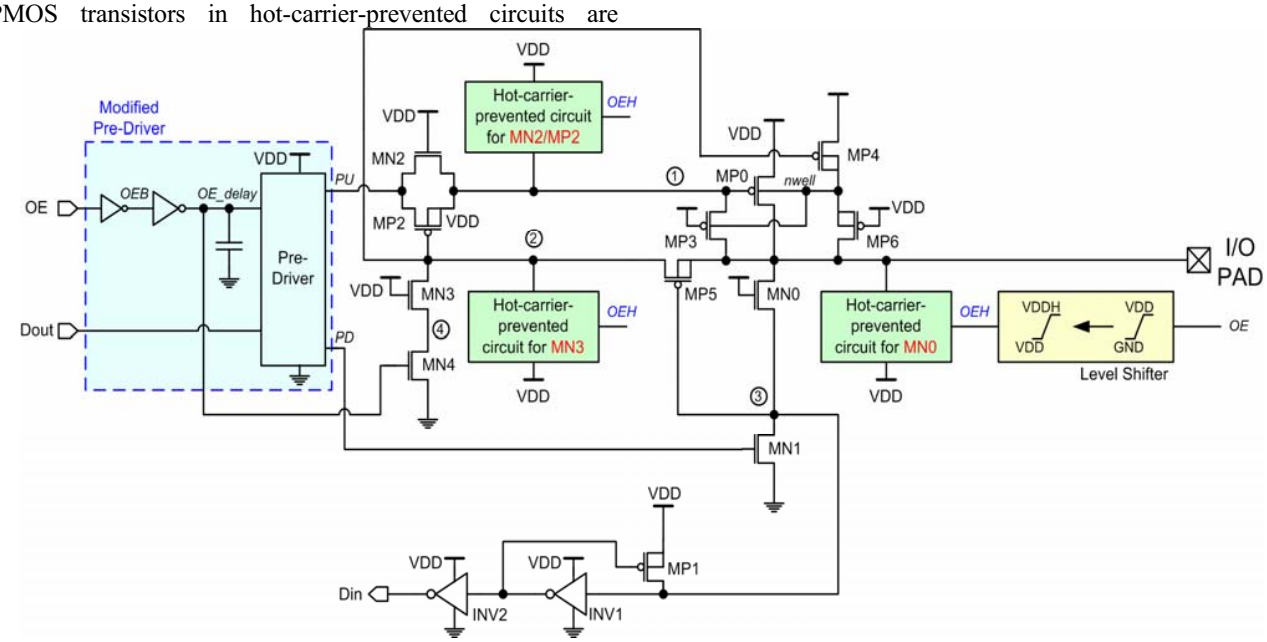
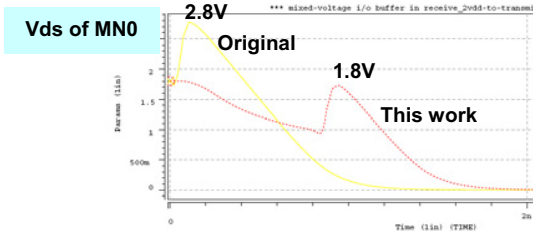
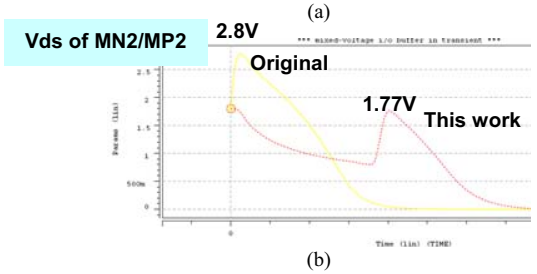


Figure 5. The whole mixed-voltage I/O buffer with the proposed hot-carrier-prevented circuits.

The new proposed 2xVDD-tolerant I/O buffer with the hot-carrier-prevented circuits has been verified by SPICE simulation. The drain-source voltages of the transistors MN0 and MN3 in this new proposed 2xVDD-tolerant I/O buffer are compared to that in the original circuit during the transition from receiving 3.3-V input signal to transmitting 0-V output signal. In Fig. 7(a), the peak of drain-source voltage on MN0 in this work is only ~1.8V, but that of the original design is as high as 2.8V. Besides, the drain-source voltages of the transistor MN2 (or MP2) in this work and the original design during the transient from receiving 3.3-V input signal to transmitting 1.5-V output signal are compared in Fig. 7(b). The drain-source voltage across the transistor MN2 (or MP2) is lower than the maximum operating voltage (1.8V) in the new design (this work). However, that across the transistor MN2 (or MP2) in the original design is still as high as ~2.8V. Therefore, the hot-carrier effect has been suppressed by the proposed hot-carrier-prevented circuits in this work.



(a)



(b)

Figure 7. Comparsions of drain-source voltages (a) across MN0, and (b) across MN2 and MP2, between the original (marked as original) and the new proposed 2xVDD-tolerant I/O buffer with hot-carrier-prevented circuits (marked as this work).

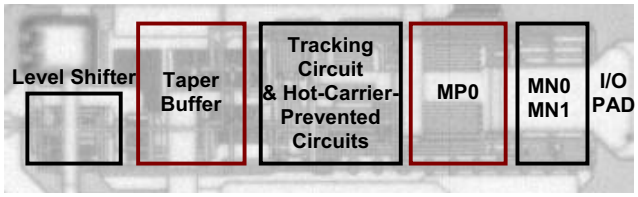
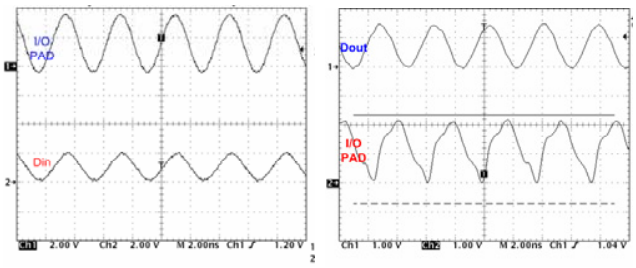


Figure.8 The photograph of 2xVDD-tolerant I/O buffer with the new proposed hot-carrier-prevented circuit in a 0.18-µm 1.8-V CMOS process.

IV. Experimental Results

The new proposed 2xVDD-tolerant I/O buffer with hot-carrier-prevented circuits has been fabricated in a 0.18-µm 1.8-V CMOS process with only thin-oxide (1.8-V) devices. The photograph of fabricated circuit is shown in Fig. 8 with the corresponding circuit blocks. Fig. 9(a) shows the measured waveforms of the proposed 2xVDD-tolerant I/O buffer in the receive mode to receive the 266-MHz input signals with voltage swing of 0-to-3.3V at I/O PAD, where the input data were transmitted to Din with a voltage swing of 0-to-1.5V. Fig. 9(b) shows the measured waveforms in the transmit mode to transmit the 266-MHz signals with a voltage swing of 0-to-1.5V at Dout.



(a) (b)

Figure 9. Measured waveforms of the 2xVDD-tolerant I/O buffer with hot-carrier-prevented circuits operating at 266MHz and VDD of 1.5V, (a) when receiving 0V-to-3.3V input signals at I/O PAD, (b) when transmitting 0V-to-1.5V output signals at I/O PAD.

V. Conclusion

A new 2xVDD-tolerant I/O buffer with hot-carrier-prevented circuits has been successfully verified in a 0.18-µm 1.8-V CMOS process with only thin-oxide devices. The drain-source voltages of transistors in the 2xVDD-tolerant I/O buffer can be kept within the normal operating voltage range (VDD) by the proposed hot-carrier-prevented circuits. This new 2xVDD-tolerant I/O buffer can be operated up to 266MHz to receive 1.5-V/3.3-V input signals or to transmit the 1.5-V output signals, which can meet the high-speed I/O applications of PCI-X 2.0.

References

[1] T. Furukawa, D. Turner, S. Mittl, M. Maloney, R. Serafin, W. Clark, L. Longenbach, and J. Howard, "Accelerated gate-oxide breakdown in mixed-voltage I/O buffers," in *Proc. IEEE Int. Reliability Physics Symp.*, 1997, pp. 169−173.

[2] I.-C. Chen, J. Y. Choi, and C. Hu, "The effect of channel hot-carrier stressing on gate-oxide integrity in MOSFETs," *IEEE Trans. Electron Devices*, vol. 35, pp. 2253−2258, Dec. 1988.

[3] S. Voldman, "ESD protection in a mixed voltage interface and multrial disconnected power grid environment in 0.5- and 0.25-µm channel length CMOS technologies," in *Proc. EOS/ESD Symp.*, 1994, pp. 125−134.

[4] M. J. M. Pelgrom and E. C. Dijkmans, "A 3/5-V compatible buffer", *IEEE J. Solid-State Circuits*, vol. 30, pp. 823-825, July 1995.

[5] M.-D. Ker, S.-L. Chen, and C.-S. Tsai, "Overview and design of mixed-voltage I/O buffers with low-voltage thin-oxide CMOS transistors," *IEEE Trans. on Circuits and Systems I*, vol. 53, no. 9, pp. 1934-1945, Sept. 2006.

[6] M.-D. Ker and S.-L. Chen, "Design of mixed-voltage I/O buffer by using NMOS-blocking technique," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 10, pp. 2324-2333, Oct. 2006.

[7] A.-J. Annema, G. J. G. M. Geelen, and P. C. de Jong, "5.5-V I/O in a 2.5-V 0.25-µm CMOS Technology," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, March 2001.

[8] J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits – A Design Perspective*, 2nd Ed., Pearson Education Inc., 2003.