Design of On-Panel Digital-to-Analog Converter with Reordering Decoder Circuit in LTPS Technology

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An on-panel 6-bit R-string gamma-correction digital-to-analog converter (DAC) with reordering decoder circuit for panel data driver is proposed, which is composed of folded R-string circuit, segmented digital decoder, and reordering decoding circuit. By using the proposed reordering decoder circuit, the area of the proposed circuit is effectively reduced to about one sixth compared with the conventional one in a 3-μm low-temperature poly-Si (LTPS) technology.

1. Introduction

Low-temperature poly-silicon (LTPS) thin-film transistors (TFTs) have been widely used for portable systems, such as digital camera, mobile phone, personal digital assistants (PDAs), notebook, and so on. The electron mobility of LTPS TFTs is about 100 times larger than that of the conventional amorphous silicon TFTs [1], so LTPS technology can achieve slim, compact, and high-resolution display by integrating the driver circuits on peripheral area of display. This LTPS technology will become more suitable for realization of system-on-panel (SOP) applications [2].

The periphery circuit blocks of LCD panel are roughly composed of four parts — display panel, timing control circuit, scan driver circuit, and data driver circuit [3]. Fig. 1 shows the block diagram of the TFT-LCD panel circuits. Display panel is constructed of the active matrix liquid crystals and the operation of the active matrixes is similar to DRAM (dynamic random access memory) which is used to charge and discharge the capacitor of the pixel. Timing control circuit is responsible for transmitting RGB (red, green, and blue) signals to the data driver and controlling the behavior of scan driver.

Scan driver circuit consists of shifter register, level shifter, and digital output buffer. Shifter register is used to store digital input signals then transit to the next stage according to timing control circuit. The purpose of the level shifter is to convert the digital signal to higher voltage level. Finally, since the scan lines can be modeled as RC (resister and capacitor) ladder, the digital output buffer should be used in the last stage for driving the large load.

Data driver circuit is composed of shifter register, data latch, level shifter, digital-to-analog converter (DAC), and analog output buffer. Shifter register and data latch manage to transit and store the RGB signals. Also, the purpose of level shifter is the same as the one in scan driver circuit, which is applied to translate the RGB signal to a higher level voltage. In addition, digital-to-analog converter is used to convert the digital RGB signal to analog gray level. The analog output buffer is applied to drive active pixels into a desired gray level. However, the LCD panel usually has large load, especially in larger panel display or higher resolution display, so the analog output buffer should enhance the driving capability of the data driver.

Currently, LTPS technology has a tendency towards integrating all control circuits and driver circuits on the glass substrate [4], [5]. However, the poly-Si TFTs suffered poor uniformity with large variations on the device characteristics due to the narrow laser process window for producing large-grained poly-Si TFTs. The device variation becomes a serious problem for analog circuit realization on the LCD panel [6]. For this reason, the design of on-panel analog circuits is a challenge for SOP applications.

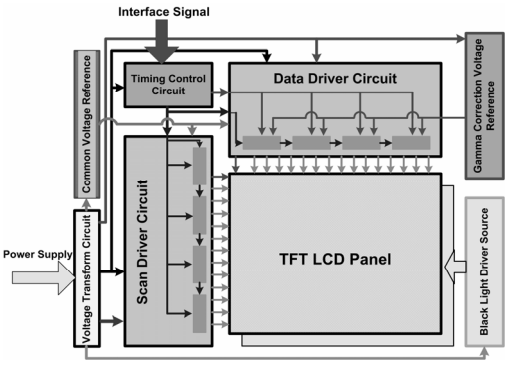

Fig. 1. The block diagram of TFT-LCD panel circuits.

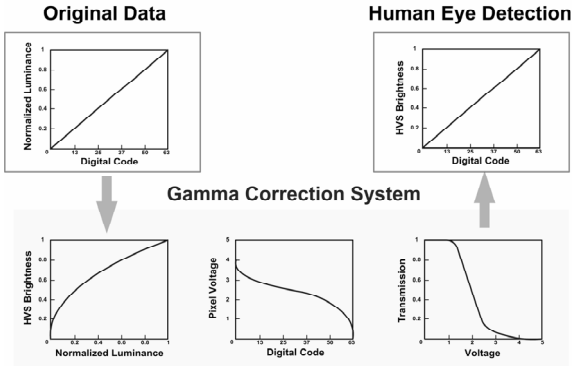

Fig. 2. The operation of the gamma correction for the normally white TN type LCD panel [3].

In this paper, an on-panel 6-bit R-string gamma-correction digital-to-analog converter (DAC) with reordering decoder circuit for panel data driver is proposed, which can reduce the area and complexity of the DAC on-glass substrate. Therefore, the proposed DAC circuit is beneficial for data driver to be integrated in the peripheral area of TFT-LCD panels in LTPS process.

2. Gamma Correction and Digital-to-Analog Converter

Gamma Correction

Gamma correction of liquid crystal displays is involved due to the nonlinearity between luminance and human visual system (HVS). The pupils of the human's eyes would vary automatically for the change of the ambient light. For this reason, a data driver with gamma correction is necessary in TFT-LCD panel. The data driver circuit is often required to compensate for the human visual system's transfer function. Moreover, it must also compensate for the LCD transfer function. Fig. 2 shows the operation of the gamma correction for the normally white TN type LCD panel [3]. The gamma correction system is composed of three relationships: luminance vs. HVS brightness, input digital code vs. pixel voltage, and the V-T curve of the NW-TN type liquid crystal. In general, the input digital codes (media codes) are designed to be direct proportion to brightness in human eye linear with this system. In data driver circuit, DAC is used to convert the digital RGB signal to analog gray level, so Gamma Correction System in Fig. 2 can be implemented by DAC with gamma.

Digital-to-Analog Converter

Fig. 3 shows a traditional 6-bit R-string DAC circuit [7]. The architecture of this DAC requires no digital decoders and is usually used in LCD data drivers, because this architecture is simple for gamma correction design. However, the area of such traditional switch array becomes larger and larger, if the resolution of DAC becomes higher. The load at the output node (Vout) also becomes larger due to the huge switch array in the traditional design.

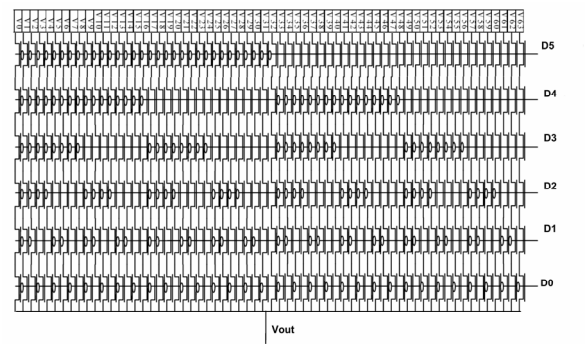

Fig. 3. A traditional 6-bit R-string DAC with switch array decoding [7].

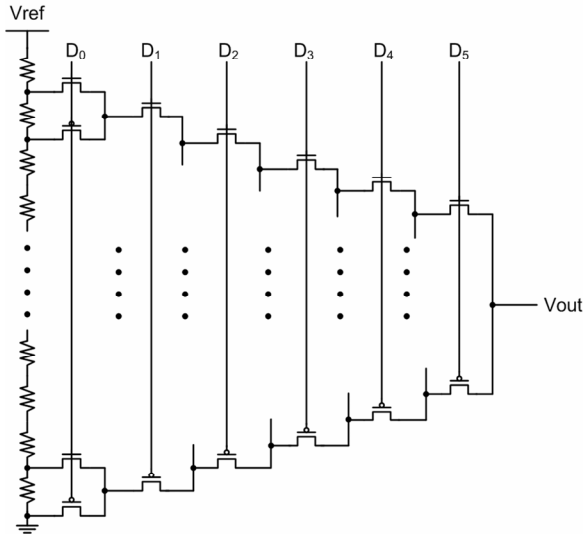

Fig. 4. A 6-bit R-string DAC with binary-tree decoding [8].

Fig. 4 shows a 6-bit R-string DAC with binary-tree decoding [8]. This architecture also requires no digital decoders. In opposition to the R-string DAC with switch array decoding, this circuit has less transistors in the decoding circuits. Nevertheless, the speed of this circuit is limited by the delay through the switch network. The timing skew among the switch-controlling signals results in large glitches at Vout. This circuit also has larger RC-type load at the output node (Vout) due to the binary-tree switches.

For higher-speed applications, Fig. 5 shows a modified 6-bit R-string DAC with digital decoding [9]. The load of the output node can be reduced by the digital decoder, because the output node is only connected to one column of analog switches. The operational speed of this DAC using digital decoding is faster than that using binary-tree decoder in Fig. 4. This architecture is also more suitable for gamma correction design because it is easy to produce different sections in the resistor string. However, the area and complexity of the decoder circuits become larger and larger, if the resolution becomes higher. For this reason, this R-string DAC with digital decoding is not good enough for integrating the data

driver in the higher resolution TFT-LCD panels.

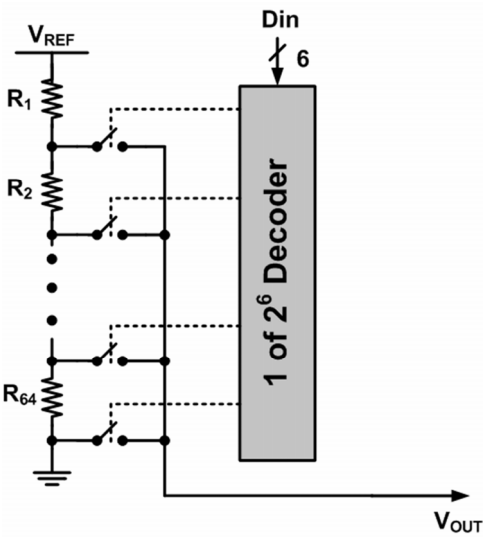

Fig. 5. A modified 6-bit R-string DAC with digital decoding [9].

3. New Folded R-String Gamma-Correction DAC with Reordering Decoding Circuit

Fig. 6 shows the new proposed folded R-string gamma-correction DAC with reordering decoding circuit for panel data driver in LTPS technology. The lower area and lower complexity can be achieved in this new design. The modified DAC is composed of folded R-string circuit, switch array, two identical segmented decoders, and reordering decoding circuit. The input signal Din is segmented into two parts (MSBs and LSBs). The MSBs and the LSBs of the input signal are assigned to two identical segmented decoders. The output signal of one decoder turns on the switches on the top row of the switch array while the other decoder turns on the switches in the reordering decoding circuit. Therefore, the output voltage (Vo) matches correct gray level.

For a 6-bit R-string DAC with gamma correction design, the transform function of this system is shown in Fig. 7 [3]. The nonlinearity between gray level domain and luminance domain can be corrected by gamma correction design. For a 6-bit gamma correction, the transform function of this system can be expressed as following

$$\frac{T(GL)-T_{\min}}{T_{\max}-T_{\min}}=(GL/63)^{\gamma}, \quad (1)$$

$$L(GL)=T(GL)\times K_{backlight}. \quad (2)$$

Pixel value can be derived with gamma value of 2.2 by using the transform function with proper resistance ratio. The proposed DAC circuit has been fabricated in 3-μm LTPS technology. The simulation result of this DAC, assigned a series of digital input codes from 000000 (GL=0) to 111111 (GL=63) at 100-kHz operation frequency, is shown in Fig. 8. The spike of the proposed DAC is small during transition of digital input code at 100-kHz operation frequency.

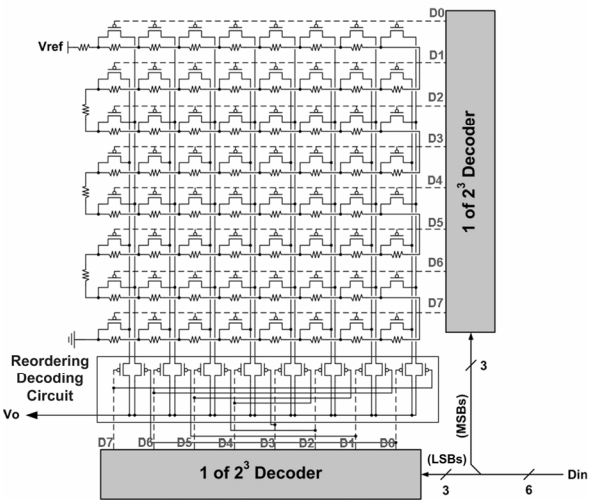

Fig. 6. The proposed on-panel folded R-string gamma-correction DAC with reordering decoding circuit for panel data driver in LTPS technology.

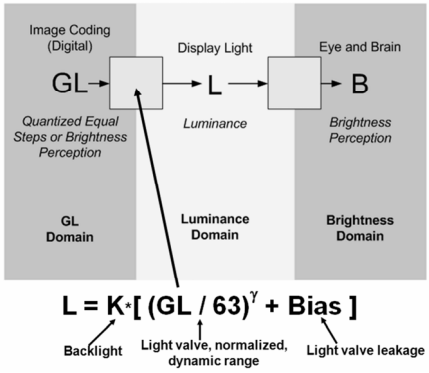

Fig. 7. The transform function of display system.

With the R-string approach, the DAC has guaranteed monotonicity and also has higher accuracy, because the accuracy of the R-string DAC is dependent on the ratio of resistors, not dependent on absolute resistor values. Furthermore, the area of the proposed folded R-string DAC with gamma correction is smaller because the reordering decoding circuit can simplify the decoder circuit. The partial decoding function is replaced by the signal paths routing of the reordering decoding circuit. For this reason, the fundamental decoders can be utilized for the two identical segmented digital decoders.

The 1 of 26 Decoder in the design of Fig. 5 needs 64 6-input NAND gates and 6 inverters, while the 1 of 23 Decoder in the new proposed design of Fig. 6 only needs 8 3-input NAND gates and 3 inverters. Therefore, the total transistors of the decoders can be decreased from 780 to 124 in such a 6-bit DAC. The area of the R-string DAC can be effectively reduced to about one sixth of the traditional one by using this proposed architecture. This new proposed 6-bit folded R-string gamma-correction DAC with reordering decoding circuit is also more suitable for different gamma correction in TFT-LCD panels.

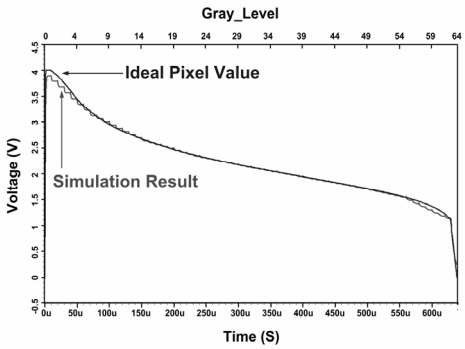

Fig. 8. The simulation result of on-glass 6-bit folded R-string gamma-correction DAC with reordering decoding circuit in 3-μm LTPS technology at 100-kHz operation frequency.

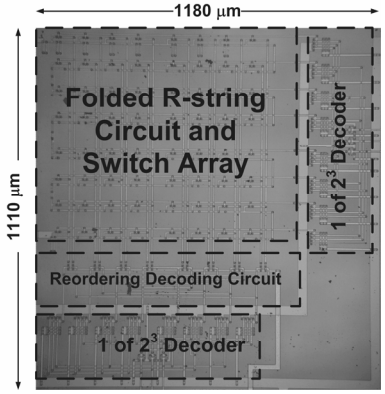

Fig. 9. The die photo of on-glass folded R-string gamma-correction DAC with reordering decoding circuit realized in 3-μm LTPS process.

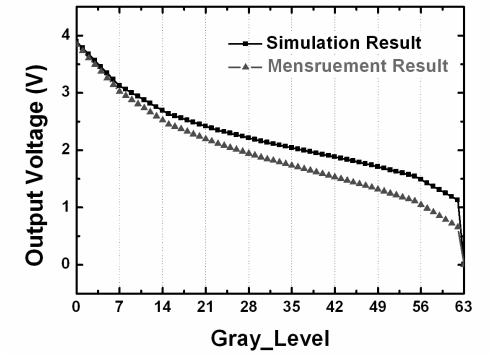

Fig. 10. The measurement result of output voltage in fabricated on-glass folded R-string gamma-correction DAC with reordering decoding circuit in 3-μm LTPS process.

4. Experimental Results

The proposed on-panel folded R-string gamma-correction DAC with reordering decoding circuit for panel data driver has been designed and fabricated in a 3-μm LTPS process. The die photo of the fabricated circuit is shown in Fig. 9, where the area is 1110μm x 1180μm. Fig. 10 shows the measurement result of output voltage in the folded R-string DAC with gamma correction in 3-μm LTPS process. With the transform function and proper resistance ratio, the simulation result similar to ideal pixel value is with gamma value of 2.2. However, the measurement result is not well consistent with the simulation result due to the variation of on-glass resistance in LTPS process. Suitable adjustment on the resistance of R-string in the LTPS process, a precise result of the proposed on-glass DAC can be achieved.

5. Conclusions

An on-panel 6-bit folded R-string gamma-correction DAC with reordering decoding circuit has been successfully designed and fabricated in 3-μm LTPS technology. By using the folded R-string circuit, segmented digital decoders, and reordering decoding circuit, the area of the fabricated circuit can be effectively reduced to about one sixth of the conventional one. Furthermore, the proposed architecture is also more suitable for gamma correction design in different kinds of LTPS processes. This new proposed architecture can be applied to different kinds of gamma value and normally white (or black) TFT-LCD panels by modifying the corresponding R-string value and the decoder.

Acknowledgments

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