Transient-to-Digital Converter for ESD Protection Design in Microelectronic Systems

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***Abstract* - An on-chip transient-to-digital converter for system-level electrostatic discharge (ESD) protection is proposed. The proposed transient-to-digital converter is designed to detect fast electrical transients during the system-level ESD events. The output digital thermometer codes can correspond to different ESD voltages under system-level ESD tests. The experimental results in a 0.18-μm CMOS integrated circuit (IC) with 3.3-V devices have confirmed the detection function and digital output codes.**

I. Introduction

The reliability issue of system-level electrostatic discharge (ESD) events has attracted more attentions than before in the state-of-the-art circuits and systems [1]. This tendency results from not only the progress of more functions integrated into a single chip but also from the strict requirements of reliability test standards, such as the system-level ESD test. The microelectronic product must sustain the ESD level of ±8kV (± 15kV) under contact-discharge (air-discharge) test mode to achieve the immunity requirement of "level 4" in the IEC 61000-4-2 test standard [2]. During system-level ESD test, the power and ground lines of the CMOS integrated circuit (IC) in the microelectronic products no longer maintained their normal voltage levels, but an underdamped sinusoidal voltage with the amplitude of several tens volts occurred. Such high-energy ESD-induced noises often cause damage or malfunction to CMOS ICs inside the equipment under test (EUT). It has been also reported that some CMOS ICs are very susceptible to system-level ESD stress [3]-[5], even though they have passed the component-level ESD specifications such as human-body-model (HBM) of ±2kV, machine-model (MM) of ±200V, and charged-device-model (CDM) of ±1kV.

In order to solve such system-level ESD issues, the traditional solution is to add some board-level discrete components or board-level noise filters into the microelectronic products to decouple, bypass, or absorb the electrical transients under system-level ESD tests [6], [7]. The noise filter networks, such as the capacitor filter, ferrite bead, LC-like, and π–section filters, can be used to enhance the system-level ESD immunity. However, such additional discrete components may not be integrated into a single chip due to the limitation of chip area and substantially increase the total cost of microelectronic products. Therefore, the chip-level solutions to meet high system-level ESD specification for microelectronic products without using additional discrete noise-bypassing components on the PCB are highly requested by IC industry [8].

In this paper, a novel transient-to-digital converter composed of transient detection circuits is proposed to detect the fast electrical transients and convert to digital thermometer codes under the system-level ESD stress. The test chip fabricated in a 0.18-μm CMOS process has verified that the proposed on-chip transient-to-digital converter can successfully transfer different ESD voltage levels into digital thermometer codes.

II. Transient Detection Circuit

A. Circuit Structure

Fig. 1 shows the proposed on-chip transient detection circuit. The RC-based circuit structure is designed to realize the transient detection function. The two-inverter latch (INV_2 and INV_3) is designed to memorize the logic state before and after system-level ESD stress. The NMOS (M_{nr}) is used to provide the initial reset function to set the initial output voltage (V_{OUT}) level to 0V. In Fig. 1, the node V_X is biased at V_{DD} and the node V_G is biased at V_{SS} during the normal operation condition. Under the system-level ESD tests, the ESD voltage has fast rise time in the order of nanosecond (ns). The voltage level of V_X has much slower voltage response than the voltage level at V_{DD} because the RC circuit has a time constant in the order of microsecond (μs). Due to the longer time delay of the voltage increase at the node V_X, the PMOS device in the inverter1 (INV_1) can be turned on by the overshooting ESD voltage and conducts a voltage to the node V_G to further turn on the M_{n1} device. The turned-on M_{n1} device can pull down the output voltage level at the node V_A. Therefore, the logic level stored in the two-inverter latch can be changed due to the system-level ESD event. The output voltage (V_{OUT}) of the proposed on-chip transient detection circuit is finally changed from 0V to 3.3V to memorize the occurrence of system-level ESD events.

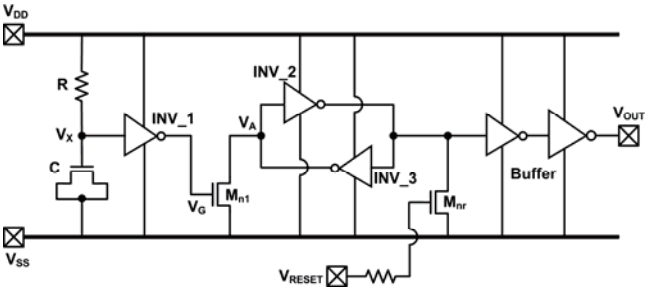

Fig. 1. The proposed on-chip transient detection circuits realized with RC-delay and NMOS-reset function.

B. Measurement Setup

In the test standard of IEC 61000-4-2 [2], two test modes have been specified: air-discharge test mode and contact-discharge test mode. Fig. 2 shows the measurement setup of the system-level ESD test with indirect contact-discharge test mode, which consists of a wooden table on the grounded reference plane (GRP). In addition, an isulation plane is used to isolate the EUT from horizontal coupling plane (HCP). The HCP are connected to the GRP with two 470kΩ resistors in series.

With the measurement setup shown in Fig. 2, the transient responses on power lines of CMOS ICs inside EUT can be further analyzed and recorded by digital oscilloscope. Thus, the circuit performance of the proposed on-chip transient detection circuit and transient-to-digital converter can be evaluated through this measurement setup.

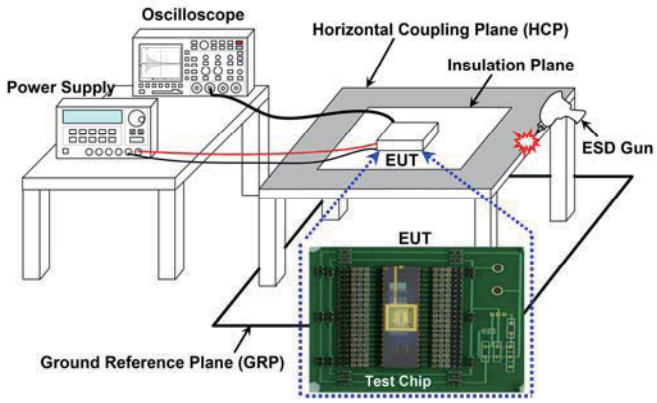

Fig. 2. Measurement setup for system-level ESD test with indirect contact-discharge test mode.

C. Measurement Results

The circuit performance of the on-chip transient detection circuit under the system-level ESD test has been verified in a silicon chip fabricated in 0.18-μm CMOS process with 3.3-V devices. The system-level ESD test with indirect contact-discharge test mode is used to experimentally verify the detection performance of proposed on-chip transient detection circuit. Under both positive and negative system-level ESD stress conditions, the measured V_{DD} and V_{OUT} transient response can be recorded by the oscilloscope. This can clearly indicate whether the proposed on-chip transient detection circuit works correctly during the system-level ESD tests.

The measured V_{DD} and V_{OUT} waveforms of the proposed on-chip transient detection circuit with ESD voltage of +0.2kV zapping on the HCP under system-level ESD test are shown in Fig. 3(a). As shown in Fig. 3(a), under the system-level ESD test with positive ESD voltage, V_{DD} begins to increase rapidly from 3.3V. Meanwhile, V_{OUT} begins to greatly increase with positive-going underdamped sinusoidal voltages on V_{DD} power line. Finally, the output voltage (V_{OUT}) of the on-chip transient detection circuit is changed from 0V to 3.3V. As a result, the on-chip transient detection circuit can memorize the occurrence of the system-level ESD event with positive ESD voltage. The experimental result in Fig. 3(a) can be further analyzed by using the HSPICE simulator.

The measured V_{DD} and V_{OUT} transient waveforms of the proposed on-chip transient detection circuits with ESD voltage of -0.2kV zapping on the HCP under system-level ESD test are shown in Fig. 3(b). As shown in Fig. 3(b), under the system-level ESD test with negative ESD voltage, V_{DD} begins to decrease rapidly from 3.3V. V_{OUT} is disturbed simultaneously with negative underdamped sinusoidal voltages on V_{DD} power line. Finally, V_{OUT} is pulled up from 0V to the 3.3V after the system-level ESD test with negative ESD voltage. The experimental result in Fig. 3(b) can be further analyzed by using the HSPICE simulator.

From the system-level ESD test results, with positive-going and negative-going underdamped sinusoidal voltages coupled on V_{DD} power lines, the output voltages (V_{OUT}) of the on-chip transient detection circuit can both change from 0V to a stable voltage of 3.3V. Therefore, the proposed on-chip transient detection circuit can memorize the occurrence of the system-level ESD events with positive and negative ESD voltages.

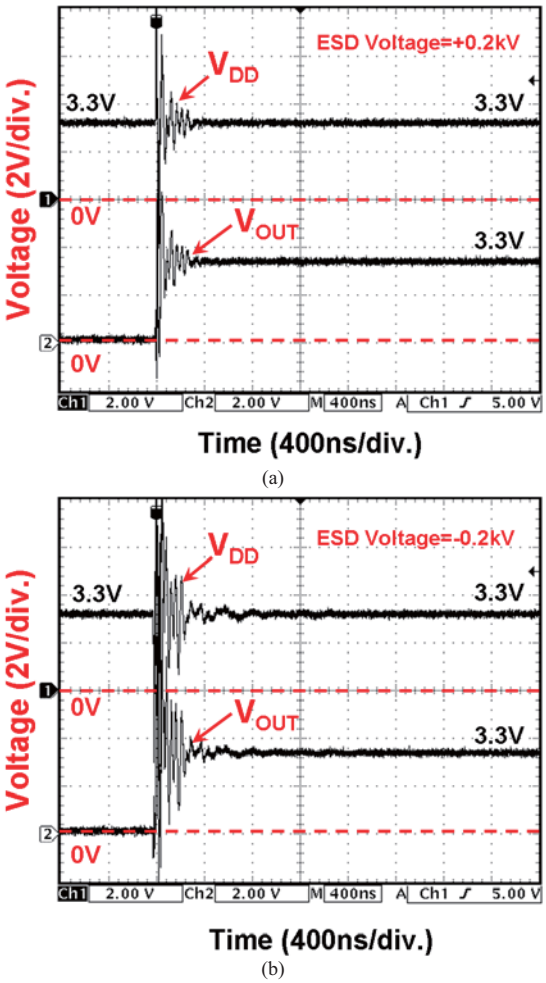

Fig. 3. Measured V_{DD} and V_{OUT} transient responses with ESD voltage of (a) +0.2kV, and (b) -0.2kV, zapping on the HCP under system-level ESD test.

III. Transient-to-Digital Converter

A. Circuit Structure

It has been investigated that noise filter networks can enhance susceptibility of CMOS ICs to system-level ESD test by decoupling, bypassing, or absorbing ESD-induced noise voltage (energy). It has also been reported that the noise filter networks have strong impacts to the parameters of the underdamped sinusoidal voltage such as transient peak voltage, damping frequency, and damping factor [7].

Fig. 4 shows the proposed transient-to-digital converter consisted of four transient detection circuits with four different RC filter networks. The RC filter network is realized with one decoupling capacitor and two resistors with equal value to provide the noise filter function during system-level ESD stresses. The RC noise filter network can suppress the transient peak voltages on V_{DD} and V_{SS}, which has influence on positive and negative system-level ESD voltages to cause transition at the output (V_{OUT}) of the proposed on-chip transient detection circuit. For the proposed transient-to-digital converter, with different R and C values in the filter networks, different ESD levels on V_{DD} and V_{SS} will reach to each transient detection circuit. Under the system-level ESD zapping conditions, the four transient detection circuits will have different output voltage responses. Therefore, by combining with different RC noise filter networks, the proposed transient-to-digital converter can be designed to detect different ESD voltage levels and transfer output voltages into digital thermometer codes under system-level ESD stress.

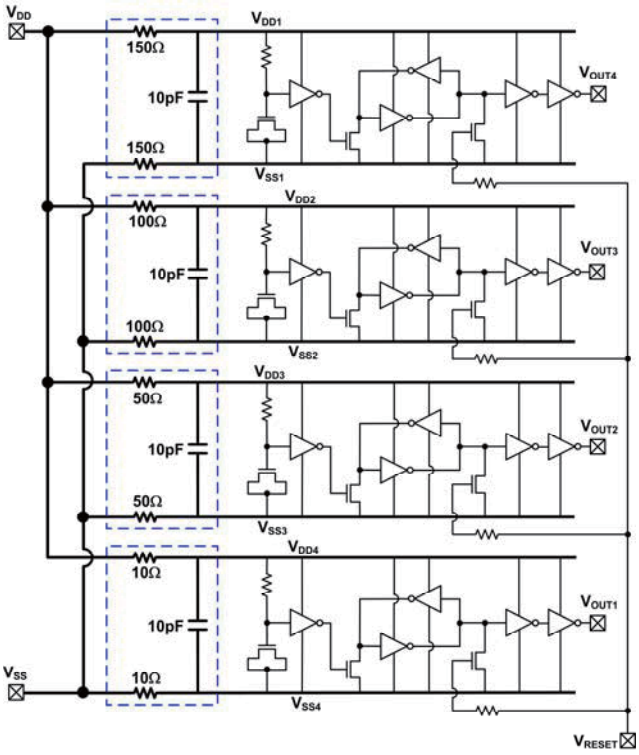

Fig. 4: The proposed 4-bit transient-to-digital converter realized with four transient detection circuits and four RC filter networks.

B. Measurement Results

The measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} waveforms of the proposed transient-to-digital converter under system-level ESD test with ESD voltage of +0.8kV zapping on the HCP are shown in Fig. 5(a). During the fast transient of ESD stress, V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} are disturbed simultaneously during V_{DD}/V_{SS} disturbance. Finally, V_{OUT1} will be changed from 0V to 3.3V, while V_{OUT2}, V_{OUT3}, and V_{OUT4} are still kept at 0V. Therefore, under system-level ESD test with ESD voltage of +0.8kV zapping, the detection output voltages can be transferred into a digital thermometer code of "0001."

Under system-level ESD test with ESD voltage of +1.2kV zapping on the HCP, V_{OUT1} and V_{OUT2} are pulled up from 0V to 3.3V, while V_{OUT3} and V_{OUT4} are still kept at 0V. Therefore, under system-level ESD test with ESD voltage of +1.2kV zapping condition, the output voltages can be transferred into a digital thermometer code of "0011.".

Under system-level ESD test with ESD voltage of +1.8kV zapping on the HCP, V_{OUT1}, V_{OUT2}, and V_{OUT3} will be changed from 0V to 3.3V, while V_{OUT4} is still kept at 0V. Therefore, with ESD voltage of +1.8kV zapping, the detection results can be transferred into a digital thermometer code of "0111."

The measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} waveforms of the proposed transient-to-digital converter under system-level ESD test with ESD voltage of +3.1kV zapping on the HCP are measured in Fig. 5(b). During the high-energy fast transient of ESD stress, all transient detection circuits can detect the occurrence of disturbance on V_{DD}/V_{SS}. Finally, when V_{DD} finally returns to its normal stable voltage level of 3.3V, V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} have been all changed from 0V to 3.3V, as shown in Fig. 5(b). Therefore, with ESD voltage of +3.1kV zapping, the detection results s can be transferred into a digital thermometer code of "1111."

Fig. 6 depicts the ESD voltage to digital code characteristic of the proposed transient-to-digital converter. With larger ESD voltage level under system-level ESD tests, the transferred digital thermometer code goes higher, as shown in the inset table in Fig. 6.

C. Application in Microelectronic Systems with Hardware/Firmware Co-design

The proposed on-chip transient-to-digital converter can be co-designed with firmware to provide a system solution to solve the system-level ESD event on microelectronic products equipped with CMOS ICs.

Under the normal power-on condition, the V_{DD} power-on voltage waveform has a rise time on the order of a millisecond (ms). The power on reset circuit can send the power-on signal for a microelectronic system to execute a normal reset procedure. Under the system-level ESD zapping with a low ESD voltage, the output digital code of the proposed on-chip transient-to-digital converter becomes "0001." Then, the firmware can execute the partial system recover procedure to check and to recover partial electrical functions of microelectronic system, as shown in Fig. 7(a). Under the system-level ESD zapping with high enough ESD voltage, the output digital code of the proposed on-chip transient-to-digital

converter becomes "1111." Then, the firmware can execute the recover procedure to recover all the electrical functions to a desired stable state as soon as possible, as shown in Fig. 7(b). The firmware can be designed to execute different recover procedures with different digital codes. After the recover procedures, the output digital code of the proposed on-chip transient-to-digital converter is again reset to "0000" for detecting the next transient ESD events.

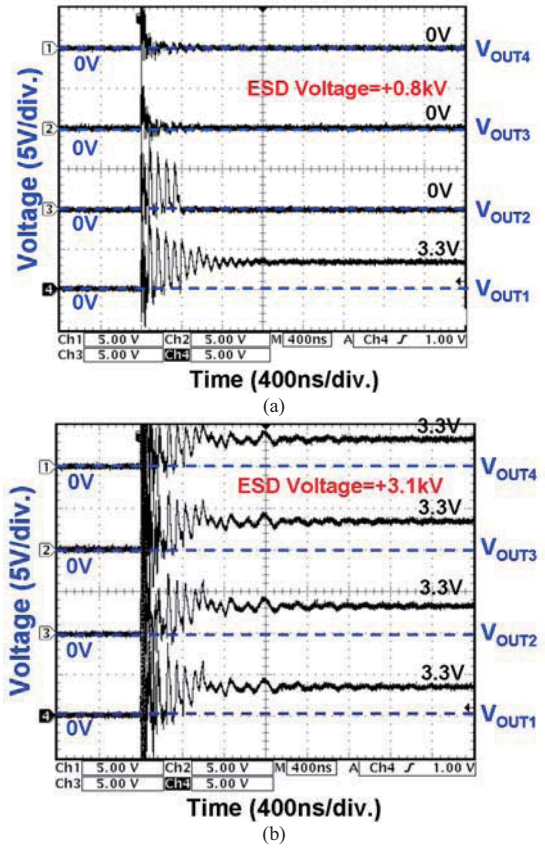

Fig. 5: Measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} transient voltage waveforms under system-level ESD test with ESD voltage of (a) +0.8kV and (b) +3.1kV, zapping on the HCP.

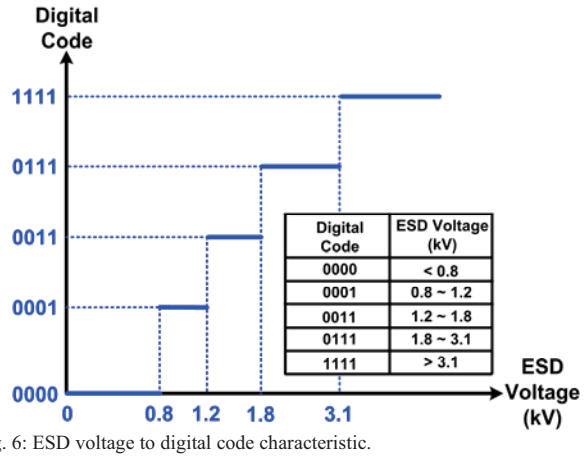

Fig. 6: ESD voltage to digital code characteristic.

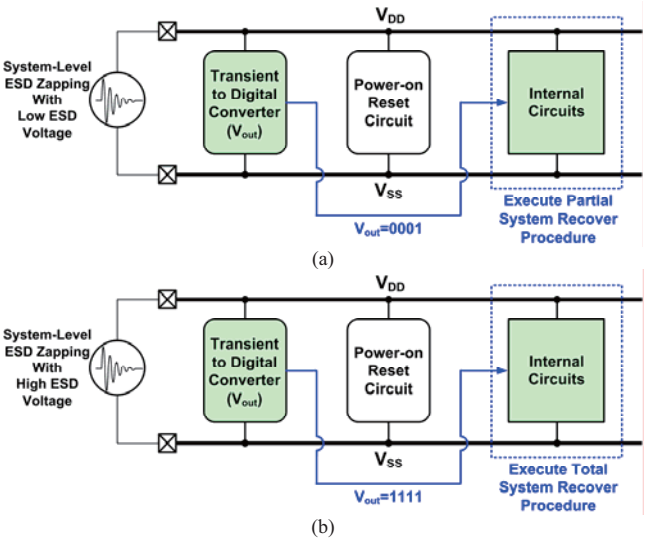

Fig. 7: Hardware/firmware operation during (a) low system-level ESD zapping and (b) high system-level ESD zapping.

IV. Conclusions

A novel transient-to-digital converter composed of four transient detection circuits and four different RC filter networks has been successfully designed and verified in a 0.18-μm CMOS process with 3.3-V devices. The output digital thermometer codes of the proposed transient-to-digital converter correspond to different ESD voltages under system-level ESD tests. These output digital thermometer codes can be used as the firmware index to execute different system recovery procedure of microelectronic products. Thus, the proposed transient-to-digital converter can be further combined with firmware co-design to provide an effective solution to solve the system-level ESD protection issue in microelectronic systems equipped with CMOS ICs.

References

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