

An ESD-Protected 5-GHz Differential Low-Noise Amplifier in a 130-nm CMOS Process

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Abstract- A novel ESD protection design for radio-frequency (RF) differential input/output (I/O) pads is proposed and successfully applied to a 5-GHz differential low-noise amplifier (LNA) in a 130-nm CMOS process. In the proposed ESD protection design, an ESD bus and a local ESD clamp device are added between the differential input pads to quickly bypass ESD current, especially under the pin-to-pin ESD-stress condition. With 10.3-mW power consumption under 1.2-V power supply, the differential LNA with the proposed ESD protection design has the human-body-model (HBM) ESD robustness of 3 kV, and exhibits 18-dB power gain and 2.62-dB noise figure at 5 GHz. Experimental results have demonstrated that the proposed ESD protection circuit can be co-designed with the input matching network of LNA to simultaneously achieve excellent RF performance and high ESD robustness.

I. INTRODUCTION

Radio-frequency integrated circuits (RF ICs) are used in a lot of portable electronics devices for wireless communications. Recently, the feature size of MOS transistor in CMOS processes has been continuously scaled down to improve its high-frequency characteristics, which makes them more attractive to implement RF ICs. With the advantages of high integration capability and low cost for mass production, RF ICs operating in giga-Hz frequency bands have been fabricated in CMOS technology. In an RF receiver, low-noise amplifier (LNA) plays a very important role because it is the first stage in the RF receiver. Differential configuration is popular for LNA design because differential LNA has the advantages of common-mode noise rejection, less sensitivity to substrate noise/supply noise, and less bond-wire inductance variation [1]. In addition, the differential output signals of the differential LNA can be directly connected to the differential inputs of the double balanced mixer.

Electrostatic discharge (ESD), which has been the most important reliability issue in IC industry, is getting more attention in nanoscale CMOS technology. With the advances of CMOS processes, ESD robustness of CMOS ICs becomes worse because of the thinner gate oxide of MOS transistors. Since the input of LNA is usually connected to the external node of RF receiver chip such as the off-chip antenna, on-chip ESD protection circuits are needed for all input pads of LNA. However, applying ESD protection circuits at the input pads inevitably introduce impacts to RF performance. Therefore, LNA and ESD protection circuit have to be co-designed to simultaneously optimize RF performance and ESD robustness.

Recently, several ESD-protected LNAs in CMOS processes have been reported [2]-[6]. The typical ESD protection design with diodes at the input pad and the power-rail ESD clamp circuit had been verified [2]. Besides diodes, the inductor-based ESD-protected LNA had been proposed [3]. The inductor serves as part of the input matching network and provides ESD current path. With the parallel LC network resonating at the RF operation frequency, the shunt impedance of the ESD protection circuit becomes very large to mitigate the RF performance degradation [4]. Moreover, the LC-tanks, which resonate at the RF operation frequency, can be used between input pad and VDD, as well as between input pad and VSS, respectively [5]. In addition to single-ended LNA, ESD protection design for differential LNA had also been reported, recently [6].

In this paper, a novel ESD protection design for differential input/output (I/O) pads is proposed. Applied to a 5-GHz differential LNA, the ESD-protected LNA has been designed and successfully verified in a 130-nm CMOS process. The reference differential LNA without ESD protection was also designed and fabricated in the same wafer for comparison. Moreover, the pin-to-pin ESD stress on differential LNAs, which was never mentioned in the previous works, is first studied in this work.

II. DESIGN OF DIFFERENTIAL LNA

The circuit schematic of the differential LNA without ESD protection is shown in Fig. 1. The architecture of common-source with inductive degeneration is applied to match the source impedance ($50\ \Omega$) at the resonant frequency of 5 GHz. Cascode configuration provides good stability and reduces the Miller effect [7]. With the input matching network resonating at the RF operation frequency, the input impedance is purely real and proportional to the inductance of source inductor L_{S1} (L_{S2}). Therefore, input impedance matching can be achieved by choosing appropriate inductance for L_{S1} and L_{S2} . After the inductance of L_{S1} (L_{S2}) is determined, the remaining capacitive impedance needs to be cancelled by the inductance of gate inductor L_{G1} (L_{G2}). The drain inductor L_{D1} (L_{D2}) and drain capacitor C_{D1} (C_{D2}) form the output matching network. The LC-tank consisting of L_{TANK} and C_{TANK} is used to enhance the common-mode rejection. NMOS transistors M_1 - M_4 are fully silicided. All devices in Fig. 1 except the bias tee were fully integrated in the experimental test chip.

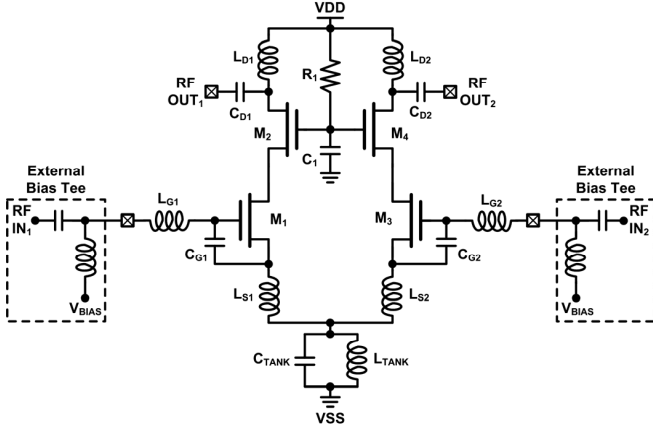


Fig. 1. Circuit schematic of differential LNA without ESD protection.

III. ESD PROTECTION DESIGN FOR DIFFERENTIAL LNA

A. ESD Protection Device

Silicon-controlled rectifier (SCR) is suitable for ESD protection design for RF ICs, because it has the features of high ESD robustness and low parasitic capacitance under a small layout area [8]. Besides, SCR had been demonstrated to be the optimum ESD protection device for high-speed differential I/O pads [9]. The P-type substrate-triggered SCR (P-STSCR) is utilized in this work to protect the LNA against ESD stresses. The cross-sectional view of the P-STSCR is shown in Fig. 2(a). The SCR path exists among the P+ diffusion (anode), N-well, P-well, and N+ diffusion (cathode). The equivalent circuit of the P-STSCR is shown in Fig. 2(b), which consists of a parasitic vertical PNP BJT and a parasitic lateral NPN BJT. The PNP BJT Q_{PNP} is formed by the P+ diffusion (anode), N-well, and P-well. The NPN BJT Q_{NPN} is formed by the N-well, P-well, and N+ diffusion (cathode).

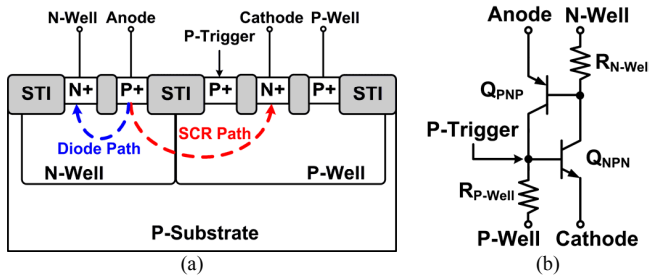


Fig. 2. (a) Cross-sectional view of P-STSCR. (b) Equivalent circuit of P-STSCR.

To quickly turn on the P-STSCR during ESD stresses, the P+ trigger diffusion (in the P-well region) was added between the anode and cathode. An ESD detection circuit was designed to inject trigger current to the P-trigger node during ESD stresses. After the trigger current is injected into the P-trigger node, the SCR is turned on to bypass ESD current. Since the holding voltage (2.58 V at 85 °C) of the SCR in this work is larger than the supply voltage of 1.2 V, the SCR can be safely used without latchup issue.

B. Differential LNA With Proposed ESD Protection Design

The schematic of differential LNA with the proposed ESD protection design is shown in Fig. 3. An ESD bus is inserted between the differential input pads and VDD. The anode of P-STSCR₁ is connected to the ESD bus with its cathode grounded. A P-diode is connected between each input pad and the anode of P-STSCR₁, whereas an N-diode is connected between VSS and each input pad. With the N-well of P-STSCR₁ directly connected to VDD, ESD current paths from the input pads to VDD can be established. Besides, a power-rail ESD clamp circuit was also designed to provide ESD current path between VDD and VSS to achieve comprehensive whole-chip ESD protection [10]. The power-rail ESD clamp circuit consists of an RC timer, an inverter, and an ESD clamp device realized by another SCR (P-STSCR₂). During ESD stresses, when ESD voltage is coupled to VDD, RC delay causes the PMOS in the inverter to be turned on and therefore to inject trigger current to turn on P-STSCR₁ and P-STSCR₂. Under normal circuit operating conditions, the output of inverter is kept at low (0 V) to turn off P-STSCR₁ and P-STSCR₂.

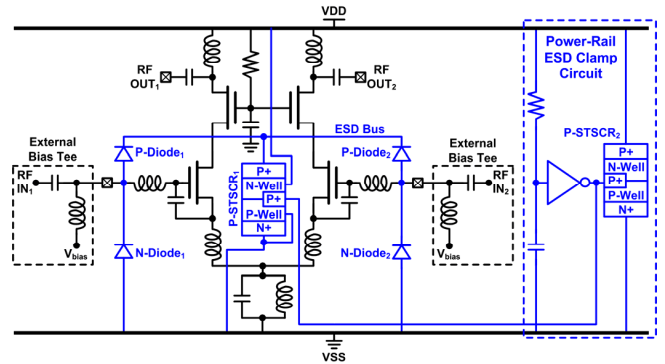


Fig. 3. Circuit schematic of differential LNA with the proposed ESD protection design.

IV. EXPERIMENTAL RESULTS

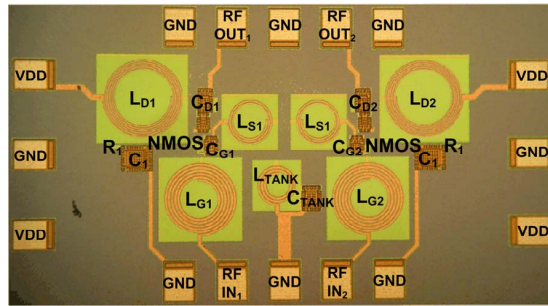
The differential LNAs without ESD protection and with the proposed ESD protection design have been fabricated in the same wafer in a 130-nm CMOS process to compare their performance. The chip microphotographs of the differential LNAs without ESD protection and with the proposed ESD protection design are shown in Figs. 4(a) and 4(b), respectively. The differential LNA without ESD protection occupies the area of 1070 $\mu\text{m} \times 630 \mu\text{m}$, and the circuit area of the differential LNA with the proposed ESD protection design is 1090 $\mu\text{m} \times 750 \mu\text{m}$. Both LNA consume 10.3 mW under 1.2-V power supply because the ESD protection circuit does not consume any DC power.

A. RF Performance

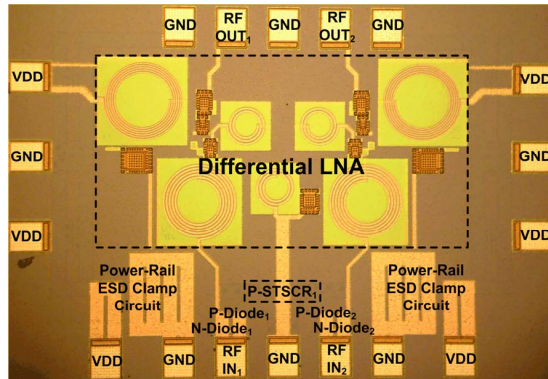
Fig. 5(a) shows the measured S21-parameters of the fabricated LNAs. Both LNAs have their best S-parameters around 5 GHz. The power gain of the differential LNA without ESD protection is 16.2 dB at 5 GHz, while the

differential LNA with the proposed ESD protection design exhibits 18-dB power gain. The measured S11-parameters are compared in Fig. 5(b). Both of the fabricated LNAs have the S11-parameters of less than -25 dB at 5 GHz. The differential LNAs without ESD protection and with the proposed ESD protection design achieve best input matching at the same frequency, which demonstrates that no shift in the center operation frequency can be achieved after adding ESD protection circuits as long as the parasitic effects caused by ESD protection devices are well-characterized and included in the input matching network. As shown in Fig. 5(c), the differential LNA without ESD protection exhibits the S22-parameter of -9.3 dB at 5 GHz, whereas the differential LNA with the proposed ESD protection design has the S22-parameter of -11.4 dB. Fig. 5(d) compares the S12-parameters of these two LNAs. The S12-parameters of these two LNAs are better than -28 dB because good reverse isolation is one of the attributes in the cascode configuration.

The measured noise figures are shown in Fig. 6. The differential LNA without ESD protection has better noise figure, which is 2.16 dB at 5 GHz, whereas the differential LNA with the proposed ESD protection design exhibits the noise figure of 2.62 dB. The increase in noise figure is due to the addition of ESD protection devices connected to the RF input pads. The measured input-referred third-order intercept (IIP3) value is -12.5 dB for both LNAs. There is no significant difference on RF performances except noise figure between these two fabricated LNAs, which demonstrates the co-design effectiveness of LNA with ESD protection.

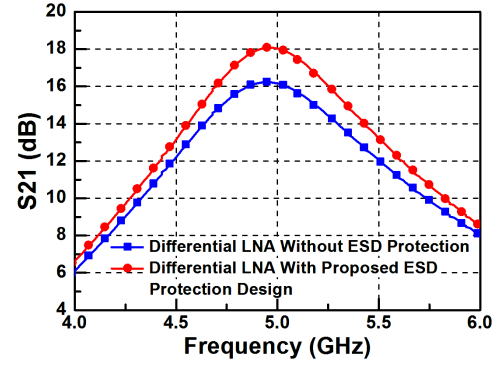


(a)

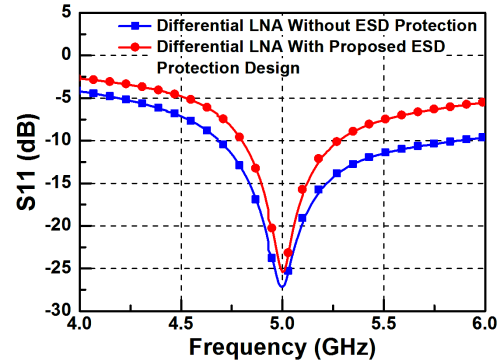


(b)

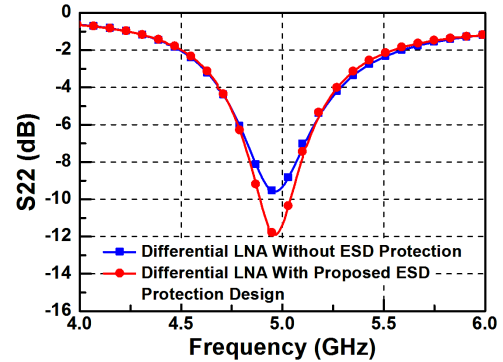
Fig. 4. Chip microphotographs of (a) differential LNA without ESD protection, and (b) differential LNA with the proposed ESD protection design.



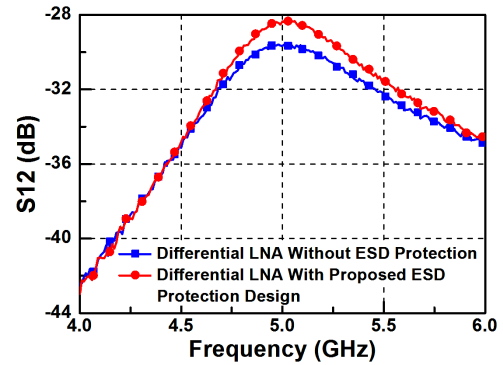
(a)



(b)



(c)



(d)

Fig. 5. Measured (a) S21-, (b) S11-, (c) S22-, and (d) S12-parameters of the differential LNAs without ESD protection and with the proposed ESD protection design.

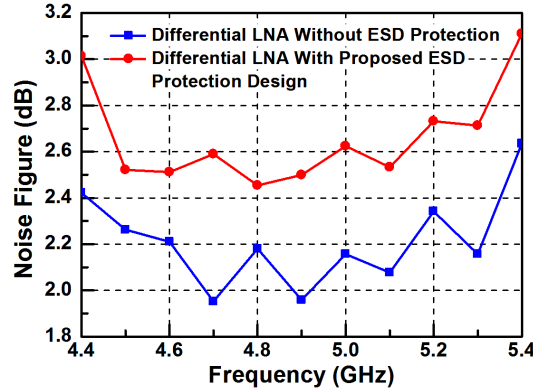


Fig. 6. Measured noise figures of the differential LNAs without ESD protection and with the proposed ESD protection design.

B. ESD Robustness

The human-body-model (HBM) ESD levels of these two fabricated LNAs are measured and listed in Table I. The differential LNA without ESD protection is very vulnerable to ESD. The differential LNA with the proposed ESD protection design has HBM ESD level of 3 kV, which meets the typical ESD specification of 2 kV for commercial ICs. During pin-to-pin ESD test, one input pad is zapped by ESD with the other input pad grounded, while VDD and VSS pads are floating. The ESD path during pin-to-pin ESD stresses is through P-diode₁, P-STSCR₁, and N-diode₂. Since P-STSCR₁ is placed near the differential input pads which can be quickly turned on during ESD stresses, the pin-to-pin ESD robustness is quite high of 6.5 kV. The differential LNA with the proposed ESD protection design can sustain VDD-to-VSS ESD stress of over 8 kV. Failure analysis has been also performed to investigate the failure mechanism. The scanning-electron-microscope (SEM) picture at the failure points is shown in Fig. 7. The failure points locate at the gate oxide of the input NMOS whose gate terminal is connected to the input pad.

TABLE I
HBM ESD LEVELS OF FABRICATED DIFFERENTIAL LNAs

HBM ESD Level	LNA Without ESD Protection	LNA With Proposed ESD Protection Design
Positive to VSS	< 50 V	3 kV
Negative to VDD	< 50 V	7 kV
VDD to VSS	0.5 kV	> 8 kV
Pin to Pin	< 50 V	6.5 kV

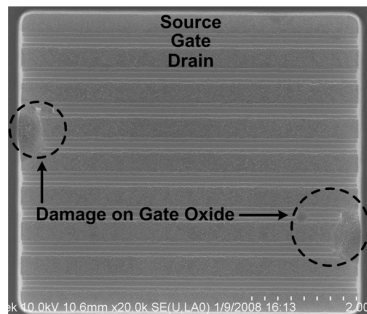


Fig. 7. SEM failure picture of differential LNA with the proposed ESD protection design after 3.5-kV PS-mode ESD test.

Because the ESD-clamping voltage between the input pad and VSS under 3.5-kV PS-mode ESD test is larger than the gate-oxide breakdown voltage, the gate oxide is damaged before the ESD protection devices damaged. To further enhance the ESD robustness, the turn-on resistance of the ESD protection devices and parasitic resistance along the ESD current path need to be further reduced.

V. CONCLUSION

A novel ESD protection design for differential I/O pads is proposed, especially considering the pin-to-pin ESD stress. Applied to a 5-GHz differential LNA, the proposed ESD protection design has been successfully verified in a 130-nm CMOS process. Once the parasitic effects caused by ESD protection devices can be accurately characterized, they can be matched without causing degradation on RF performance. Thus, the operation frequency of LNA will not be shifted and the RF performance can be still maintained after the ESD protection circuit is added into the chip. Excellent RF performance and ESD robustness can be simultaneously achieved by co-designing the LNA with ESD protection circuit.

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