Design of Bandgap Voltage Reference Circuit with all TFT Devices on Glass Substrate in a 3-μm LTPS Process

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***Abstract*-A bandgap voltage reference (BGR) circuit designed with the low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) on glass substrate is proposed, which has been successfully verified in a 3-μm LTPS process. The experimental results have shown that the measured temperature coefficient of the new proposed bandgap voltage reference circuit is around 195 ppm/°C under the supply voltage of 10V. The proposed bandgap voltage reference circuit can be applied on precise analog circuits for System-on-Panel (SoP) or System-on-Glass (SoG) applications.**

I. Introduction

Recently, low-temperature poly-Si (LTPS) thin-film transistors (TFTs) technology has been used to fabricate compact and high-resolution displays [1]. LTPS active-matrix liquid crystal displays (AMLCDs) integrated with driver and control circuits on glass substrate have been practically applied in some portable products, such as mobile phone, digital camera, and notebook, etc. The CPU, memory, timing controller, digital-to-analog converter (DAC), and driver buffer had been implemented on glass substrate with the LTPS TFT process [2], [3]. How to integrate more analog and digital circuits on panel is important for SoP (System-on-Panel) or SoG (System-on-Glass) applications.

Voltage reference generators are widely used in analog and digital circuits, such as DRAM, flash memory, analog-to-digital converter (ADC), and so on. The bandgap reference (BGR) circuit is the key design in analog circuits to provide a stable voltage reference with low sensitivity to temperature and supply voltage. So far, many techniques in CMOS silicon processes have been proposed to develop voltage or current references, which can be almost independent of temperature and power-supply voltage.

In CMOS silicon technology, the parasitic vertical bipolar junction transistors (BJTs) or the diodes had been commonly used in the BGR circuits [4], [5]. The main idea is to use the temperature-dependent voltage drop across the diode-connected BJTs (or the diodes) to modulate and stabilize the output voltage. With the negative temperature coefficients (TCs) of the diode-connected BJTs (or the diodes), a positive TC can be generated by a proper circuit design to compensate the negative TC and to stabilize the output voltage.

The incorporation of BJTs into CMOS technology somehow makes the process control difficult. Therefore, it was also considered to use only MOSFETs in the BGR circuit to simplify the process and to reduce the operating voltage/power. The voltage across MOSFETs is sensitive to temperature only when the MOSFETs are biased in the sub-threshold region. The gate-to-source voltage of MOSFETs in sub-threshold region is strongly dependent on temperature and exhibits a negative temperature coefficient. Some successful demonstrations of BGR circuits realized with MOSFETs in sub-threshold region have been reported in CMOS technology [6], [7]. However, to precisely bias the devices in the sub-threshold region is quite difficult with consideration of process variation.

Although the BGR circuit has been reported to provide a stable output reference voltage in CMOS technology, the LTPS BGR circuit on glass substrate was never reported in the literature. The conventional BGR circuit incorporated with BJTs or diodes is a great challenge for LTPS process since the characteristics of the poly-Si BJTs or the poly-Si diodes are still unknown or lack of reliable control. The use of LTPS TFT devices biased in the sub-threshold region is also not practical because the poly-Si TFT devices often suffer from significant threshold voltage variation. However, the I-V characteristics of LTPS TFT devices have been found to be strongly dependent on temperature when the devices are operated in the saturation region [8], [9]. Therefore, the LTPS BGR circuits can be realized by using only LTPS TFT devices. The particular thermionic-emission characteristic of LTPS TFT devices is first used in this work to design BGR circuit on glass substrate.

In this paper, a method to realize the circuit of bandgap voltage reference in LTPS process is proposed. Without additional laser trimming after fabrication, the new proposed bandgap voltage reference circuit has been verified on the glass substrate with the output voltage V_{REF} of 6.87 V at the room temperature. The temperature coefficient of BGR

output voltage is 195 ppm/°C under V_{DD} power supply of 10 V when the temperature varies from 25 °C to 125 °C.

II. Traditional Bandgap Reference Circuit In CMOS Technology

A traditional implementation of bandgap voltage reference circuit in CMOS technology is shown in Fig. 1 [10]. In this circuit, the output voltage (V_{REF}) is the sum of a base-emitter voltage (V_{EB}) of BJT Q_3 and the voltage drop across the upper resistor R_2. The BJTs (Q_1, Q_2, and Q_3) are typically implemented by the diode-connected parasitic vertical PNP bipolar junction transistors in CMOS process with the current proportional to exp (V_{EB}/V_T), where V_T *(=kT/q)* is the thermal voltage. Under constant current bias, V_{EB} is strongly dependent on V_T as well as temperature. The current mirror (formed by M_1, M_2, and M_3) is designed to bias Q_1, Q_2, and Q_3 with identical current. Then, the voltage drop on the resistor R_1 can be expressed by

$$V_{R1} = V_T \ln(\frac{A_1}{A_2}), \tag{1}$$

where A_1 and A_2 are the emitter areas of Q_1 and Q_2. It is noted that V_{R1} exhibits a positive temperature coefficient when A_1 is larger than A_2. Besides, since the current flows through R_1 is equal to the current flows through R_2, the output voltage of the traditional bandgap voltage reference circuit can be written as

$$V_{REF} = V_{EB3} + \frac{R_2}{R_1} V_T \ln(\frac{A_1}{A_2}). \tag{2}$$

The second item in Eq. (2) is proportional to the absolute temperature (PTAT), which is used to compensate the negative temperature coefficient of V_{EB3}. In general, the PTAT voltage comes from the thermal voltage V_T with a temperature coefficient about +0.085 mV/°C in CMOS technology, which is quite smaller than that of V_{EB}. After multiplying the PTAT voltage with an appropriate factor (R_2/R_1) and summing with V_{EB}, the output voltage V_{REF} of bandgap reference circuit can result in very low sensitivity to temperature.

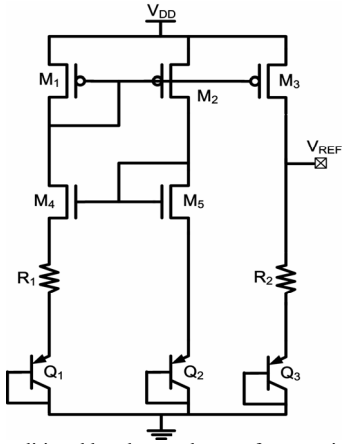

Figure 1. The traditional bandgap voltage reference circuit realized in CMOS technology with parasitic vertical PNP bipolar junction transistors.

III. New Proposed Bandgap Voltage Reference Circuit In LTPS Technology

From the analysis on traditional BGR circuit, it has been known that the realization of BGR circuit strongly depends on the temperature coefficient of BJTs (Q_1, Q_2, and Q_3). In other words, the exponential term exp(V_{EB}/V_T) in the I-V relationship of BJTs makes it possible to obtain a PTAT voltage from the voltage difference between a large-area BJT and a small-area BJT.

For LTPS TFT devices, the drain current I_{DS} of devices operated in the saturation region can be expressed as [11]

$$I_{DS} = \frac{W}{2L} \mu_0 C_{ox} (V_{GS} - V_{TH})^2 \exp(-\frac{V_B}{V_T}), \tag{3}$$

where μ_0 is the carrier mobility within the grain, L denotes the effective channel length, W is the effective channel width, C_{ox} is the gate oxide capacitance per unit area, V_{TH} is the threshold voltage of TFT device, and V_{GS} is the gate-to-source voltage of TFT device. V_B is the potential barrier at grain boundaries which is associated with the crystallization quality of the poly-Si film. Under small V_{GS}, V_B is large. When the V_{GS} increases, V_B decreases rapidly. A typical relationship between V_B and V_{GS} is depicted in Fig. 2, which is exactly measured from an N-type TFT (NTFT) device. When the devices are operated under small V_{GS}, it is found that the drain current I_{DS} of devices is dominated by the exponential term and can be estimated by

$$I_{DS} = W\alpha \exp(-\frac{V_B}{V_T}), \tag{4}$$

where α is treated as a constant under small gate bias (V_{GS}). Then, the equation for V_B can be derived as

$$V_B = V_T \ln(\frac{W\alpha}{I_{DS}}) = \frac{kT}{q} \ln(\frac{W\alpha}{I_{DS}}). \tag{5}$$

When there is a variation of temperature ΔT, the corresponding variation of V_B is

$$\Delta V_B = \frac{k\Delta T}{q} \ln(\frac{W\alpha}{I_{DS}}). \tag{6}$$

From Eq. (6), it can be found that the temperature coefficient (TC) of V_B can be modulated by the channel width. The larger channel width gives rise to the larger TC of V_B.

From Fig. 2, the variation of V_B is related to the variation of V_{GS}. Assuming that the variation of V_{GS} (ΔV_{GS}) is very small, a negative linear approximation can be given between ΔV_B and ΔV_{GS} as

$$\Delta V_{GS} = -\frac{1}{m} \Delta V_B = -\frac{k\Delta T}{mq} \ln(\frac{W\alpha}{I_{DS}}) = -\frac{\Delta V_B \Delta T}{m\Delta T}, \tag{7}$$

where m is the absolute value of the slope under linear approximation as shown in the inset of Fig. 2. The devices biased at small V_{GS} can exhibit a large V_B if its channel width is enlarged. As a result, the LTPS TFT devices with larger channel width exhibit larger absolute value of TC. Such assumption has been verified by the following measurements

on the LTPS TFT devices. All the devices are n-type poly-Si TFT devices fabricated in the same run with commercial excimer laser annealing process. The channel length of NTFT devices is fixed as 6 μm and the LDD length is 1.25 μm.

First, the measurement of the TC of diode-connected LTPS TFT devices with channel width of 6 μm is performed by changing the temperature from 25°C to 125°C. Under a constant driving current of 10 μA, the V_{GS} as a function of temperature is plotted in Fig. 3(a). It can be observed that when temperature increases from 25°C to 125°C, the V_{GS} decreases from 1.88 V to 1.66 V. In Fig. 3(a), the temperature coefficient of this TFT device with channel width of 6 μm is approximated as -2.15 mV/°C. Furthermore, the TC of diode-connected LTPS TFT devices with a wide channel width of 30 μm is measured. Under a constant driving current of 10 μA, the V_{GS} as a function of temperature is plotted in Fig. 3(b). As temperature changes from 25°C to 125°C, the V_{GS} decreases from 1.23V to 0.78V, significantly. In Fig. 3(b), the temperature coefficient of this TFT device with 30-μm channel width is approximated as -4.85 mV/°C. As predicted, the LTPS TFT device with a larger channel width exhibits a larger absolute value of TC.

After the evaluation on the TC of poly-Si TFT devices with different channel widths, the new LTPS BGR circuit can be implemented in Fig. 4. In this design, the TFT devices M_1, M_2, M_3, M_4, and M_5 are biased in saturation region. The diode-connected NTFT devices M_6, M_7, and M_8, which replace the diode-connected BJTs in the traditional CMOS BGR circuit (Fig.1) are also biased in saturation region. The nodes n_1 and n_2 are designed to have equal potential by the current mirror circuit.

The channel width of M_6 (W_6) is larger than the channel width of M_7 (W_7), so the TC of M_6 is more negative than the TC of M_7. The voltage drop across the resistor R_1 (V_{R1}) therefore exhibits a positive TC. If the dependence of m on V_{GS} is neglected, the variation of V_{R1} (ΔV_{R1}) as a function of ΔT can be expressed as

$$\Delta V_{R1} = \frac{k\Delta T}{mq}\ln\left(\frac{W_6}{W_7}\right) = \frac{k\Delta T}{mq}\ln N. \quad (8)$$

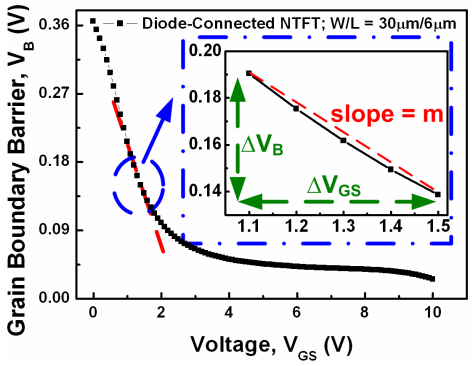

Figure 2. The dependence between potential barrier V_B and gate-to-source voltage V_{GS} of diode-connected N-type TFT (NTFT) device.

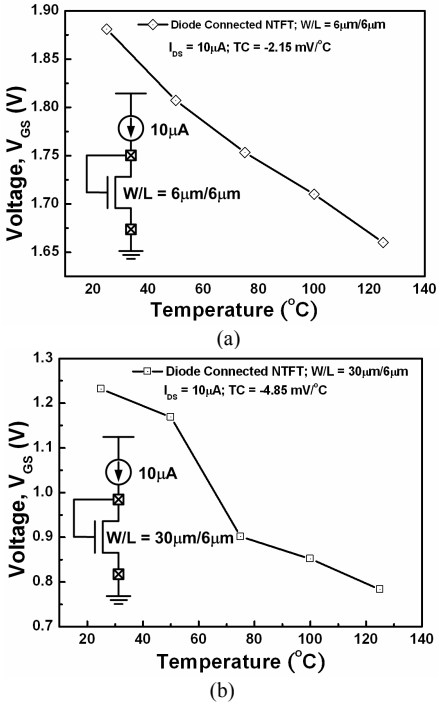

Figure 3. The measured temperature coefficients (TC) of diode -connected TFT devices under a constant drain current of 10μA with (a) channel width of 6μm, and (b) channel width of 30μm, in LTPS process.

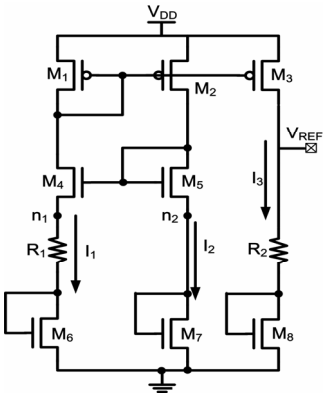

Figure 4. The implementation of the new proposed bandgap voltage reference circuit with all TFT devices in a LTPS process.

Obviously, ΔV_{R1} is proportional to the absolute temperature (PTAT). Hence, a PTAT loop is formed by M_6, M_7, and R_1. The PTAT current variation ΔI_1 can be written as

$$\Delta I_1 = \frac{k\Delta T}{mqR_1}\ln N, \quad (9)$$

where N ($=W_6/W_7$) is the channel width ratio of M_6 and M_7, and V_T is the thermal voltage. The current mirror, which is composed of M_1, M_2, and M_3, imposes equal currents in these three branches I_1, I_2, and I_3 of the circuit. The output voltage (V_{REF}) is the sum of a gate-source voltage of TFT M_8 (V_{GS8}) and the voltage drop across the upper resistor (V_{R2}). Therefore, the output voltage variation (ΔV_{REF}) of the new proposed bandgap reference circuit can be expressed as

$$\Delta V_{REF} = \Delta I_3 R_2 + \Delta V_{GS8} = \frac{R_2}{R_1}\frac{k\Delta T}{mq}\ln N + \Delta V_{GS8}, \quad (10)$$

where R_1 and R_2 are the resistors shown in Fig. 4. The first item in Eq. (10) with positive TC is proportional to the absolute temperature (PTAT), which is used to compensate the negative temperature coefficient of ΔV_{GS8}. After multiplying the PTAT voltage with an appropriate factor (proper ratio of resistors) and summing with ΔV_{GS8}, the output voltage of bandgap reference circuit can result in very low sensitivity to temperature.

IV. Experimental Results

The new proposed bandgap reference circuit has been fabricated in a 3-μm LTPS technology. The chip photo of the fabricated bandgap reference circuit on glass substrate is shown in Fig. 5. The threshold voltage of TFT devices is about $V_{thn} \approx V_{thp} \approx 1.25$ V at 25 °C. The total gate area of M_6 is 480 μm^2 and that of M_7 is 80 μm^2 in this fabrication. The resistors in this chip, formed by ploy resistors with minimum process variation, are used to improve the accuracy of resistance ratio. The chip size of the fabricated bandgap reference circuit is 400 × 380 μm^2. The power supply voltage V_{DD} is set to 10 V, and the total operating current is 8.97 μA. The measured results of the output voltage V_{REF} are shown in Fig. 6, where the R_2 is drawn with different values in the test chips. As R_2 is equal to 500 kΩ, the measured temperature coefficient of the fabricated bandgap reference circuit on glass substrate is around 195 ppm/°C (without laser trimming after fabrication) from 25 to 125 °C, whereas the output voltage (V_{REF}) is kept at 6.87 V.

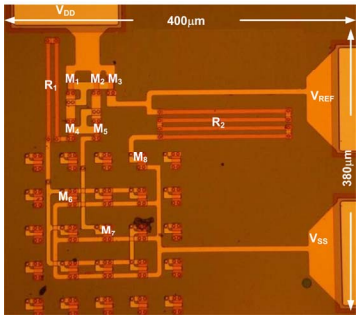

Figure 5. Chip photo with PAD of the new proposed bandgap reference circuit fabricated in a 3-μm LTPS process.

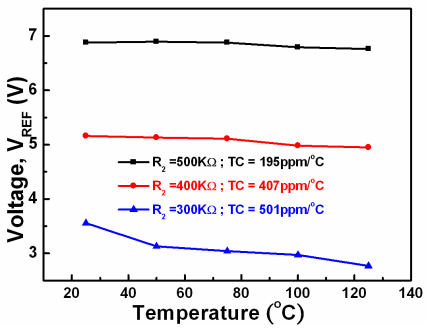

Figure 6. The measured output voltage (V_{REF}) of the fabricated bandgap reference circuit without laser trimming after fabrication.

V. Conclusion

The new proposed bandgap voltage reference circuit realized by all TFT devices has been successfully verified in a 3-μm LTPS process. The measurement results of the bandgap voltage reference are V_{REF} of 6.87 V with temperature coefficient of 195 ppm/°C, which consumes an operating current of 8.97 μA under supply voltage of 10 V on glass substrate. The new proposed bandgap voltage reference circuit can be used to realize the precise analog circuits in LTPS process for System-on-Panel (SoP) or System-on-Glass (SoG) applications.

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