CDM ESD Protection in CMOS Integrated Circuits

Ming-Dou Ker and Yuan-Wen Hsiao
Nanoelectronics and Gigascale Systems Laboratory
Institute of Electronics, National Chiao-Tung University
Hsinchu, Taiwan

***Abstract*—The impacts of charged-device-model (CDM) electrostatic discharge (ESD) events on integrated circuit (IC) products are presented in this paper. The mechanism of chip-level CDM ESD event is introduced with some case studies on CDM ESD damages. Besides the chip-level CDM ESD event, the board-level CDM ESD event, which had been reported to cause damages in many customer-returned ICs, is also investigated in this work. The chip-level and board-level CDM ESD levels of several test devices and test circuits fabricated in CMOS processes are characterized and compared. The experimental results have shown that the board-level CDM ESD level of the test circuit is much lower than the chip-level CDM ESD level, which indicates that the board-level CDM ESD test is more critical than the chip-level CDM ESD test in the field applications. In addition, failure analysis reveals that the failure on the test circuit under board-level CDM ESD test is much severer than that under chip-level CDM ESD test.**

I. INTRODUCTION

With the advances of CMOS processes, integrated circuits (ICs) have been fabricated with thinner gate oxides to achieve higher operation speed and lower power consumption. However, in the field applications, electrostatic discharge (ESD) was not scaled down with CMOS technology. Thus, ESD protection design in nanoscale CMOS processes becomes a challenging task. There are three component-level (or called as chip-level) ESD test standards, which are human body model (HBM) [1], machine model (MM) [2], and charged device model (CDM) [3]. CDM ESD test becomes more and more critical, because the nanoscale CMOS devices are fabricated with thinner gate oxide, and more function blocks are integrated into a single chip for system-on-chip (SoC) applications with a larger die size. An IC with larger die size can store more static charges in its body, which leads to larger discharging current during CDM ESD events. In addition, CDM ESD event has huge peak current and short duration, which increase the difficulty to effectively protect the internal circuits against CDM ESD events. To provide efficient CDM ESD protection, the ESD protection device should be turned on quickly and has high ESD robustness. Furthermore, CDM ESD current flows from the chip substrate to the external ground, whereas HBM and MM ESD currents are injected from the external ESD source into the zapped pin. As a result, CDM ESD events often cause internal damage to CMOS ICs. The aforementioned features make CDM ESD protection for CMOS ICs more challenging. Recently, effective ESD protection design against CDM ESD stresses has gotten more requests from IC industry.

Besides chip-level CDM ESD issue, board-level CDM ESD issue becomes more important recently, because it often causes the ICs to be damaged after the IC is installed to the circuit board of electronic system. For example, board-level CDM ESD events often occur during the module function test on the circuit board of electronic system. Even though the IC has been designed with good chip-level ESD robustness, it would still be very weak in board-level CDM ESD test. The reason is that the discharging current during the board-level CDM ESD event is significantly larger than that of the chip-level CDM ESD event. There are several papers addressing the phenomenon of the board-level CDM ESD events on real IC products [4], [5]. In these two previous works, the ICs which already passed the component-level ESD specifications were still returned by customers because of ESD failure. After performing the field-induced CDM ESD test on the ICs which have been mounted on the printed circuit board (PCB), the failure is the same as that happened in the customer returned ICs. This indicates that the real-world charged-board-model (CBM) ESD damage can be duplicated by the board-level CDM ESD test. The previous works have demonstrated that the board-level CDM ESD events indeed exist, which should be taken into consideration for all IC products.

In this paper, the CDM ESD issue in CMOS ICs is comprehensively addressed, including chip-level and board-level CDM ESD events. The mechanisms of chip-level and board-level CDM ESD events are introduced and compared. The chip-level and board-level CDM ESD tests are performed to some test devices and test circuits fabricated in CMOS processes. Moreover, failure analysis is also performed to investigate the difference between the failures under chip-level and board-level CDM ESD tests.

II. CHIP-LEVEL CDM ESD EVENT

A. Mechanism of Chip-Level CDM ESD Event

During the assembly of IC products, static charges could be stored within the body of IC products due to induction or rubs. Once a certain pin of the IC chip is suddenly grounded, the static charges originally stored within the IC body will be discharged out through the grounded pin, which is called as the CDM ESD event and shown in Fig. 1. The CDM ESD event causes huge current (of ~10 A) in a very short time

period (of ~1 ns). There are many situations for the pins of an IC to touch ground. For example, when the pin touches grounded metallic surface or the pin is touched by grounded metallic tools, as shown in Fig. 2.

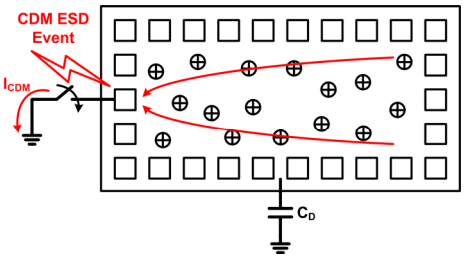


Fig. 1. In CDM ESD event, the stored charges in the IC are quickly discharged through the grounded pin.

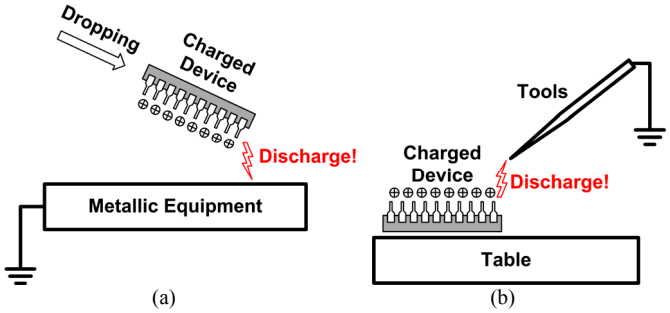


Fig. 2. CDM ESD event may occur when (a) the pin touches grounded metallic surface, or (b) the pin is touched by grounded metallic tool.

Different ICs have different die sizes, so their equivalent parasitic capacitances (C_D) are totally different from another one. Thus, different ICs have different peak currents and robustness under CDM ESD tests. When a device under test (DUT) with the equivalent capacitance of 4 pF is under 1-kV CDM ESD test, the CDM ESD current rises to more than 15 A in several nanoseconds [6]. As compared with HBM and MM ESD events, the discharging current in CDM ESD event is not only huge, but also faster. Since the duration of CDM ESD event is much shorter than that of HBM and MM ESD events, the IC may be damaged during CDM ESD events before the ESD protection circuit is turned on. Capacitor will be a low-impedance device, when the signal frequency is increased. Thus, CDM ESD current is most likely to flow through the capacitive structures of devices in ICs. In CMOS ICs, the gate oxides of MOS transistors are capacitive structures, so the gate oxide is most likely to be damaged under CDM ESD events. In nanoscale CMOS processes, the gate oxide becomes thinner, which makes the equivalent capacitance per unit area larger. Consequently, the thinner gate oxides of MOS transistors in nanoscale CMOS processes are more vulnerable to CDM ESD stresses. Besides, more functions are integrated into a single chip, which makes the die size larger. Under the same charged voltage, larger capacitance stores more static charges, so the CDM ESD current is larger for the IC with larger die size. Therefore, nanoscale CMOS ICs with larger die size and thinner gate oxide are very sensitive to ESD, especially CDM ESD events.

During the manufacturing of IC products, some of the steps had been reported to cause chip-level CDM ESD events, which leads to yield loss. There are several works addressing the cause of chip-level CDM ESD events during manufacturing of IC products [7]-[9]. In the packaging process of plastic-leaded-chip-carrier (PLCC) packages, the chips are induced to store static charges when they are carried by the carrier of the machine. When a certain pin of the charged chip is connected to external ground, CDM ESD event occurs. To solve this problem, the ionizing air blower can be utilized in the manufacturing environment to neutralize the static charges stored in the chips and the machines [7].

An IC fabricated in a 0.8-μm CMOS process had been reported to have leakage current when it was normally biased, but it worked well during function test after fabrication. Failure analysis demonstrated that the gate oxide of the NMOS in the input buffer was damaged by CDM ESD event. After study, it was found that the socket of the IC tester was charged during function test, which induced the tested IC to store static charges. After finishing function test, the charged IC was placed on the grounded metallic table, and CDM ESD event occurred to damage the IC which has passed function test [8].

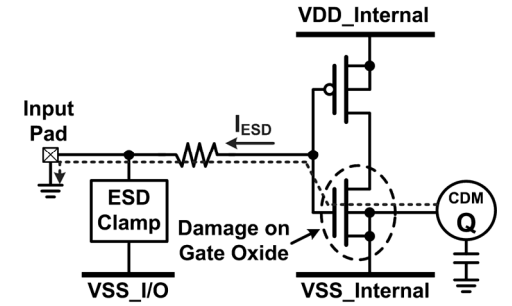
During the fabrication of ICs, separating the tape and die after cutting the die from wafer also causes substantial charge accumulation in the die. Measured by the Faraday cup, it was reported that the CDM ESD voltage could be more than 1000 V during the separation of the tape and die. Such a high CDM ESD voltage may damage the IC product [9].

B. Case Study on Chip-Level CDM ESD Damage

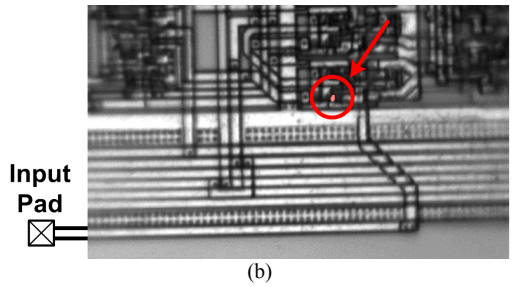
The CDM ESD current path in an input buffer fabricated in a 0.8-μm CMOS process is shown in Fig. 3(a). This chip passes 2-kV HBM and 200-V MM ESD tests. Although this chip is equipped with ESD protection circuit at its input pad, it is still damaged after 1000-V CDM ESD test. As shown in Fig. 3(b), the failure point after CDM ESD test is located at the gate oxide of the NMOS in the input buffer. Duo to consideration of noise isolation between I/O cells and internal circuits, the VSS of I/O cells (VSS_I/O) and the VSS of internal circuits (VSS_Internal) are often separated in the chip layout. As a result, the ESD clamp device located at the input pad can not effectively protect the gate oxide of the input buffer during CDM ESD stresses, because there is no connection between VSS_I/O and VSS_Internal. The CDM ESD current which damages the gate oxide of NMOS in the input buffer is shown by the dash line in Fig. 3(a). Fig. 4 is the failure picture of another IC after CDM ESD test. This IC was fabricated in a 0.5-μm CMOS process. The scanning-electron-microscope (SEM) picture had proven that the failure caused by CDM ESD event is located at the poly gate of a MOS transistor in the internal circuit that is connected to some input pad through metal connection.

From these two aforementioned cases, the charges stored in the body of chip still flow through the gate terminal of the input MOS transistor in the internal circuits to damage its gate oxide during CDM ESD stresses, even though ESD protection circuit has been applied to the input pad. According to the previous works, the pins around the corners in IC products are more often to suffer CDM ESD events, because the corner pins are usually first touched by external ground during

transportation or assembly [10]. In addition to HBM and MM ESD protection, how to design efficient CDM ESD protection circuit for IC products is an important consideration in component-level ESD protection design.



(a)



(b)

Fig. 3. (a) CDM ESD current path in an input buffer. (b) The failure point is located at the gate oxide of the input NMOS.

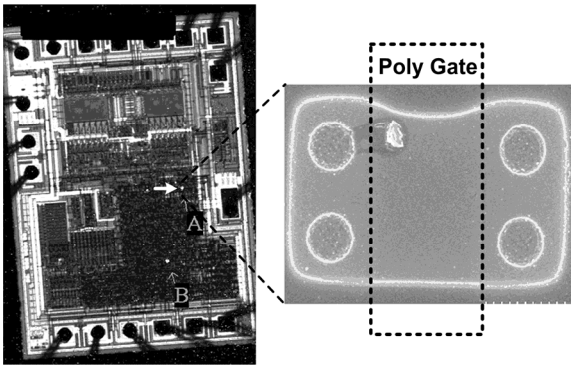


Fig. 4. After chip-level CDM ESD test, the failure point is located at the gate oxide of an NMOS in the internal circuit.

III. BOARD-LEVEL CDM ESD EVENT

A. Mechanism of Board-Level CDM ESD Event

In microelectronic systems, IC chips must be attached to the PCB. Before the attachment, static charges could be stored in the substrate of the chip or the metal traces on the dielectric layer in the PCB. During the attachment, the static charges originally stored in the IC chip or the PCB will be redistributed, as illustrated in Fig. 5. To illustrate the charge redistribution mechanism, two capacitors C_1 and C_2 are used to denote the parasitic capacitances of the IC chip and the PCB, respectively. Usually C_2 is much larger than C_1, because the size of PCB is much larger than that of the IC chip. The initial voltages across C_1 and C_2 are V_1 and V_2, respectively. C_1 and C_2 are not connected together in the beginning. When the IC chip is attached to the PCB, C_1 and C_2 are shorted and the charges stored in the IC chip and the PCB are redistributed. Consequently, the voltages across C_1 and C_2 will be equal and become $(C_1 \times V_1 + C_2 \times V_2) / (C_1 + C_2)$ after they are connected together. The instantaneous current during the attachment of IC chip to PCB will be increased if the initial voltage difference between the IC chip and PCB is increased. The instantaneous current during the charge redistribution may be larger than 10 A, which can easily damage the IC to cause a CDM-like failure. This is one of the examples of board-level CDM ESD events. Moreover, installing the modules to the system during the assembly of microelectronic products also causes board-level CDM ESD events. To mitigate this impact, the ionizing air blower can be utilized in the manufacturing environment to neutralize the static charges stored in the IC chips and PCBs.

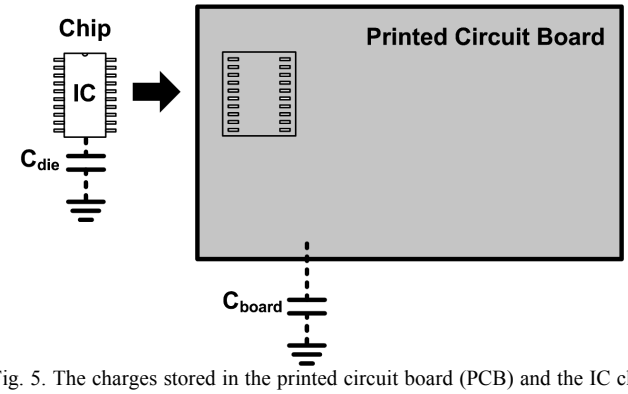


Fig. 5. The charges stored in the printed circuit board (PCB) and the IC chip will be redistributed when the IC chip is attached to the PCB.

After the IC chips are attached to the PCB, module function test is performed. During module function test, I/O pins of the module are connected to the instruments. If there are static charges stored in the module, board-level CDM ESD event will occur to damage the IC chips on the PCB. Besides, board-level CDM ESD event may also occur before module function test when the I/O pin is connected to the cable, and the other terminal of the cable is accidentally grounded. If the voltages across the equivalent capacitances of the chips and PCB are larger, more charges are stored, which leads to larger discharging current. To solve this problem, ESD dischargers consisting of large resistances (~ MΩ) can be used to ground the I/O pins of the module before module function test. Although there is still current flowing through the IC chips, the current peak can be significantly reduced by the large series resistance. As a result, the chip can be protected from being damaged by the board-level CDM ESD event during module function test.

In the assembly and testing of LCD monitor, board-level CDM ESD events may also occur. As shown in Fig. 6, when the driver ICs are attached to the LCD panel, charge transfer occurs, which causes board-level CDM ESD current flowing between the driver ICs and LCD panel to damage them. Moreover, the driver IC can be also damaged by such board-level CDM ESD events when a certain pin of the driver IC on panel is connected to ground during panel function test. The charges stored in the LCD panel will be discharged through the pins of the driver ICs to the external ground during the

panel function test. The ESD current paths are shown by the dash lines in Fig. 7. Since the on-glass thin-film transistors (TFTs) in LCD panel have higher operation voltage than that of the most digital ICs, the core circuits and I/O cells of LCD driver ICs have different operation voltages. Such ICs with multiple power domains have individual power pads and ground pads for each power domain. Once the aforementioned board-level CDM ESD events occur, ESD current will flow from the LCD panel through the output pad of the driver IC into the driver IC. Although ESD protection circuits have been applied to each output pad of the driver IC to bypass ESD current to the power pad (VCC) or ground pad (VSS1) within the power domain, the interface circuits between different power domains are often damaged during such board-level CDM ESD events due to the disconnection between the power pads or ground pads in different power domains. To solve this problem, ESD protection devices can be inserted between the power pads or ground pads in different power domains to provide ESD current paths between the separated power domains, as shown in Fig. 8 [11].

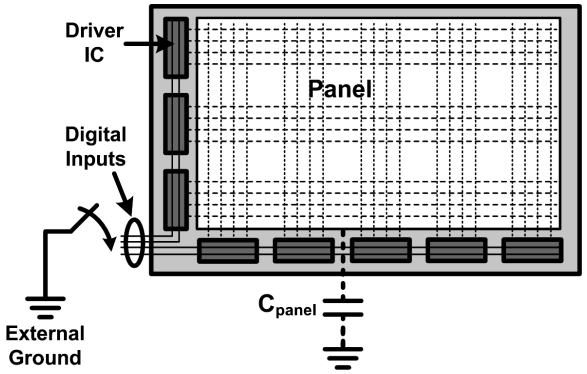


Fig. 6. During panel function test, connecting the pins of the driver IC to external ground will cause board-level CDM ESD event.

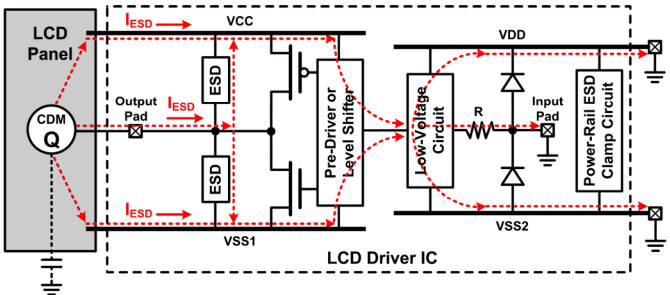


Fig. 7. During board-level CDM ESD event, ESD current flows from the LCD panel through the interface circuits of driver IC to the grounded pins.

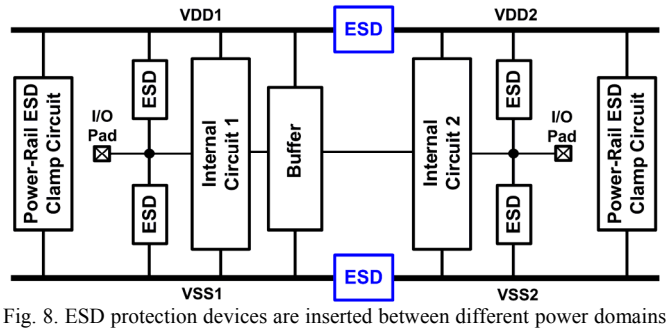


Fig. 8. ESD protection devices are inserted between different power domains to provide ESD current paths between the separated power domains.

B. Case Study on Board-Level CDM ESD Damage

Recently, it has been reported that the real-world CBM ESD damage is caused by the board-level CDM ESD event [4], [5]. In [5], a LCD driver IC had passed 4-kV HBM, 200-V MM, and 500-V CDM ESD test, but it was still returned by customer. Failure analysis had shown that the ESD protection diode was damaged with a CDM-like failure. To verify the ESD damage, the board-level CDM ESD test was performed to the LCD driver IC. In the board-level CDM ESD test, the IC and the PCB on which the IC is mounted are both put on the charging plate of the conventional field-induced CDM ESD tester, as shown in Fig. 9. After +1000-V board-level CDM ESD test, the LCD driver IC was damaged. Failure analysis showed that the IC after board-level CDM ESD test exhibits the same failure as that found in the customer returned IC, as shown in Fig. 10. This experiment had demonstrated that performing the board-level CDM ESD test can successfully duplicate the failure in the customer returned IC.

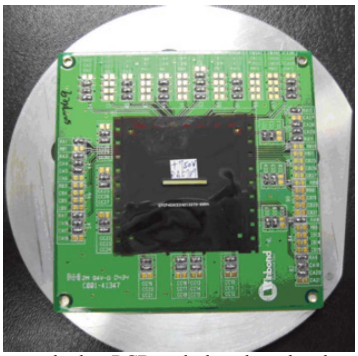
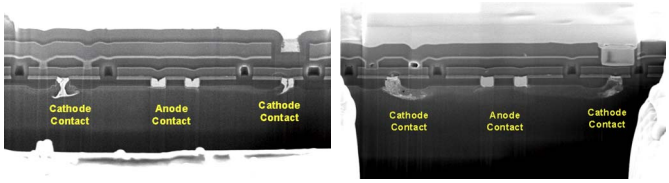


Fig. 9. The IC was attached to PCB and placed on the charging plate of field-induced CDM ESD tester to perform board-level CDM ESD test.



(a) (b)

Fig. 10. SEM cross sectional pictures of the ESD protection diode in the (a) customer returned IC and (b) IC after +1000-V board-level CDM ESD test.

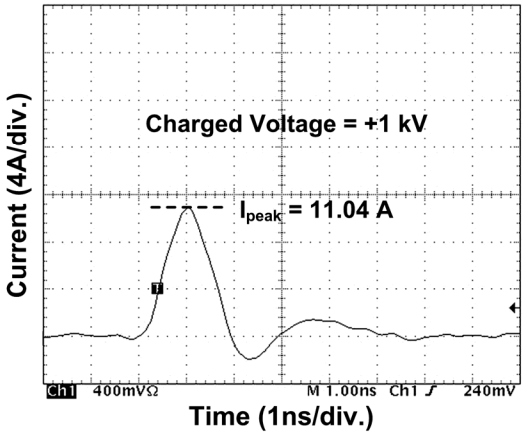
IV. Experimental Results of CDM ESD Test

In this section, the board-level and chip-level CDM ESD tests have been performed to several CMOS ICs. There are two components to be tested, which are the stand-alone gate-grounded NMOS (GGNMOS) and a 2.5-GHz high-speed receiver circuit. The equivalent capacitance of the PCB in the board-level CDM ESD test in this test is 274 pF. The main difference between board-level CDM and chip-level CDM ESD test is that the IC and PCB are both charged in board-level CDM ESD test, whereas only the IC is charged in the chip-level CDM ESD test. Since the equivalent capacitance of the PCB is significantly larger than that of the DUT, more charges are stored and discharged in board-level CDM ESD test. Therefore, it is expected that the board-level CDM ESD test is more critical than the conventional chip-level CDM

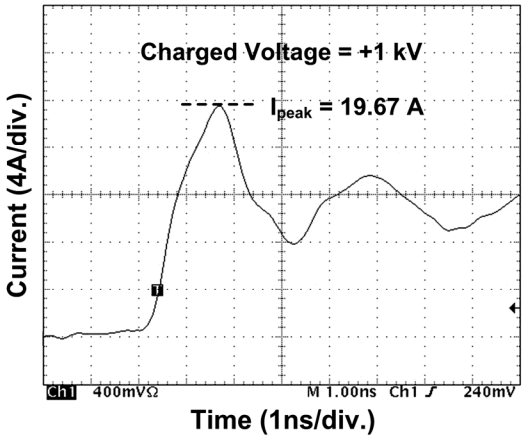
ESD test. The measured results on the chip-level and board-level CDM ESD levels with the different test components are compared. In addition, failure analysis has been performed to characterize the failure mechanism.

A. Test With Gate-Grounded NMOS

A GGNMOS fabricated in a 0.18-μm CMOS process was used as the DUT for the chip-level and board-level CDM ESD tests. GGNMOS is a widely used ESD protection device in CMOS ICs. In a GGNMOS, the drain terminal is connected to the protected pad, whereas the gate, source, and bulk terminals are connected to the VSS power line of the IC. The equivalent capacitance of this GGNMOS in IC package between its drain terminal and substrate is 6.2 pF. In the chip-level and board-level CDM ESD tests, the drain terminal of the GGNMOS is tested. Fig. 11 (a) and (b) show the measured current waveforms under 1-kV chip-level and board-level CDM ESD tests, respectively. The peak currents under chip-level and board-level CDM ESD tests are 11.04 A and 19.67 A, respectively. Under the same charged voltage, the peak discharging current under board-level CDM ESD test is significantly larger than that under chip-level CDM ESD test. Such a huge discharging current with a very short rise time can easily damage the GGNMOS.



(a)



(b)

Fig. 11. Measured current waveforms of GGNMOS under (a) +1-kV chip-level CDM ESD test, and (b) +1-kV board-level CDM ESD test.

B. Test With 2.5-GHz High-Speed Receiver Interface Circuit

A 2.5-GHz differential high-speed receiver interface circuit fabricated in a 0.13-μm CMOS process was also verified with the chip-level and board-level CDM ESD tests. Fig. 12 shows the circuit schematic of the 2.5-GHz differential high-speed receiver interface circuit with on-chip ESD protection design. The receiver interface circuit has the differential input stage realized by PMOS transistors. The double-diode ESD protection scheme is applied to each differential input pad. Besides ESD protection devices at the differential input pads, the power-rail ESD clamp circuit has been designed to provide ESD current path between VDD and VSS. P-type substrate-triggered silicon-controlled rectifier (P-STSCR) [12] was used in the power-rail ESD clamp circuit because SCR devices had been reported to have high ESD robustness under a small device size.

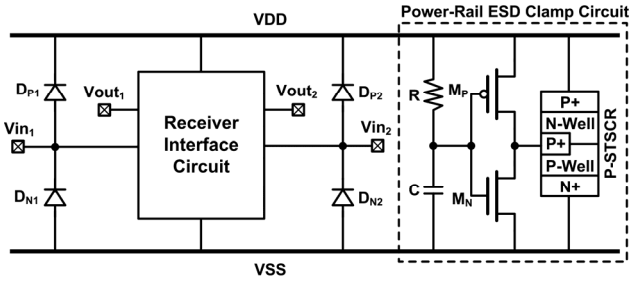


Fig. 12. Test circuit of 2.5-GHz high-speed receiver interface circuit for chip-level and board-level CDM ESD tests.

Because of high-speed application, the dimensions of the ESD protection diodes at the input pads are limited to reduce the parasitic capacitance at the pads. Besides, the ESD protection devices and the inverter of the power-rail ESD clamp circuit were placed under the bonding pad to save chip area. A reference high-speed receiver interface circuit without on-chip ESD protection design was also fabricated in the same process to compare its ESD robustness. The tested pin under chip-level and board-level CDM ESD tests is the Vin_1 pad. The chip-level and board-level CDM ESD levels of the reference high-speed receiver interface circuit without ESD protection are quite poor, which failed at ±100 V and ±50 V, respectively. With the on-chip ESD protection circuits, the failure voltages under chip-level and board-level CDM ESD tests are greatly improved to +2000 V/-1300 V and +1300 V/-900 V, respectively. Again, the board-level CDM ESD level is lower than the chip-level CDM ESD level. Failure analysis had been performed on the ESD-protected high-speed receiver interface circuits after chip-level CDM ESD test of -1300 V and board-level CDM ESD test of -900 V. The SEM failure pictures after chip-level and board-level CDM ESD tests are shown in Fig. 13(a) and (b), respectively. The failure points are located at the ESD diode D_{P1}. Although the ESD protection devices are successfully turned on during CDM ESD tests, huge current during CDM ESD tests still damages the ESD protection devices. According to the SEM failure pictures, the failure in Fig. 13(b) is much worse under board-level CDM ESD test than that in Fig. 13(a) under chip-level CDM ESD test. This again demonstrates that the board-level CDM ESD event is more critical than the chip-level CDM ESD event.

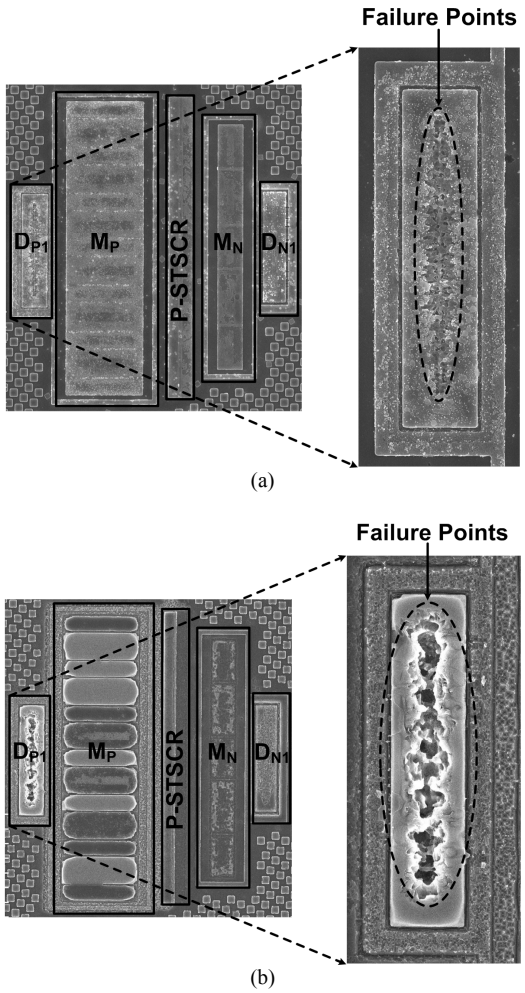


Fig. 13. SEM failure pictures on the failure points of the 2.5-GHz high-speed receiver interface circuit after (a) -1300-V chip-level CDM ESD test, and (b) -900-V board-level CDM ESD test.

V. Conclusion

Both the chip-level and board-level CDM ESD issues in CMOS ICs have been comprehensively addressed in this work. The mechanisms of chip-level and board-level CDM ESD events are presented with some case studies. Then, the chip-level and board-level CDM ESD tests are performed to several test devices and test circuits fabricated in 0.18-μm and 0.13-μm CMOS processes. Measured results have shown that the board-level CDM ESD tests are more critical than the chip-level CDM ESD tests. There were several designs reported for chip-level CDM ESD protection [13]-[18]. However, no design against board-level CDM ESD events is reported so far. In the nanaoscale CMOS processes, the gate-oxide becomes thinner, which degrades the CDM ESD robustness of CMOS ICs. In high-speed or radio-frequency (RF) applications, large ESD protection devices can not be applied to the I/O pad due to the limitation on parasitic capacitance, which further increases the difficulty on CDM ESD protection design. Moreover, the die size becomes larger in SoC applications, which indicates that more charges can be stored in the substrate of chip. Consequently, CDM ESD issues, including chip-level and board-level CDM ESD events, will become more critical and should be taken into consideration in ICs and microelectronic systems which are realized in nanoscale CMOS processes.

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