Transient Detection Circuit for System-Level ESD Protection and Its On-Board Behavior with EMI/EMC Filters

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***Abstract*—A new on-chip transient detection circuit for system-level electrostatic discharge (ESD) protection is proposed. The circuit performance of detecting fast electrical transients has been verified in a 0.18-μm CMOS integrated circuit (IC). The experimental results have confirmed that the proposed on-chip transient detection circuit can detect positive and negative fast electrical transients during system-level ESD zapping. Three board-level noise filtering networks have been investigated their enhancement on detection range of the proposed on-chip transient detection circuit. The chip-level solution can be further co-designed with the board-level solution in order to meet high system-level ESD specification.**

***Keywords*—Electrostatic discharge (ESD), system-level ESD test, ESD protection circuit, detection circuit.**

I. INTRODUCTION

System-level electrostatic discharge (ESD) issue is an increasingly significant reliability issue in CMOS IC products [1]-[4]. This tendency results from the strict requirements of reliability test standards, such as system-level ESD test for electromagnetic compatibility (EMC) regulation. In the system-level ESD test standard of IEC 61000-4-2 [5], the electrical/electronic product must sustain the ESD level of +8kV (+15kV) under contact-discharge (air-discharge) test mode to achieve the immunity requirement of "level 4." During the system-level ESD test, the high-energy ESD-induced fast transients often cause damage or malfunction of CMOS integrated circuits (ICs) inside the equipment under test (EUT) after the system-level ESD zapping. It has been found [6] that some CMOS ICs are very susceptible to system-level ESD stresses, even though they have passed the component-level ESD specifications such as human-body-model (HBM) of ±2kV [7], machine-model (MM) of ±200V [8], and charged-device-model (CDM) of ±1kV [9].

In order to meet the EMC regulation, one effective method to improve the system-level ESD immunity is to add some discrete noise-decoupling components or board-level noise filtering networks into the printed circuit board (PCB) to decouple, bypass, or absorb the electrical transient energy under system-level ESD test, such as ferrite bead, transient voltage suppressor (TVS), or low-pass noise filters [10]-[13]. In order to reduce the cost of microelectronics system, an on-chip solution integrated with the CMOS ICs is strongly requested by IC industry [14]. The chip-level solution can be further co-designed with board-level solution in order to meet high system-level ESD specification.

In this paper, a new on-chip transient detection circuit is proposed to detect the fast electrical transients under the system-level ESD tests. The silicon chip of new proposed on-chip transient detection circuit has been fabricated in 0.18-μm CMOS process with 3.3-V devices. The experimental results have confirmed that the proposed on-chip transient detection circuit can successfully detect fast electrical transients during system-level ESD zapping.

II. TRANSIENT DETECTION CIRCUIT

A. Circuit Structure

Fig. 1 shows the proposed on-chip transient detection circuit. The RC-based circuit structure is designed to realize the transient detection function. The two-inverter latch (INV_2 and INV_3) is designed to memorize the logic state before and after system-level ESD stress. The NMOS (M_{nr}) is used to provide the initial reset function to set the initial output voltage (V_{OUT}) level to 0V. In Fig. 1, the node V_X is biased at V_{DD} and the node V_G is biased at V_{SS} during the normal operation condition. Under the system-level ESD stress, the ESD voltage has fast rise time in the order of nanosecond (ns). The voltage level of V_X has much slower voltage response than the voltage level at V_{DD} because the RC circuit has a time constant in the order of microsecond (μs). Due to the longer delay of the voltage increase at the node V_X, the PMOS device in the inverter1 (INV_1) can be turned on by the overshooting ESD voltage and conducts a voltage to the node V_G to further turn on the M_{n1} device. The turned-on M_{n1} device can pull down the output voltage level at the node V_A. Therefore, the logic level stored in the two-inverter latch can be changed to detect the system-level ESD event. The output voltage (V_{OUT}) of the proposed on-chip transient detection circuit can change from 0V to 3.3V to memorize the occurrence of system-level ESD events.

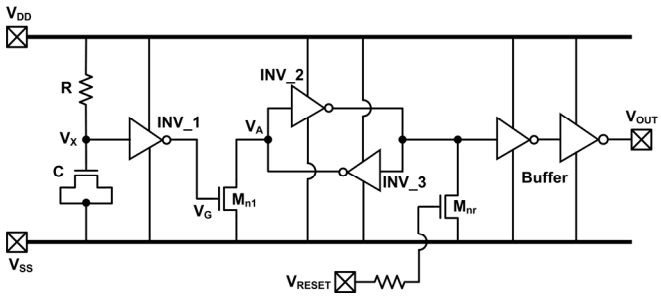

Figure 1. The proposed on-chip transient detection circuit.

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B. Measurement Setup

In the test standard of IEC 61000-4-2 [5], two test modes have been specified: air-discharge test mode and contact-discharge test mode. Fig. 2 shows the measurement setup of the system-level ESD test with indirect contact-discharge test mode, which consists of a wooden table on the grounded reference plane (GRP). In addition, an isolation plane is used to isolate the EUT from horizontal coupling plane (HCP). The HCP are connected to the GRP with two 470kΩ resistors in series.

By using the digital oscilloscope, the transient responses of CMOS ICs can be recorded and analyzed. Before each ESD zapping, the initial output voltage (V_{OUT}) of the proposed on-chip transient detection circuit is measured to make sure the correct voltage level of 0V. After each ESD zapping, the V_{OUT} voltage is measured to check the final voltage level in order to verify the detection function. Thus, the circuit performance of the proposed on-chip transient detection circuit can be evaluated with this measurement setup.

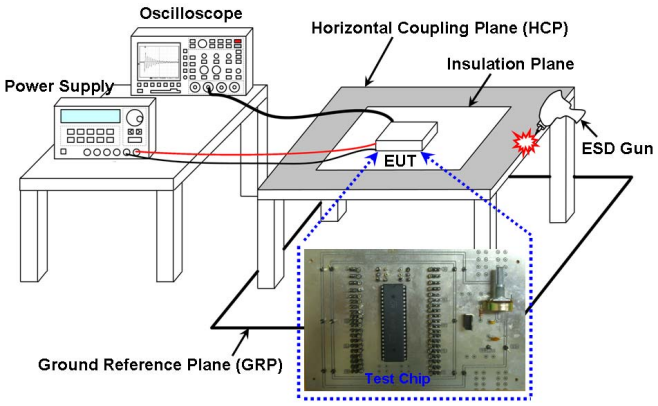


Figure 2. Measurement setup of the system-level ESD test with indirect contact-discharge test mode.

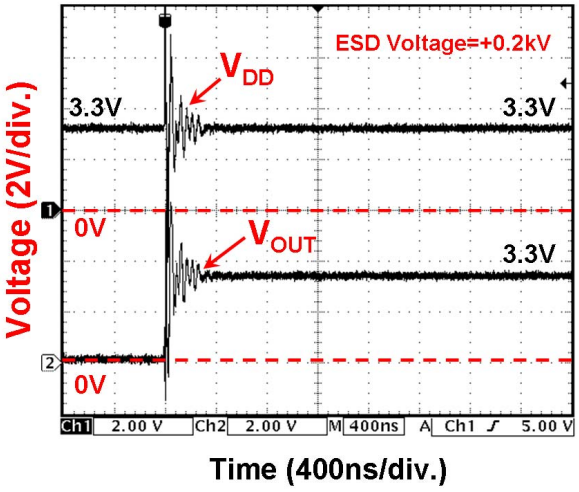
C. Measurement Results

The system-level ESD test with indirect contact-discharge test mode is used to experimentally verify circuit performance of the proposed on-chip transient detection circuit. Under system-level ESD tests, the V_{DD} and V_{OUT} transient responses are both recorded by the digital oscilloscope. This can clearly indicate whether the detection function works correctly during the system-level tests.

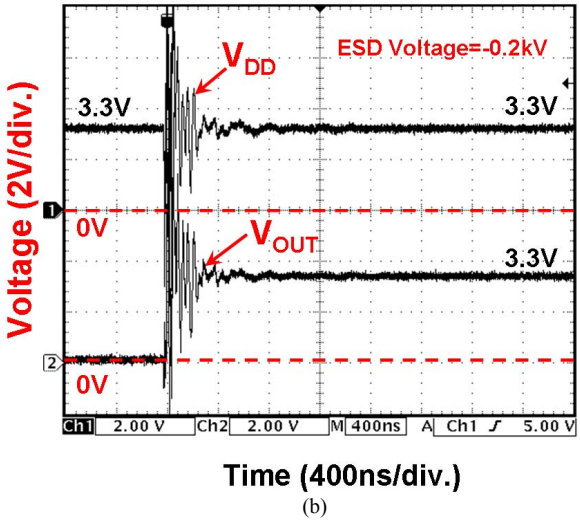
Under system-level ESD test with ESD voltage of +0.2kV zapping on the HCP, the measured V_{DD} and V_{OUT} waveforms of the proposed transient detection circuit are shown in Fig. 3(a). V_{DD} begins to increase rapidly from the normal voltage (+3.3V). As shown in Fig. 3(a), under the system-level ESD test with positive ESD voltage, V_{DD} begins to increase rapidly from 3.3V. Meanwhile, V_{OUT} begins to greatly increase with positive-going underdamped sinusoidal voltages on V_{DD} power line. Finally, the output voltage (V_{OUT}) of the proposed on-chip transient detection circuit is changed from 0V to 3.3V. As a result, the proposed on-chip transient detection circuit can detect fast electrical transient under system-level ESD test with positive ESD voltage.

Under system-level ESD test with ESD voltage of -0.2kV zapping on the HCP, the measured V_{DD} and V_{OUT} transient waveforms of the proposed transient detection circuits are shown in Fig. 3(b). As shown in Fig. 3(b), under the system-level ESD test with negative ESD voltage, V_{DD} begins to decrease rapidly from 3.3V. V_{OUT} is disturbed simultaneously with negative-going underdamped sinusoidal voltages on V_{DD} power line. Finally, V_{OUT} is pulled up to the 3.3V after the system-level ESD test with ESD voltage of -0.2kV zapping on the HCP. Therefore, the proposed on-chip transient detection circuit can detect fast electrical transient under system-level ESD test with negative ESD voltage.

The circuit performance of the proposed on-chip transient detection circuit under the system-level ESD tests has been verified by the experimental results in silicon chip. From the system-level ESD test results, with positive-going and negative-going underdamped sinusoidal voltages on power lines, the output voltages (V_{OUT}) of the proposed on-chip transient detection circuit are changed from 0V to 3.3V. Therefore, the proposed on-chip transient detection circuit can successfully detect positive and negative fast electrical transients during system-level ESD zapping.



(a)



(b)

Figure 3. Measured V_{DD} and V_{OUT} transient responses with ESD voltage of (a)+0.2kV, and (b) -0.2kV zapping on the HCP under system-level ESD test.

III. ON-BOARD BEHAVIOR WITH EMI/EMC FILTERS

From Figs. 3(a) and 3(b), it has been observed that, under the system-level ESD tests, the power line (V_{DD} pin) of CMOS IC no longer maintain its normal voltage level (+3.3V) but acts as a underdamped sinusoidal voltage signal. During the system-level ESD tests, the board-level noise filtering networks can enhance immunity of CMOS ICs by decoupling, bypassing, or absorbing ESD-induced noise voltage (energy). It has been also investigated that board-level noise filters has strong impacts to the dominant parameters of the underdamped sinusoidal voltages such as transient peak voltage, damping frequency, and damping factor. As shown in Fig. 4, in the microelectronic products, board-level noise filtering networks are often designed to locate between V_{DD} and V_{SS} pins of CMOS ICs on the PCB. To better clarify how the board-level noise filtering networks will affect these underdamped sinusoidal voltages to further enhance the transient noise detection range, several examples about the influence of board-level noise filtering networks on the proposed on-chip transient detection circuit under system-level ESD tests are given in the following.

Three types of noise filtering networks: capacitor filter, L- section RC filter, and π-section RC filter are depicted in Figs. 5(a), 5(b), and 5(c), respectively. Figs. 6(a) and 6(b) show their improvements on both minimum positive and negative ESD voltages to cause transition at the output voltage (V_{OUT}) of the proposed on-chip transient detection circuit under system-level tests.

1) Capacitor Filter

The ceramic disc capacitor with advantages of high rated working voltage (1kV), good thermal stability, and low loss at wide range of frequency is employed as the decoupling capacitor in the noise filtering network, as shown in Fig. 5(a). Wide ranges of decoupling capacitance ranging from 1pF to 10nF are used to investigate their enhancements on the ESD voltage to cause transition at the output (V_{OUT}) of the proposed on-chip transient detection circuit. As shown in Fig. 6(a), with the aid of the capacitor, the positive ESD voltage to cause transition at the output (V_{OUT}) of the proposed on-chip transient detection circuit can be significantly enhanced from +0.5kV (with decoupling capacitance of 1pF) to +1.5kV (with decoupling capacitance of 10nF). Similarly, the negative ESD voltage to cause transition at the output (V_{OUT}) of the proposed on-chip transient detection circuit can be significantly enhanced from -0.2kV (with decoupling capacitance of 1pF) to -1.7kV (with decoupling capacitance of 10nF). Under system-level tests, the minimum positive and negative ESD voltages to cause transition at the output (V_{OUT}) of the proposed on-chip transient detection circuit can be both enhanced. Thus, by choosing a decoupling capacitor with proper capacitance value, a simple first-order decoupling capacitor placed between V_{DD} and V_{SS} pins can be used to appropriately adjust the transient noise detection level of the proposed on-chip transient detection circuit under system-level ESD tests, regardless of the positive and negative ESD voltage.

2) L-section RC Filter

An L-section RC filter consisted of a resistor and a capacitor is used to investigate the enhancement on minimum ESD voltages, as shown in Fig. 5(b). The L-section RC filter can block high frequency signals into the power pins of the proposed on-chip transient detection circuit. Compared with the capacitor filter, the L-section RC filter has better ESD voltage enhancement. The positive ESD voltage to cause transition at the output (V_{OUT}) of the proposed on-chip transient detection circuit can be enhanced from +0.6kV to +2kV. The magnitudes of negative ESD voltage can be enhanced from -0.2kV to -2.1kV due to a higher insertion loss, as shown in Fig. 6(a).

3) π-section RC Filter

A third-order π-section filter is shown in Fig. 5(c). This π-section filter consists of a resistor (the same one in Fig. 5(b)) and two decoupling capacitors with equal decoupling capacitance. With the highest insertion loss among the noise filtering networks in Figs. 5(a), 5(b), and 5(c), the minimum ESD voltages can be significantly improved. The magnitude of positive (negative) ESD voltage is significantly enhanced from +0.6kV (-0.2kV) to over +5kV (-3kV), as shown in Fig. 6(a).

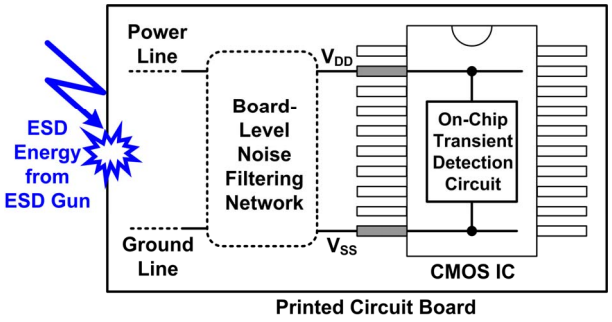


Figure 4. Board-level noise filtering networks are designed to locate between V_{DD} and V_{SS} of CMOS IC on the printed circuit board. The board-level noise filtering network can enhance the immunity of CMOS IC against system-level ESD stresses.

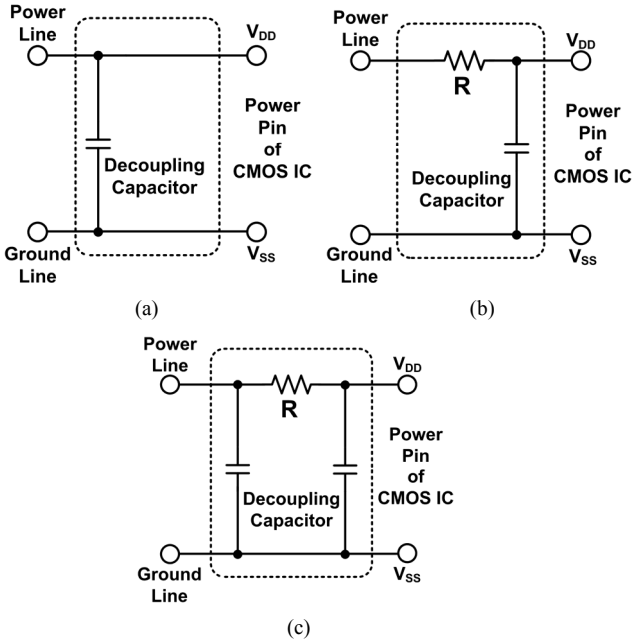


Figure 5. Three types of board-level noise filtering networks: (a) capacitor filter, (b) L-section RC filter, and (c) π-section RC filter.

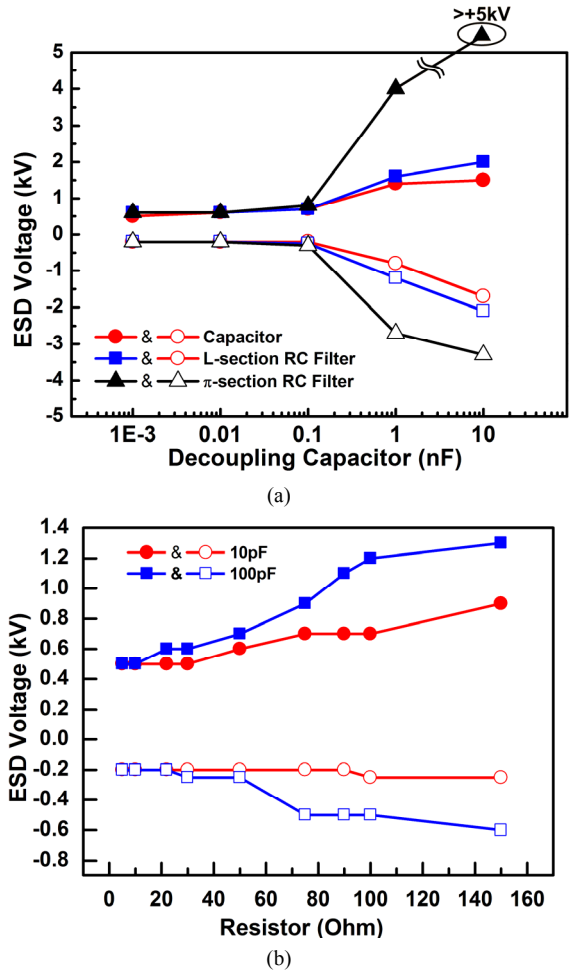


Figure 6. The relations between the ESD voltage and (a) the decoupling capacitance of three types of board-level noise filtering networks, and (b) the resistor value of L-section RC filter under system-level ESD tests.

In order to further investigate the component influence of board-level noise filtering networks under system-level ESD tests, the resistor in L-section RC filter ranging from 5Ω to 150Ω are used to investigate their enhancements on the minimum ESD voltages to cause transition at the output (V_{OUT}) of the proposed on-chip transient detection circuit. As shown in Fig. 6(b), with capacitor of 100pF, the positive ESD voltage can be enhanced from +0.5kV to +1.3kV. The magnitude of negative ESD voltage can be enhanced from -0.2kV to -0.6kV.

By investigating three types of board-level noise filtering networks to find their enhancements on minimum ESD voltages to cause transition at the output of the proposed on-chip transient detection circuit under system-level tests, it can be found that the π-section RC filter has better performance than decoupling capacitor. With the development of semiconductor process, the resistor in noise filtering network can be realized with poly resistor or N-well resistor and the decoupling capacitor can be realized with MOSFET capacitor. The RC filter can not only enhance ESD voltage level more efficiently, but also is compatible to CMOS technology for integrating the noise filtering network into silicon chips.

IV. Conclusion

A new on-chip transient detection circuit for system-level ESD protection has been implemented in 0.18-μm CMOS process with 3.3-V devices. The experimental results in silicon chip have confirmed that the proposed on-chip transient detection circuit can detect positive and negative fast electrical transients during system-level ESD zapping. By choosing proper components in noise filtering networks, the minimum positive and negative ESD voltages to cause transition at the output (V_{OUT}) of the proposed on-chip transient detection circuit under the system-level ESD tests can be significantly enhanced. From the experimental results, the π-section RC filter is better than decoupling capacitor in the noise filtering networks. The RC filter not only enhances ESD voltage more efficiently, but also is compatible to CMOS technology for integrating the noise filtering network into silicon chips. By combing with different board-level noise filtering networks, the proposed on-chip transient detection circuit can adjust the transient noise detection levels. To further improve immunity of electronic products against system-level ESD stresses, chip-level solutions can be co-designed with board-level solutions to meet high system-level ESD specification.

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