

Design on Mixed-Voltage I/O Buffers with Slew-Rate Control in Low-Voltage CMOS Process

Ming-Dou Ker, Tzu-Ming Wang, and Fang-Ling Hu

Nanoelectronics and Gigascale Systems Laboratory
Institute of Electronics, National Chiao-Tung University
1001 Ta-Hsueh Road, Hsinchu, Taiwan 300, R.O.C.

Abstract—A new design on mixed-voltage I/O buffers with slew-rate control but without gate-oxide reliability problem in low-voltage CMOS process is proposed. The proposed circuit can effectively reduce the ground bounce effects without suffering gate-oxide reliability problems and hot-carrier degradation issues. The proposed mixed-voltage I/O buffer with slew-rate control has been designed in a 0.18- μm CMOS process to meet the 1.5-V/3.3-V applications.

I. INTRODUCTION

Transistors fabricated with thin gate oxides are vulnerable to dielectric damage and reliability problems due to excessive electric fields. The difference between operating voltage and maximum allowed terminal voltages including gate-source voltage (V_{gs}), gate-drain voltage (V_{gd}) and drain-source voltage (V_{ds}) of MOS transistors have decreased drastically with the advancement of CMOS process. Also, the ground bounce effects get worse with increasing operating speed. These present special challenges for I/O designers.

Signal and power integrity are crucial problems in modern VLSI systems. Modern trends in deep sub-micron circuit designs, such as high operating frequencies, short rise/fall times, and lower supply voltage, exacerbate this problem. Output buffers provide an interface for driving mainly capacitive and inductive external loads. The capacitive load is typically composed of the bonding wire, the pin, the conductors on the PCB and the input capacitances of the connected gates. The package parasitic series inductances of the power and ground lines supplying the output buffer usually comprises the inductive load which is connected to the external power and ground rails on the PCB. A major component of the circuit noise is the inductive noise. Ground bounce, also known as simultaneous switching noise (SSN) or delta-I noise, is a voltage glitch induced at power/ground (P/G) distribution connections due to switching currents passing through either wire/substrate inductance or package lead inductance associated with power or ground rails. When the current flows through the inductance L , a voltage drop V is induced as shown in (1)

$$V = L \frac{di}{dt} \quad (1)$$

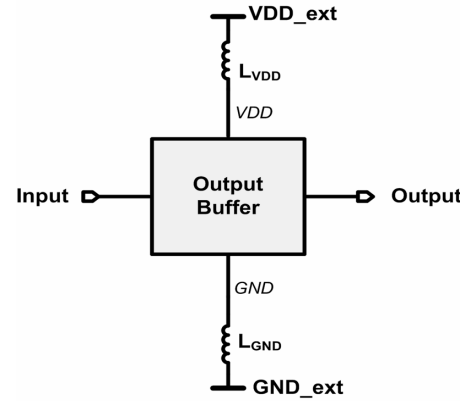


Figure 1. The model for ground bounce effect in output buffer [2].

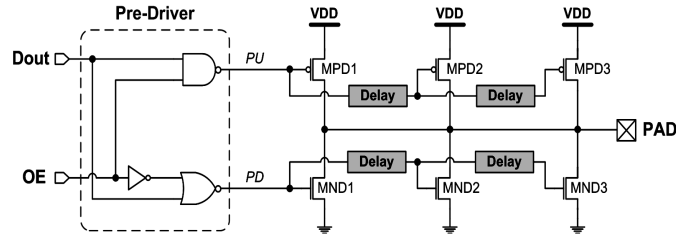


Figure 2. The output buffer with conventional slew-rate control [4].

In mixed-voltage output buffer design, the transistors sizing is imposed by DC interfacing constraints. This leads to several problems: unacceptable high current peaks which occur with the simultaneous switching of many output buffers, inductive power supply noise which results in large voltage drops, and electromagnetic interference (EMI) due to high output edge switching rates [1].

The resulting noise voltage can potentially cause spurious transitions at the inputs of devices sharing the same power and ground rails. Therefore, controlling the output voltage variations is generally required to limit the crosstalk and to reduce the inductive power supply noise. In addition, the effect of ground bounce in output buffer can be simply modeled as inductors (L_{VDD} , L_{GND}) shown in Fig. 1 [2].

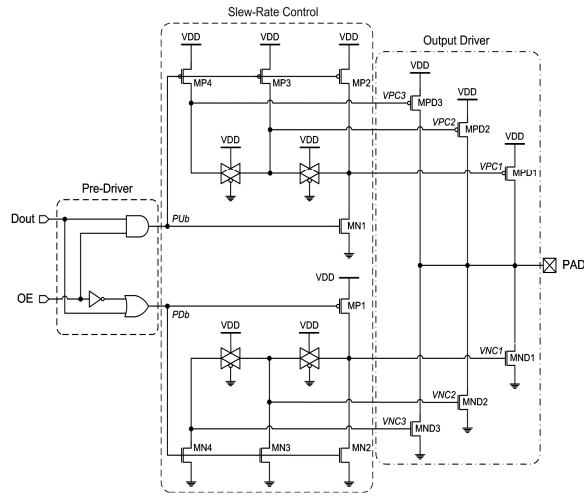


Figure 3. The output buffer with modified slew-rate control to reduce short-circuit current [4].

II. CONVENTIONAL DESIGN ON I/O BUFFERS WITH SLEW-RATE CONTROL

To solve these problems, a reduction of the slew rate in the output edges is preferred as far as the speed specification is satisfied [3]. A simple approach is to slow down the turn-on time of the output switching transistor through an access resistor to the transistor gate. Furthermore, the output driver can be divided into several parallel output drivers for ground bounce reduction and slew-rate control. An output buffer with conventional three-step slew-rate control is shown Fig. 2 [4]. The parallel output transistors of slew-rate controlled output buffer turn on progressively through delay elements implemented by resistors or transmission gates. This helps to reduce the slew rate of output buffer and therefore to reduce the ground and power bounce. The output transistors are turned off step-by-step as output transistors are turned on, and the circuit consumes unnecessary power resulting from short-circuit current. For low power consideration, modified slew-rate control topology should be developed.

Fig. 3 shows an output buffer with improved slew-rate control to reduce short-circuit current [4]. The output transistors are divided into three parts with their corresponding gate-controlled signals generated by slew-rate control. The transistors MN1 and MP1 in Fig. 3 are used to control CMOS output driver to turn it on and the pull-up signal (Pub) and pull-down signal (PDb) are the inverse of the signals, PU and PD. When the output buffer is operating in transmit (TX) mode (OE=VDD), the transmission gates are used as resistive elements to turn on each individual output transistor gradually. As the output buffer is operating in tri-state mode (OE=GND), the output transistors are quickly turned off by the transistors MP2-MP4 and MN2-MN4. As a result, this slew-rate control is compatible for low power design.

With compatibility to the earlier defined interface protocols of CMOS ICs in a microelectronics system, the chips fabricated

in the advanced CMOS processes will face to the interface of input signals with voltage levels higher than their normal supply voltage (VDD). As a result, mixed-voltage I/O buffers with only thin-oxide devices have been designed with advantages of less fabrication cost and higher operating speed to communicate the advanced circuits with the earlier ones [5].

Typical I/O buffers with slew-rate control, however, are usually not suitable for mixed-voltage applications because the gate-oxide breakdown issue [6] and hot-carrier degradation [7]. In [8], the mixed-voltage I/O buffers without gate-oxide reliability issue and hot-carrier reliability problem had been verified in a 0.18- μm 1.8-V CMOS process with only thin-oxide devices; however, the circuit did not contain slew-rate control. Therefore, a new mixed-voltage I/O buffer with slew-rate control but without gate-oxide reliability problem and hot-carrier degradation is strongly requested by IC industry.

III. PROPOSED MIXED-VOLTAGE I/O BUFFERS WITH SLEW-RATE CONTROL

The proposed mixed-voltage I/O buffer with slew-rate control but without gate-oxide reliability problem (HCPMXIO-SR) is shown in Fig. 4. The hot-carrier-prevented circuits for transistors MND4-6 and MN3 have been shown in Fig. 4 (b) and 4 (c). The NMOS transistors MNSR6-MNSR8 are used to protect transistors MPSR2-MPSR4 from gate-oxide degradation and to avoid leakage currents as the HCPMXIO-SR receives $2\times\text{VDD}$ input signals. The gate-controlled signal of transistors MPSR6-MPSR8, PDH, is high-level version of pull down signal, PD, shifted by the level shifter. Furthermore, the transistor MNSR2 is used to protect transistor MNSR1 from gate-oxide reliability and hot-carrier degradation as the mixed-voltage I/O buffer receives $2\times\text{VDD}$ input signal. Since the transmission gates MNR1/MPR1 and MNR2/MPR2 are mainly used to propagate 0-V signal to turn on PMOS output transistors, MPD1-MPD3, one-after-one, the PMOS transistors MPR1 and MPR2 can be omitted and consequently only NMOS transistors are used as resistive elements. As a result, the resistive elements do not suffer gate-oxide reliability issue.

Similarly, the transistors MNR3 and MNR4 can be omitted. When the mixed-voltage I/O buffer receives 0-V input signal at I/O PAD, the PD signal is set to 0V and consequently PDH signal is set to VDD. At this time, the gate-controlled signals of transistors MPD1-MPD3, VPC1-VPC3, are biased at "VDD-V_{th}" due to weakly turned-on transistors MPSR6-8, thus results in subthreshold leakage currents on transistors MPD1-MPD3. To avoid this problem, the gate-controlled signals of transistors MPD1-MPD3 are pulled up to VDD through the transistors MP34-MP36 in Fig. 4 as 0-V input signal is received at I/O PAD. Note that the bulks of PMOS devices and NMOS devices in the new slew rate control are connected to VDD and GND, respectively. The bulks of transistors from MP31 to MP36 are connected to the n-well self-biased circuit (nwell).

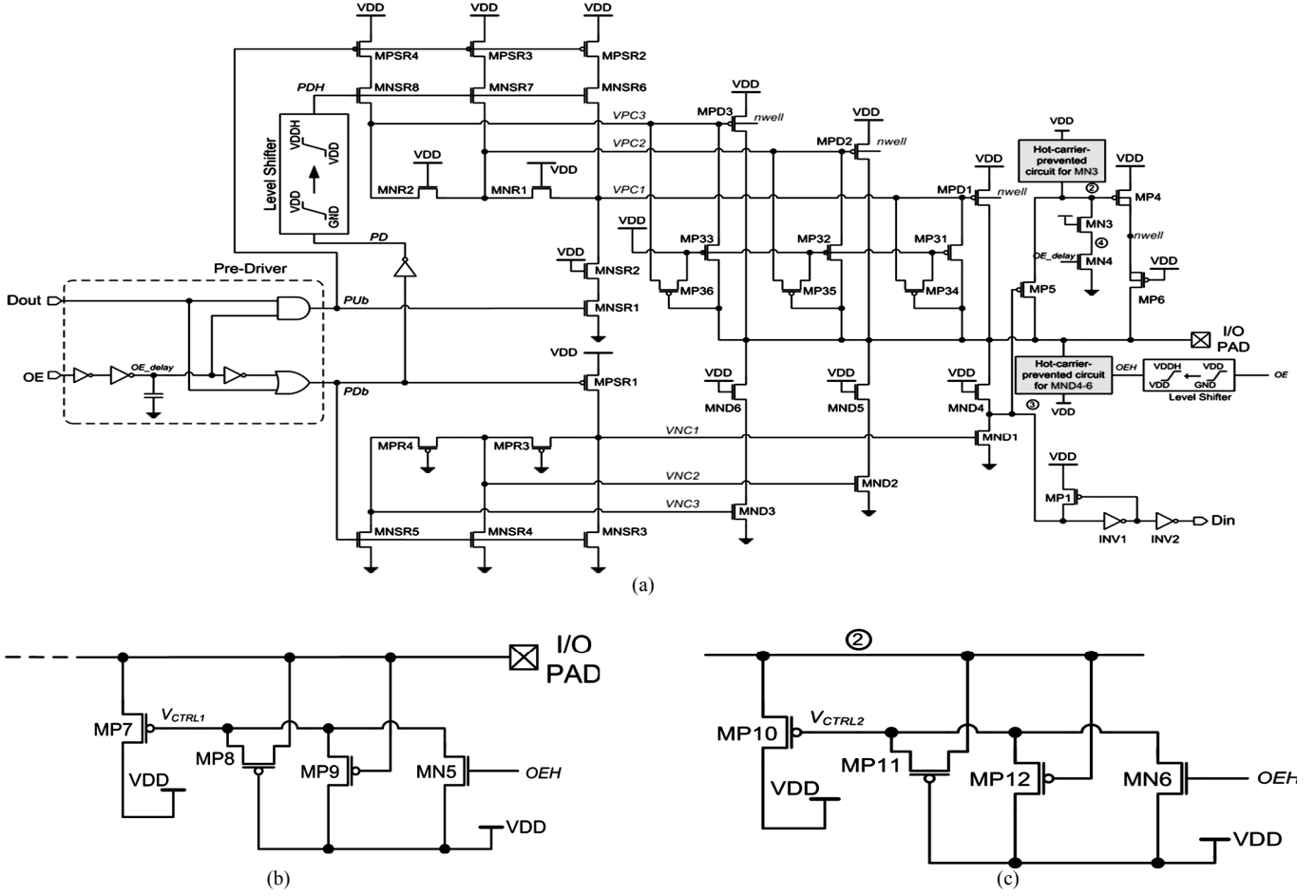


Figure 4. (a) The proposed mixed-voltage I/O buffers with slew-rate control but no gate-oxide reliability and no hot-carrier degradation issues (HCPMXIO-SR). (b) The hot-carrier-prevented circuit for transistor MND4-6, and (c) the hot-carrier-prevented circuit for transistor MN3.

The operations of HCPMXIO-SR are listed in Table I. When the HCPMXIO-SR is operated in receive (RX) mode, the PUB and PDB signal are 0V and VDD, respectively, to turn off output driver. In the meanwhile, the PDH signal is set to VDD by level shifter. The transistors MP31 and MP34 comprise the gate tracking circuit of transistor MPD1 as the I/O buffer is operating in receive mode. Similarly, transistors MP32/MP35 and MP33/MP36 are the gate-tracking circuit of transistor MPD2 and MPD3, respectively. As $2xVDD$ input signal is received at I/O PAD, the VPC1, VPC2, and VPC3 are set to $2xVDD$ through transistors MP31, MP32, and MP33. On the contrary, the VPC1, VPC2, and VPC3 are set to VDD through transistors MP34, MP35, and MP36. As a result, the input signals can be received successfully without the problems of gate-oxide reliability and leakage current.

If the mixed-voltage I/O buffer is transmitting 0-V output signal, the PDB signal is set to 0V, and consequently transistor MPSR1 is turned on to propagate VDD signal to gate terminals of transistors MND1-MND3 through transistors MPR3 and MPR4. In the meanwhile, the PDH signal is set to $2xVDD$, thus the VDD signals can be transmitted to the gate terminals of transistors MPD1-MPD3 through transistors MNSR6-MNSR8 successfully. As a result, transistors MPD1-MPD3 are quickly turned off. On the other hand, if VDD

output signal is transmitted from DOUT to I/O PAD, the PUB signal is pulled up to VDD to turn on transistor MNSR1. The 0-V signal consequently is propagated to VPC2 and VPC3 through transistors MNR1 and MNR2. The PMOS transistors MPD1, MPD2, and MPD3 are turned on one-after-one to pull up I/O PAD to VDD. In the same condition, the PDB signal is set to VDD to turn on transistors MNSR3-MNSR5, thus NMOS transistors MND1, MND2, and MND3 are quickly turned off. As the aforementioned descriptions, this HCPMXIO-SR can be successfully operated in both receive mode and transmit mode without suffering gate-oxide reliability and hot-carrier degradation.

IV. SIMULATION RESULTS

The HCPMXIO-SR is designed to meet 1.5-V/3.3-V applications. The HCPMXIO-SR has been verified in a $0.18\text{-}\mu\text{m}$ CMOS process by SPICE simulation. The simulated waveforms of the new proposed HCPMXIO-SR with an operating speed of 266 MHz in transmit mode are shown in Fig. 5. When the I/O buffer transmits VDD output signal to I/O PAD, the gate-controlled signals of MPD1-MPD3, VPC1, VPC2, and VPC3, are pulled to 0V one-after-one. In the meanwhile, the gate-controlled signals of MND1-MND3, VNC1, VNC2, and VNC3, are pulled down to 0V to turn off MND1-MND3 quickly. On the contrary, when 0-V output

signal is transmitted to I/O PAD, the VPC1, VPC2, and VPC3 are quickly pulled up to VDD to turn off MPD1-MPD3. The VNC1, VNC2, and VNC3 are progressively pulled up to VDD to turn on MND1-MND3. As a result, the HCPMXIO-SR successfully transmits data with a reduced slew rate.

The simulation results of the HCPMXIO-SR and HCPMXIO which has no slew-rate control are summarized in Table II. The propagation delay and rise/fall time of this HCPMXIO-SR are larger than those of the HCPMXIO. Also, the driving currents of HCPMXIO-SR are smaller than those of the HCPMXIO due to the slew-rate control. The power consumption of this HCPMXIO-SR is larger than that of HCPMXIO due to the additional slew-rate control circuit.

V. CONCLUSION

The new proposed mixed-voltage I/O buffers with slew-rate control but without gate-oxide reliability and hot-carrier degradation problem has been designed in a 0.18- μ m CMOS process to meet the 1.5-V/3.3-V applications, which can be successfully operated in both receive mode and transmit mode with slew-rate control to reduce power/ground bounce.

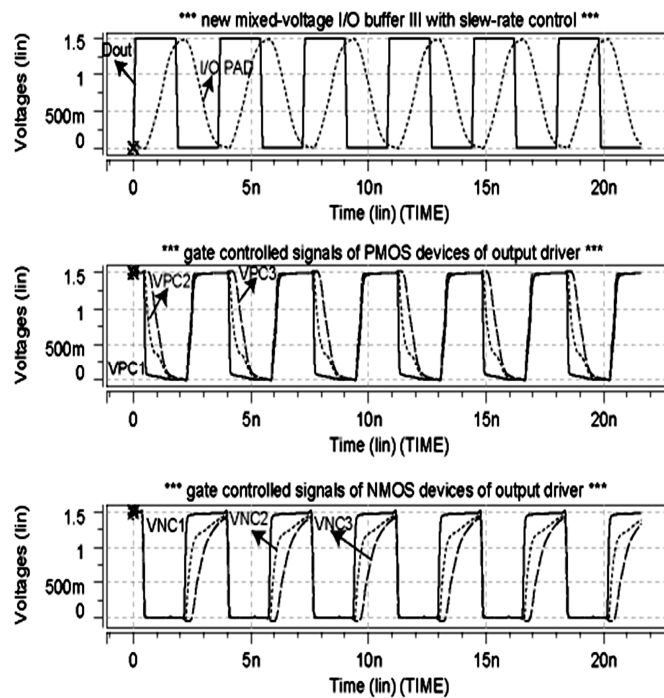


Figure 5. The simulated waveforms on the corresponding nodes in the proposed HCPMXIO-SR operating at 266 MHz when transmitting 0V-to-1.5V output signals to I/O PAD.

TABLE I. THE OPERATIONS OF THE PROPOSED HCPMXIO-SR

Parameters	Receive		Transmit	
I/O Pad	Low (0V)	High (2xVDD)	Low (0V)	High (VDD)
PUB	0V	0V	0V	VDD
PDb	VDD	VDD	0V	VDD
PDH	VDD	VDD	2xVDD	VDD
VPC1-VPC3	VDD	2xVDD	VDD	0V
VNC1-VNC3	0V	0V	VDD	0V

TABLE II. THE SIMULATION RESULTS OF THE HCPMXIO AND HCPMXIO-SR

Parameters	HCPMXIO	HCPMXIO-SR
Slew-Rate Control	No	Yes
I_{OL} at $V_{OL}=0.15$ V	7.1 mA	6.7 mA
I_{OH} at $V_{OH}=1.35$ V	6.4 mA	6.2 mA
T_{rise} at RX Mode	453 ps	454 ps
T_{fall} at RX Mode	417 ps	420 ps
T_{pr} at RX Mode	715 ps	702 ps
Power Consumption at TX Mode	28 μ W/MHz	29 μ W/MHz
T_{rise} at TX Mode	702 ps	958 ps
T_{fall} at TX Mode	708 ps	938 ps
T_{pt} at TX Mode	815 ps	925 ps
Power Consumption at TX Mode	59 μ W/MHz	66 μ W/MHz

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