Optimization on NMOS-Based Power-Rail ESD Clamp Circuits with Gate-Driven Mechanism in a 0.13-μm CMOS Technology

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***Abstract*—NMOS-based power-rail ESD clamp circuits with gate-driven mechanism have been widely used to obtain the desired ESD protection ability. All of them are based on a similar circuit scheme with 3-stage inverters to drive the ESD clamp NMOS transistor with large device dimension. In this work, the designs with 3-stage-inverter and 1-stage-inverter controlling circuits have been studied to verify the optimal circuit schemes in NMOS-based power-rail ESD clamp circuits.**

I. INTRODUCTION

ElectroStatic Discharge (ESD) protection has become a troublesome task on the reliability of CMOS integrated circuits fabricated in the nanoscale CMOS technologies. The efficient power-rail ESD clamp circuit is an essential component to achieve whole-chip ESD protection design in IC products [1]-[3]. It not only can improve ESD robustness of VDD-to-VSS ESD stress, but also can significantly enhance ESD robustness of the ESD stresses between input/output and VDD/VSS, and between pin-to-pin ESD stresses [2]. Furthermore, to efficiently protect the core circuits realized with much thinner gate oxide in nanoscale CMOS technology, some studies had reported efficient power-rail ESD clamp circuits with novel circuit skills [3]-[6]. All of them were based on the power-rail ESD clamp circuits with gate-driven mechanism which was basically implemented by a RC-based ESD-transient detection circuit including a controlling circuit [1]-[6], as illustrated in Fig. 1. Besides, those works also adopted the power-rail ESD clamp devices with no snapback operations to obtain excellent turn-on efficiency. NMOS transistors had always been used as power-rail ESD clamp device without snapback. No snapback means that the huge ESD current was discharged by the channel current of the NMOS transistors. Therefore, those NMOS transistors in the power-rail ESD clamp circuits were traditionally drawn with huge channel width of several-thousand micrometer to achieve the no snapback operation. They were often called as Big FET (BFET) in some previous publications.

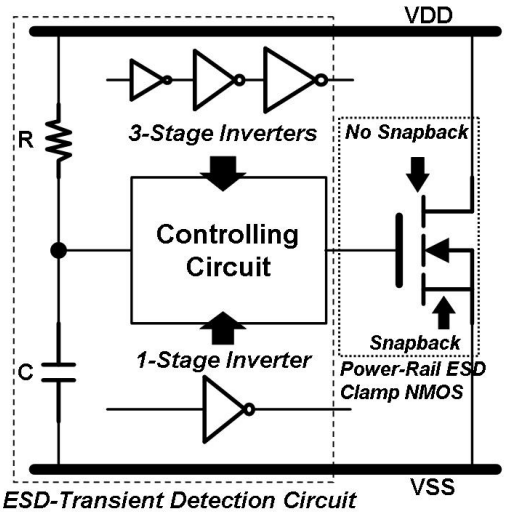

Figure 1. Typical design scheme for power-rail ESD clamp circuit.

The RC-based ESD-transient detection circuit was used to distinguish ESD-stress conditions from normal circuit operation conditions due to the difference in the rise time between these two conditions [1], [2]. In addition, 3-stage inverters, which were adopted as a function of taper buffer [7]-[11], usually performed the controlling circuit to efficiently turn-on or turn-off the BFET, which has large capacitive load from the NMOS transistor with a huge channel width in power-rail ESD clamp circuit, as shown in Fig. 1. The taper buffers, which are the multiple inverter stages with cascaded arrangement, are constantly applied to drive the large load capacitance under a desirable propagation delay and power consumption [7]-[9]. However, such design concerns are not always appropriate to the function of the controlling circuits in the power-rail ESD clamp circuits because of two main reasons. First, the controlling circuits are

only required to propagate a unity signal, such as logical high or logical low, in order to turn on the main ESD clamp devices under ESD-stress conditions, but they are not required to propagate a dynamic signal or alternating logic under normal circuit operation conditions. Second, the controlling circuits are always biased at the static off state under the normal circuit operation conditions in the power-rail ESD clamp circuits. Some circuit performances, such as short-circuit dissipation and propagation delay, would not be needed in the controlling circuits with tapered buffer arrangements. Therefore, the controlling circuits with tapered buffer concerns should be unnecessary and even be unsuitable for power-rail ESD clamp circuits.

The comparison between 1-stage and 3-stage inverters in the controlling circuits has been studied in this work. The circuit performances and characteristics of both controlling circuits in power-rail ESD clamp circuits are measured and compared under ESD-stress conditions and normal circuit operation conditions. According to these experimentally measured results, the optimized design schemes of controlling circuits for power-rail ESD clamp circuits can be evaluated.

II. Implementations of the Power-Rail ESD Clamp Circuits with Different Controlling Circuits

Both controlling circuits, which are 1-stage inverter and 3-stage inverters, are respectively arranged to command two different power-rail ESD clamp devices of NMOS transistors. One of the ESD clamp NMOS transistors has a layout style with minimized drain-contact-to-poly-gate spacing and no silicide blocking on its drain-side diffusion. This NMOS transistor, which is the Big FET (BFET), will be expected to have no snapback operation. However, the other one has a totally different layout style with extended drain-contact-to-poly-gate spacing and silicide blocking on its drain-side diffusion. It is a traditional ESD clamp NMOS transistor with snapback operation. It has been proven that the parasitic npn bipolar transistor was turned on to induce the snapback phenomena in such ESD clamp NMOS transistor [12], [13].

TABLE I The Designs of the Power-Rail ESD Clamp Circuits

Designs	Controlling Circuits	Power-Rail ESD Clamp Devices
Tradition_3_INV	3-Stage Inverters	NMOS transistor with snapback
Tradition_1_INV	1-Stage Inverter	NMOS transistor with snapback
BFET_3_INV	3-Stage Inverters	NMOS transistor with no snapback
BFET_1_INV	1-Stage Inverter	NMOS transistor with no snapback

These two ESD clamp NMOS transistors with different layout style had been designed to occupy the same silicon area. Therefore, the total channel width of the ESD clamp NMOS transistor with snapback operation is 624 μm, whereas that of the BFET is about 2600 μm. In addition, the RC time constant in this work is identically designed about 200 ns to achieve desired operation. Finally, four combinations of these two different ESD clamped NMOS transistors and those two different controlling circuits were compared in order to realize the influence of the controlling circuits on the power-rail ESD clamp circuits with snapback NMOS transistor and no snapback NMOS transistor, as shown in Table I. This testchips are fabricated in 0.13-μm 1.2-V CMOS process.

III. Experimental Results and Discussions

A. DC Leakage Current

Power-rail ESD clamp circuits must be kept off avoiding unnecessary VDD-to-VSS leakage currents under normal circuit operation conditions. However, the power-rail ESD clamp devices with NMOS transistors always have huge device dimension to achieve the required ESD robustness, so they could be a leakage concern, especially in nanoscale CMOS technologies. The leakage currents of the four power-rail ESD clamp circuits are shown in Fig. 2. According to the measured results in Fig. 2, the leakage currents of the designs with traditional ESD clamp NMOS transistors are 3-times less than those of the designs with BFET due to the large channel widths in the design with BFET. In addition, there is no obvious difference of the leakage currents between the two controlling circuits in the same ESD clamp NMOS transistors.

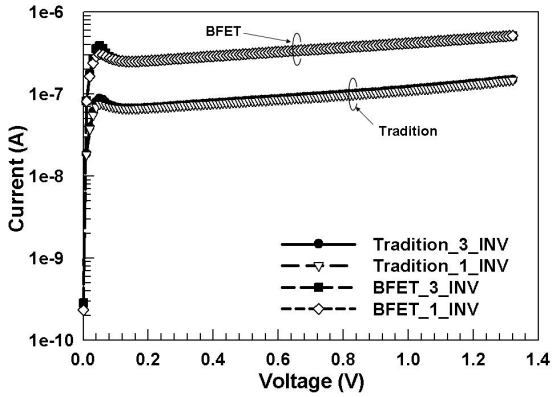

Figure 2. DC leakage currents of the power-rail ESD clamp circuits with different designs.

B. Turn-On Verifications under ESD-Like Conditions

To observe the turn-on efficiency of the power-rail ESD clamp circuits, 2.4-V ESD-like voltage pulse with 2-nano-seconds (ns) rise time was applied on the VDD terminals with VSS terminals grounded. The voltage pulse with a rise time of 2 ns and duration of 600 ns to simulate the human-body-model (HBM) ESD [14] pulse is generated from a pulse generator (HP8110A). The sharp-rising edge of the ESD-like voltage pulse will trigger on the ESD clamp NMOS transistors to degrade the voltage waveform on VDD terminals. The measured results are shown in Fig. 3. The designs with traditional ESD clamp NMOS transistor and BFET, both of which have the 1-stage inverter in controlling circuits, presented similar voltage waveforms under 2.4-V ESD-like stress. Besides, the design with traditional ESD clamp NMOS transistor having the 3-stage inverters in controlling circuits clamped the overshoot voltage pulses to a lower voltage level under first 300 ns of 2.4-V ESD-like stress. However, the BFET design with 3-stage inverters showed an excellent ability to clamp the overshoot voltage pulses to a very low voltage level. According to the measured results, the 3-stage

inverters in controlling circuits seem an optimal candidate, especially in the design with BFET.

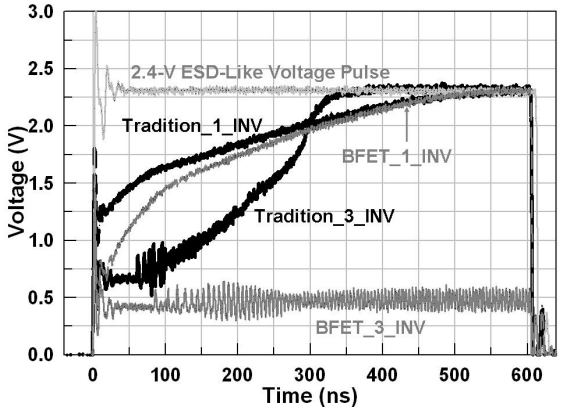

Figure 3. The voltage waveforms when 2.4-V ESD-like voltage pulses were applied to the VDD terminals of the different power-rail ESD clamp circuits.

C. TLP I-V Characteristics and HBM ESD Robustness

The Transmission Line Pulse (TLP) [15] measured I-V characteristics of the power-rail ESD clamp circuits are shown in Figs. 4 (a) and 4(b). This TLP system has a 100-ns pulse width and 10-ns rise time. The TLP I-V curves can be simply discriminated between the design with traditional ESD clamp NMOS transistor and BFET.

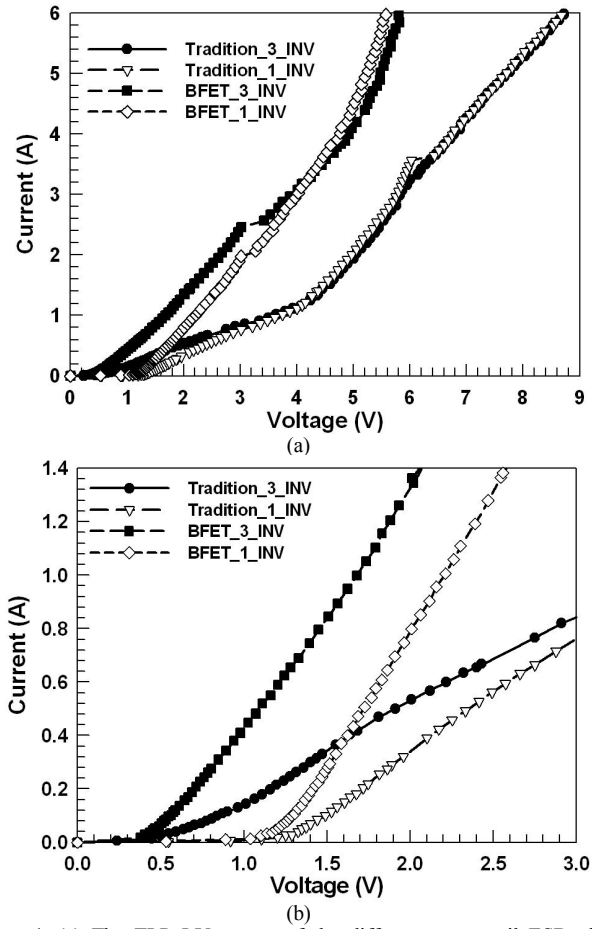

Figure 4. (a) The TLP I-V curves of the different power-rail ESD clamp circuits. (b) The zoomed-in view of (a) around the low-current region.

Although the second breakdown currents of these four designs achieved over 6 A, but the difference of on resistance (Ron) clearly separated the designs with traditional ESD clamp NMOS transistor from those with BFET. In addition, the controlling circuits with 3-stage inverters can enhance the turn-on efficiency, such as trigger voltage and on resistance, under the low current region in both traditional and BFET designs, as shown in Fig. 4(b). The enhancement of the 3-stage inverters in controlling circuit is especially emphasized on the designs with BFET. However, the influence of the different controlling circuits is gradually indistinct and lost on the turn-on efficiency under the high current region in these two designs. The phenomena can be attributed to the translations of the discharging paths. The currents conducted through the channel layers of the ESD clamp NMOS transistor under the low current region, and they will discharg by the parasitic npn bipolar transistors in the ESD clamp NMOS transistor. Such translations can be proven by the obvious turning points of the TLP I-V curves on about 4 V in the designs with tradition ESD clamp NMOS transistor. Since the designs with BFET can efficiently provide a lower impedance channel layers, the translations of the discharging paths could not be clearly observed and defined in TLP I-V curves.

The HBM ESD robustness of the different power-rail ESD clamp circuits are presented in Table II. The power-rail ESD clamp circuit with 3-stage inverters and BFET designs possessed the highest HBM ESD robustness of 7 kV. However, the ESD robustness of the design with traditional ESD clamp NMOS transistor collocating 3-stage inverters is the lowest (below 6 kV) among all ESD testing results. According to the measured results of the TLP I-V characteristics and HBM ESD robustness, the 3-stage inverters in controlling circuits seem to have no obvious advantage for the application of power-rail ESD clamp circuits.

TABLE II HBM ESD ROBUSTNESS OF THE POWER-RAIL ESD CLAMP CIRCUITS

Designs of the Power-Rail ESD Clamp Circuits	HBM Positive	HBM Negative
Tradition_3_INV	5.5 kV	> 8.0 kV
Tradition_1_INV	6.5 kV	> 8.0 kV
BFET_3_INV	7.0 kV	> 8.0 kV
BFET_1_INV	6.5 kV	> 8.0 kV

D. Power-On Conditions

In general, the normal VDD power-on voltage waveform has a rise time in the order of milli-second (ms). Due to such a slow rise time in normal power-on conditions, the ESD-transient detection circuits with a μs-order RC time constant can distinguish the power-on signal to keep the ESD clamp NMOS transistor off. All of the power-rail ESD clamp circuits in this work can successfully achieve this desirable task under ms-order power-on conditions. Nevertheless, the power-rail ESD clamp circuits with RC-based ESD transient detection circuits were easily mis-triggered on to cause themselves into a "latch-on" state under the fast power-on conditions [5], [6] or transient noise on VDD power lines [16]. In this work, the four different power-rail ESD clamp circuits were applied a 1.2-V voltage pulse with 100-ns rise time and a 3.6-V voltage

pulse with 500-ns rise time, both of which are used to simulate the fast power on and transient noise, to attain their immunities from the mis-trigger and latch-on state. The measured results are respectively shown in Figs. 5(a) and 5(b). Unfortunately, the power-rail ESD clamp circuits with 3-stage inverters presented a worse immunity from mis-trigger under the 1.2-V fast power-on testing condition. Besides, the design with 3-stage inverters and BFT will mis-trigger on and into latch-on state under both 1.2-V and 3.6-V fast power-on testing conditions. There is an abnormal mechanism to contribute a positive feedback and to trigger the occurrence of the latch-on event.

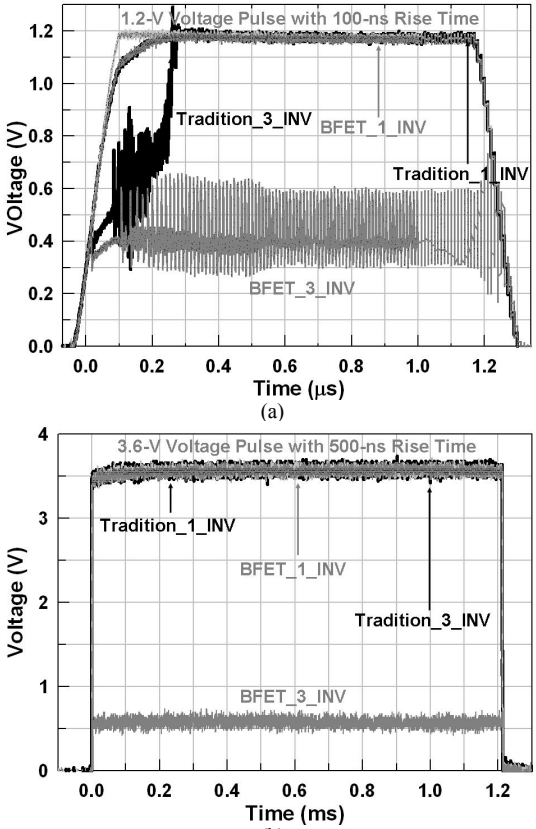

Figure 5. The voltage waveforms when (a) 1.2-V and (b) 3.6-V voltage pulses with 100-ns and 500-ns rise time, respectively, were applied to the VDD terminals of the different power-rail ESD clamp circuits.

This latch-on phenomenon has been analyzed by the emission microscope with InGaAs focal plane arrays (FPA) detector to be attributed to the abnormal mechanism of the voltage drop between the two terminals of the n-well resistance. In general, the n-well resistance is usually regarded as an optimal choice in the RC-based ESD-transient detection circuit to obtain an adequate resistance and a sufficient RC-time delay. A few electrons would be captured by this n-well resistance since this n-well resistance could be performed as the guard ring of the minority to capture the minority carriers (electrons) in the p-substrate [17]. Although the n-well resistance has been surrounded by the N+/n-well minority guard rings connecting to VDD, some escaped electrons were still captured by the n-well resistance to induce the voltage drop between the two terminals of the n-well resistance in the design with 3-stage inverters and BFT. The further results of the failure analysis will be exhibited in the presentation.

IV. Conclusion

The designs with 3-stage-inverter and 1-stage-inverter controlling circuits have been studied to verify the optimal design schemes in NMOS-based power-rail ESD clamp circuits. In addition, two ESD clamp NMOS transistors, having snapback and no snapback operations, also were co-designed with different controlling circuits to realize the impact on their required performance. According to the experiments and analyses, the 3-stage inverters can slightly increase the ESD robustness, but they also can dramatically sacrifice the mis-trigger and latch-on immunity. The 1-stage inverter should be an appropriate and reliable candidate for the power-rail ESD clamp circuits.

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