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Investigation on Discharge Current Waveforms in Board-Level CDM ESD Events With Different Board Sizes

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Biography of Presenter

The presenter, Yuan-Wen Hsiao, is currently a Ph.D. candidate at Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan.

His current research topics include RF circuit design, ESD protection design for RF circuit, and CDM ESD issues in ICs.

Abstract

- **Board-level CDM** ESD event occurs when the charged PCB touches to ground. The discharging current may flow through the IC attached to it.
- The board-level CDM ESD event causes severe impacts on reliability of IC products because of the huge ESD current larger than that of the chip-level CDM ESD event.
- An experiment is performed to compare the board-level CDM ESD current waveforms under different PCB sizes, charged voltages, and series resistances.

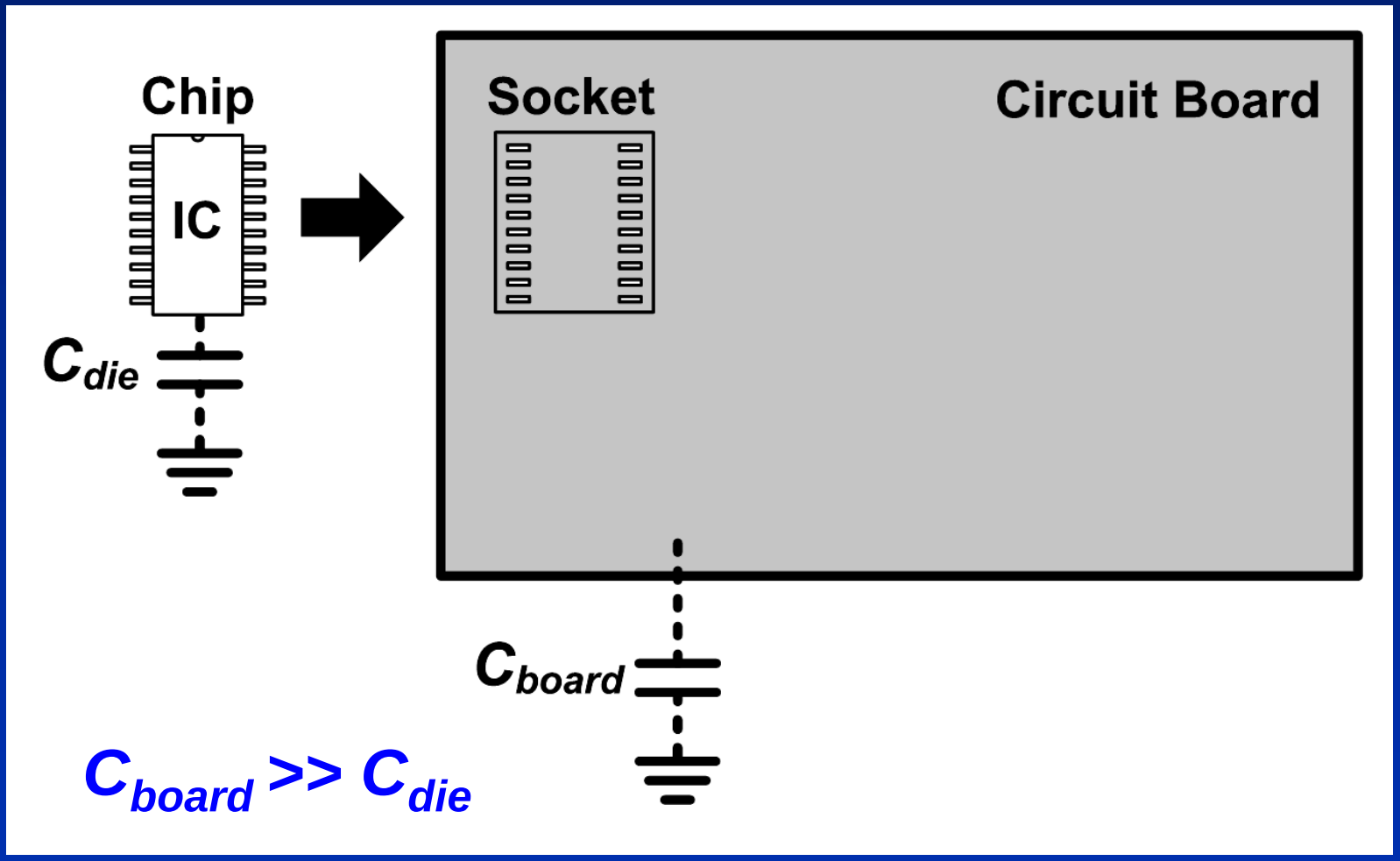
Purpose of This Work

- It has been reported that after performing the field-induced CDM ESD test for the IC attached to PCB, the failure location is the same as the customer returned ICs.
- The real-world charged-board-model (CBM) ESD damage can be duplicated by the board-level CDM ESD test.
- In this work, the mechanisms of board-level CDM ESD event under different conditions are investigated.

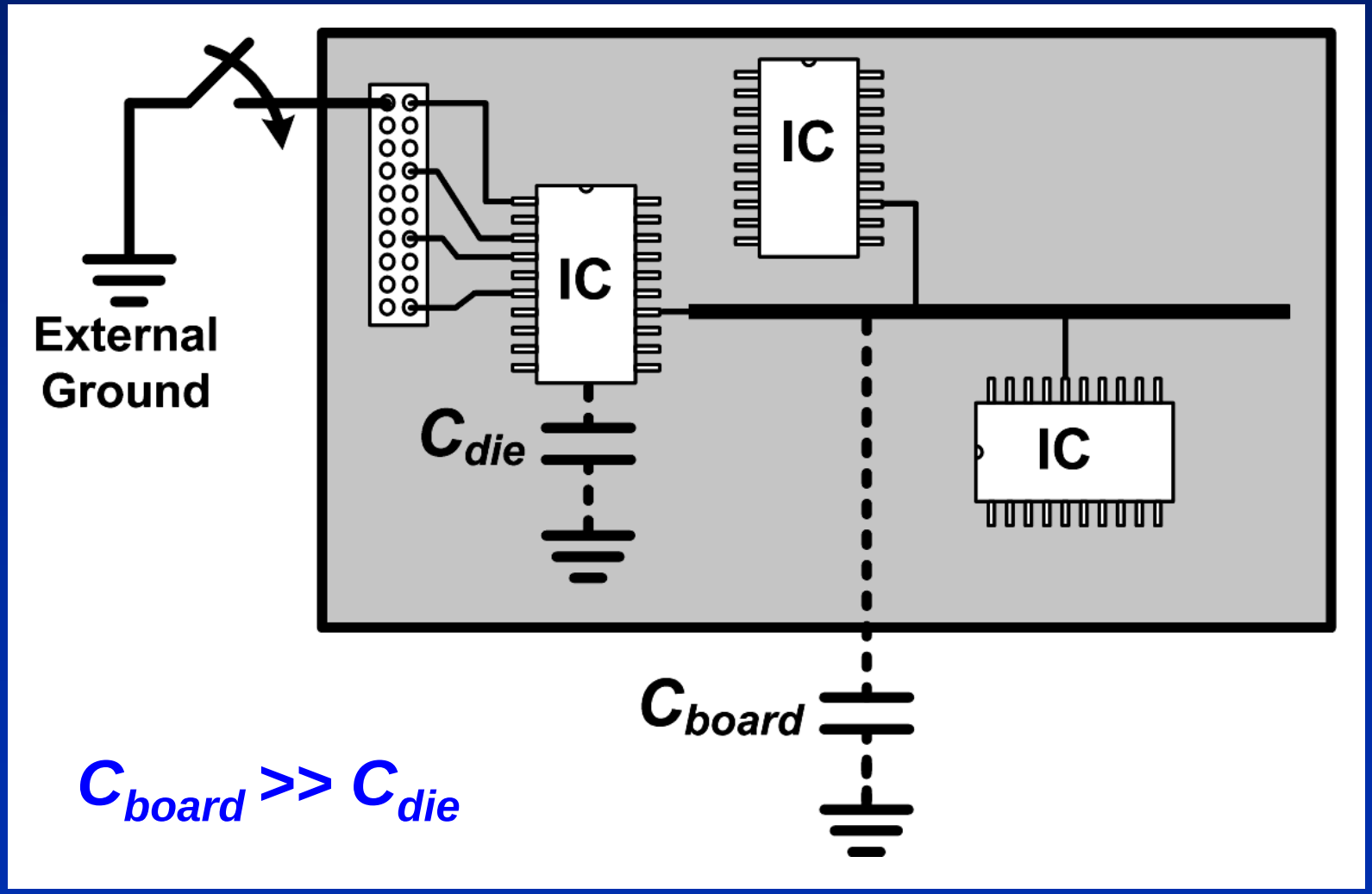
Outline

- Introduction
- Board-Level CDM ESD Test Setup
- Experimental Results
- Reducing Board-Level CDM Current by Series Resistance
- Conclusions

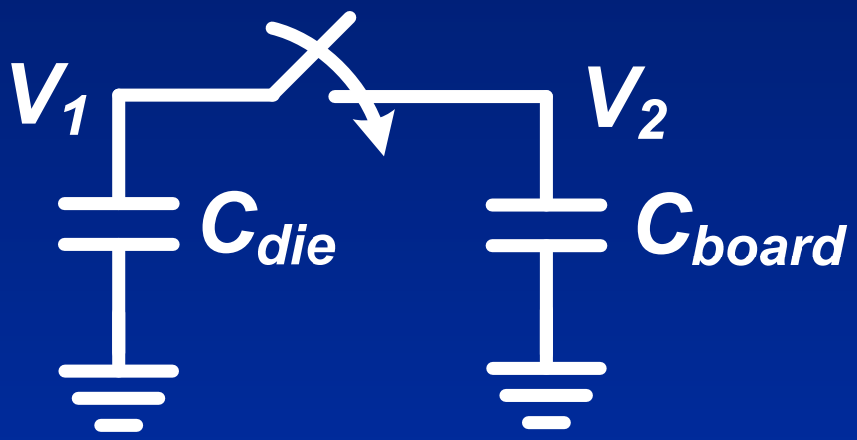
CDM ESD Event During Chip Attaching to Circuit Board



Board-Level CDM ESD Event During Module Test



Charge Redistribution During Board-Level CDM ESD Event



- Final Voltage Across Each Capacitor:

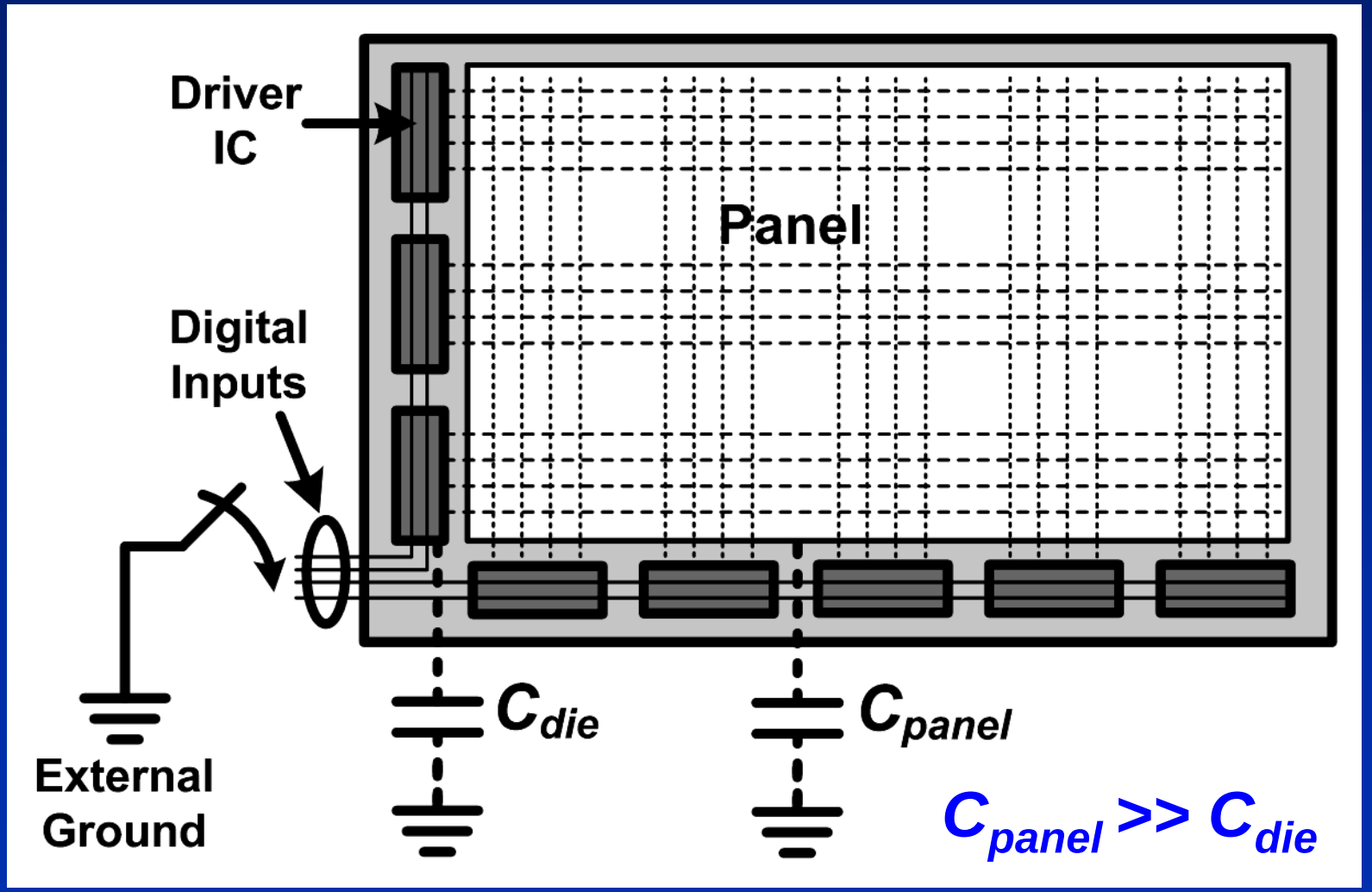
$$\frac{C_{die} \times V_1 + C_{board} \times V_2}{C_{die} + C_{board}}$$

$C_{board} >> C_{die}$

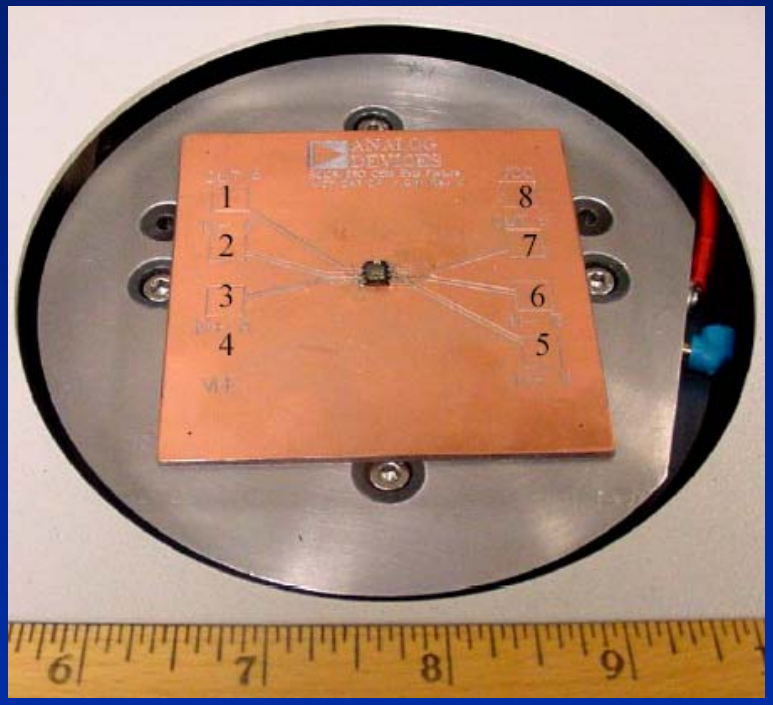
$\Delta Q = C \times \Delta V$ and $i = \frac{dQ}{dt}$

➡ Huge current will flow through IC during board-level CDM ESD events.

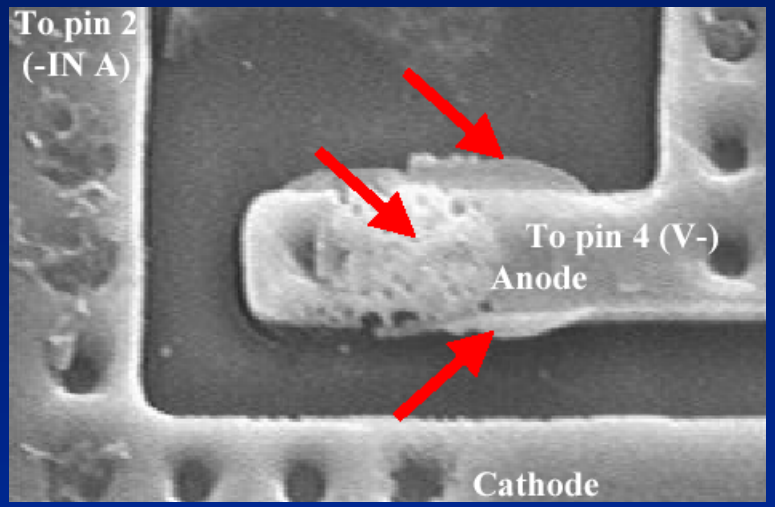
Panel-Level CDM ESD Event During Panel Function Test



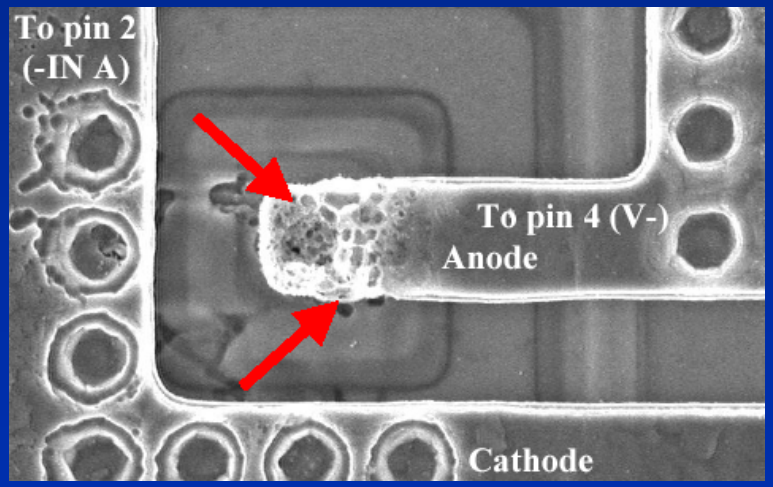
Board-Level CDM ESD Failures (1)



Field-Induced CBM Test Setup
(Op Amp IC)



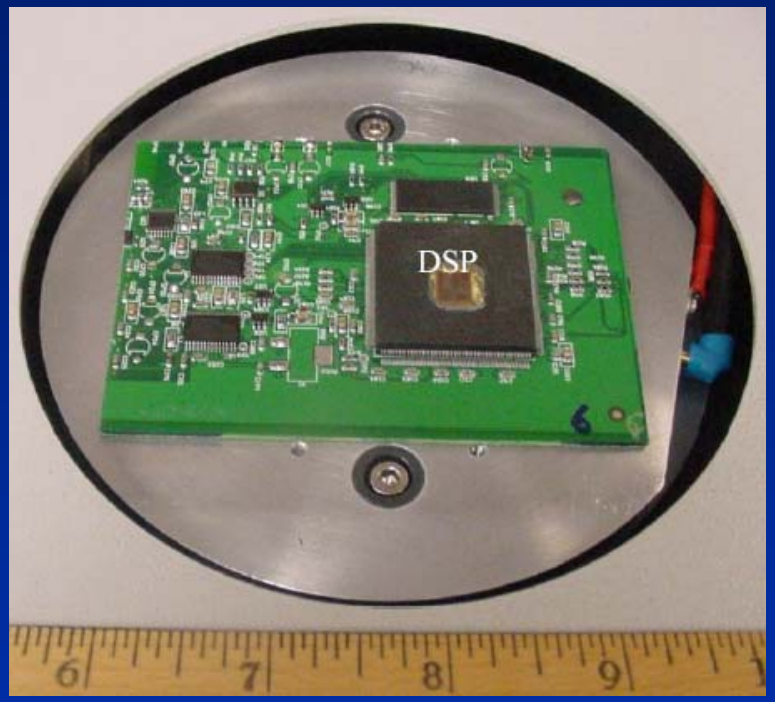
Customer's Return



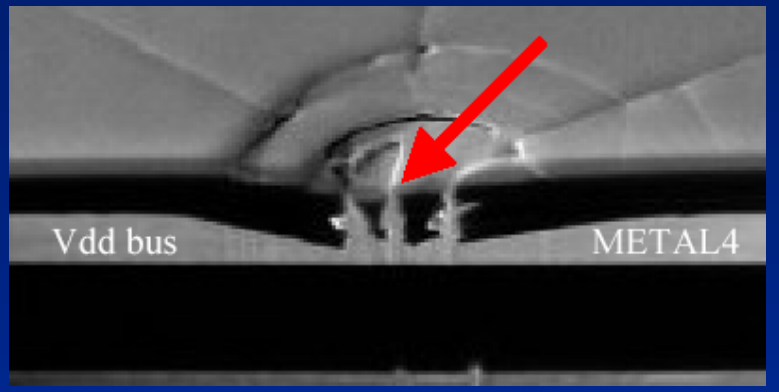
After -500 V FICBM Test

Ref.: A. Olney, B. Gifford, J. Guravage, and A. Righter, "Real-world charged board model (CBM) failures," in *Proc. EOS/ESD Symp.*, 2003, pp. 34-43. (Analog Devices)

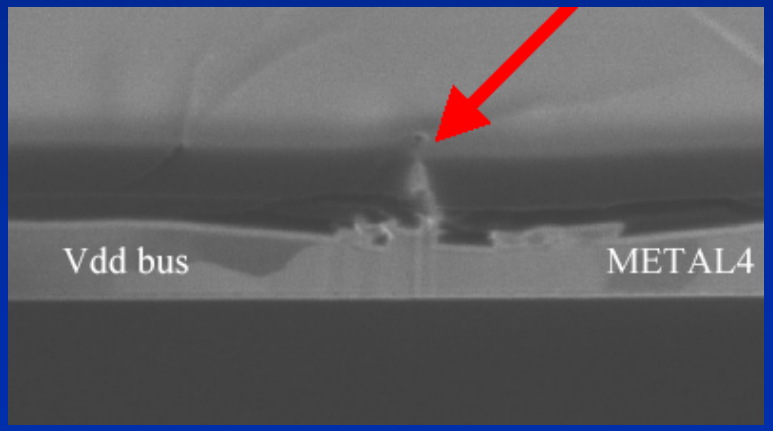
Board-Level CDM ESD Failures (2)



Field-Induced CBM Test Setup (DSP IC)



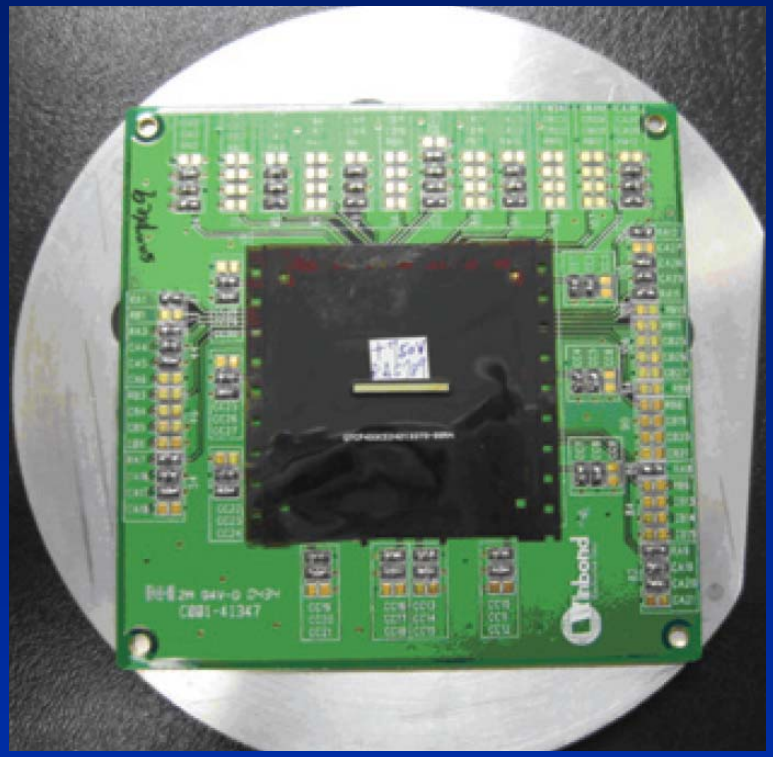
Customer's Return



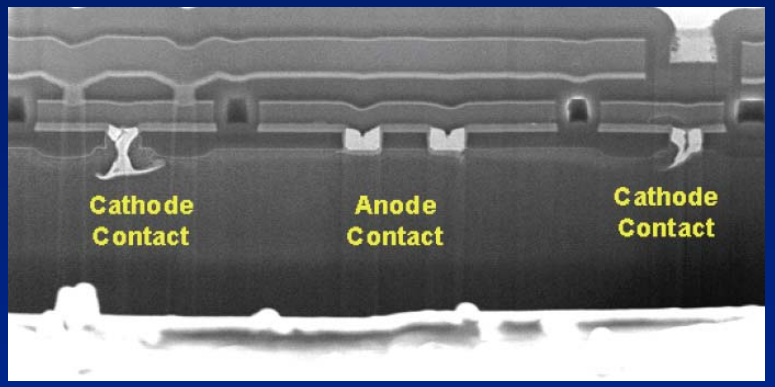
After -250 V FICBM Test

Ref.: A. Olney, B. Gifford, J. Guravage, and A. Righter, "Real-world charged board model (CBM) failures," in *Proc. EOS/ESD Symp.*, 2003, pp. 34-43. (Analog Devices)

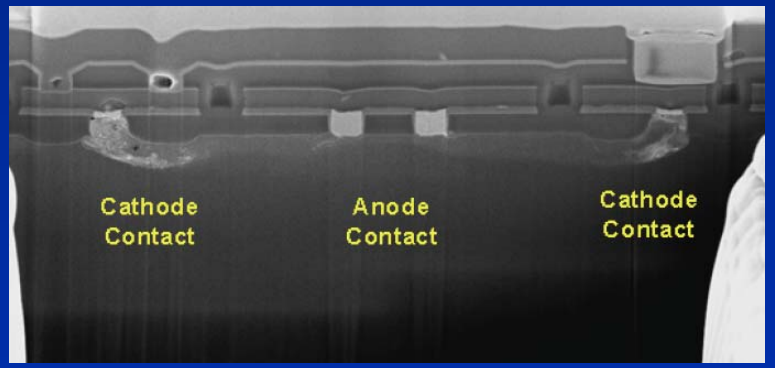
Board-Level CDM ESD Failures (3)



Field-Induced CBM Test Setup
(LCD Driver IC)



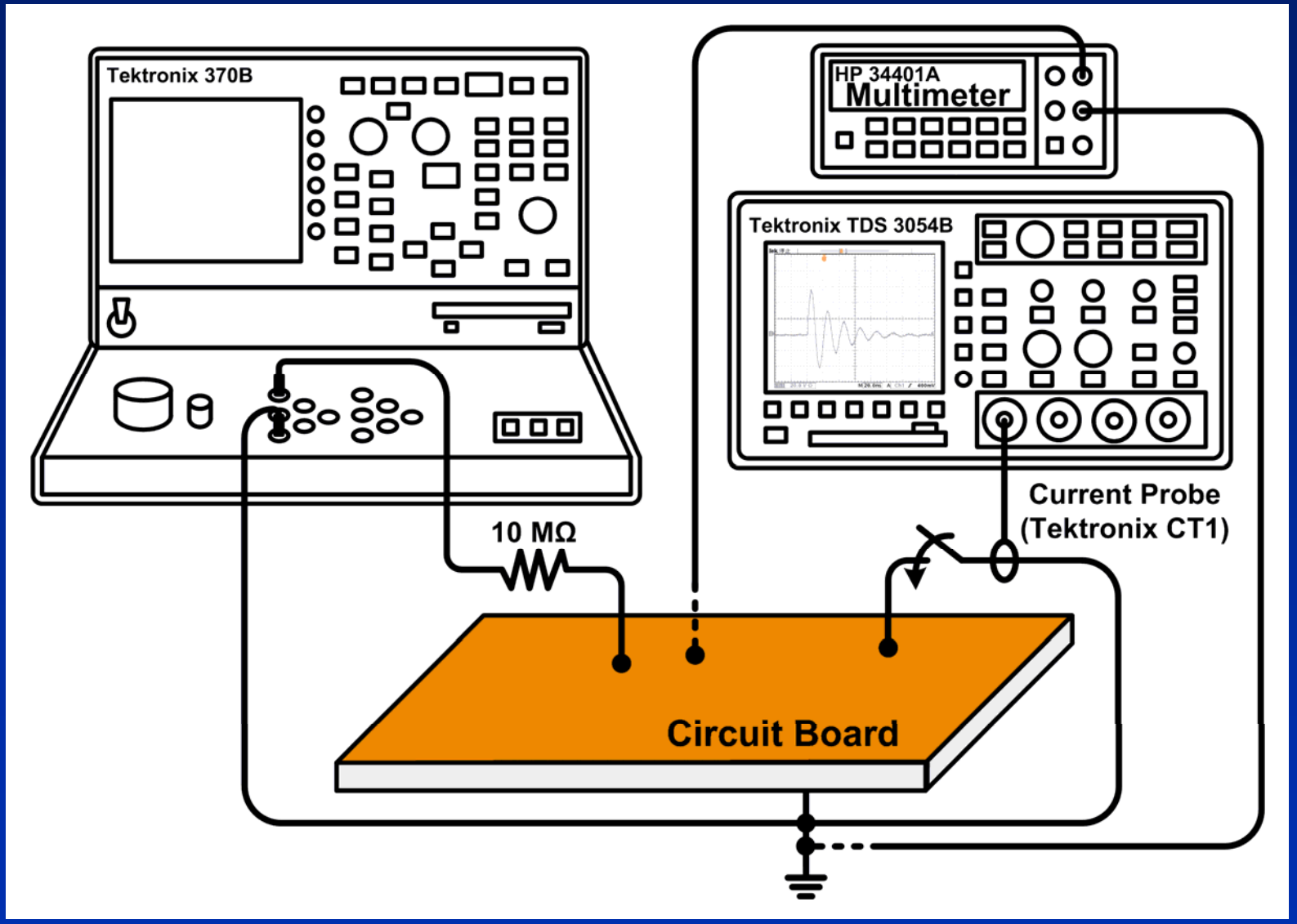
Customer's Return



After +1000 V FICBM Test

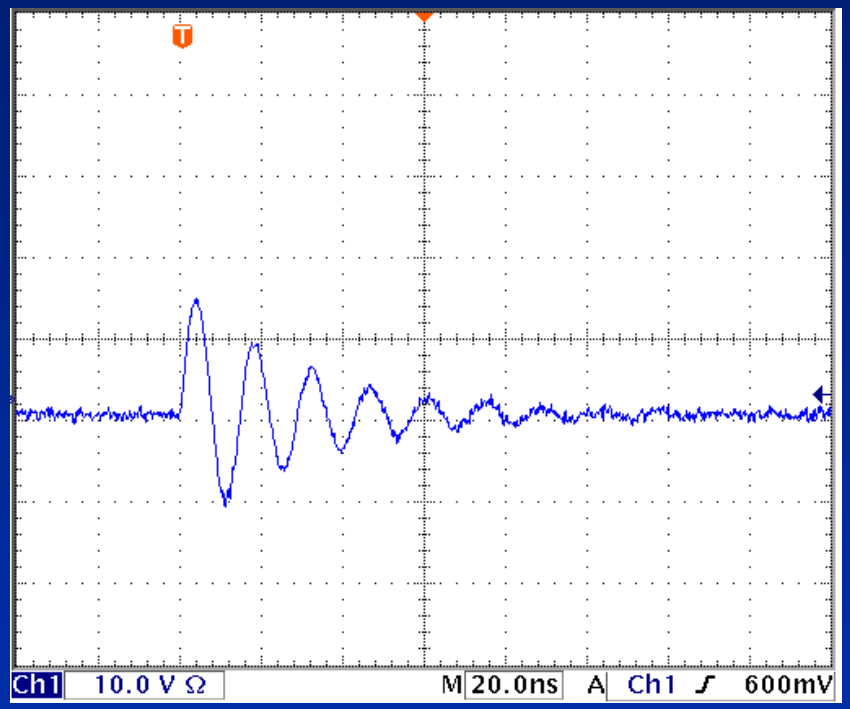
Ref.: C.-T. Hsu, J.-C. Tseng, Y.-L. Chen, F.-Y. Tsai, S.-H. Yu, P.-A. Chen, and M.-D. Ker, "Board level ESD of driver ICs on LCD panels," in *Proc. Int. Reliability Physics Symp.*, 2007, pp. 590-591. (Winbond Electronics)

Board-Level CDM Measurement Setup



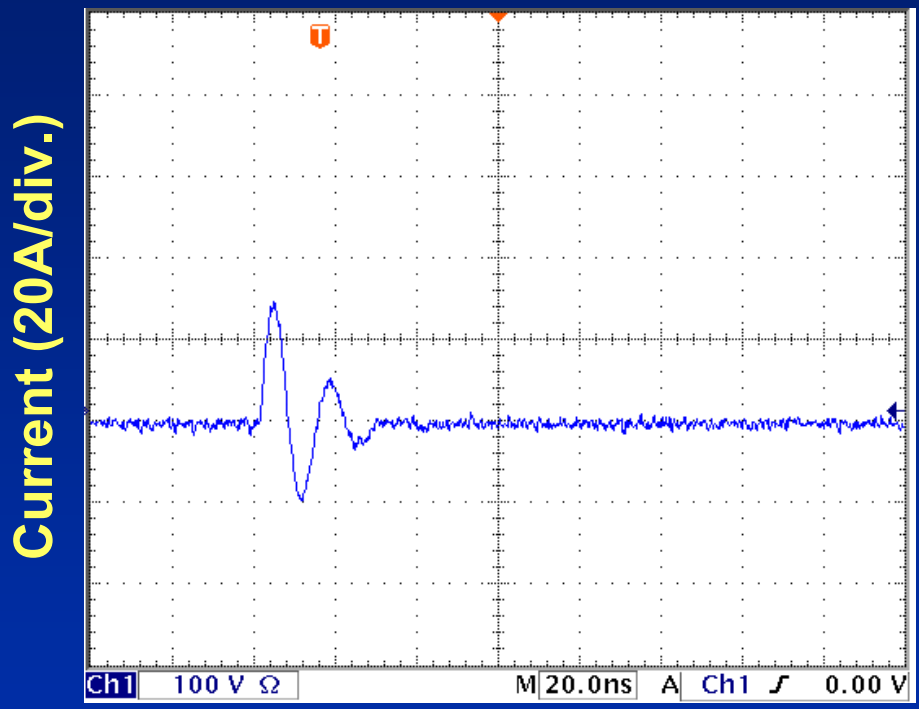
Discharge Current Waveform (1)

Circuit Board Size: 10 cm x 7.5 cm



Charged Voltage = 20 V

Peak Current = 3 A

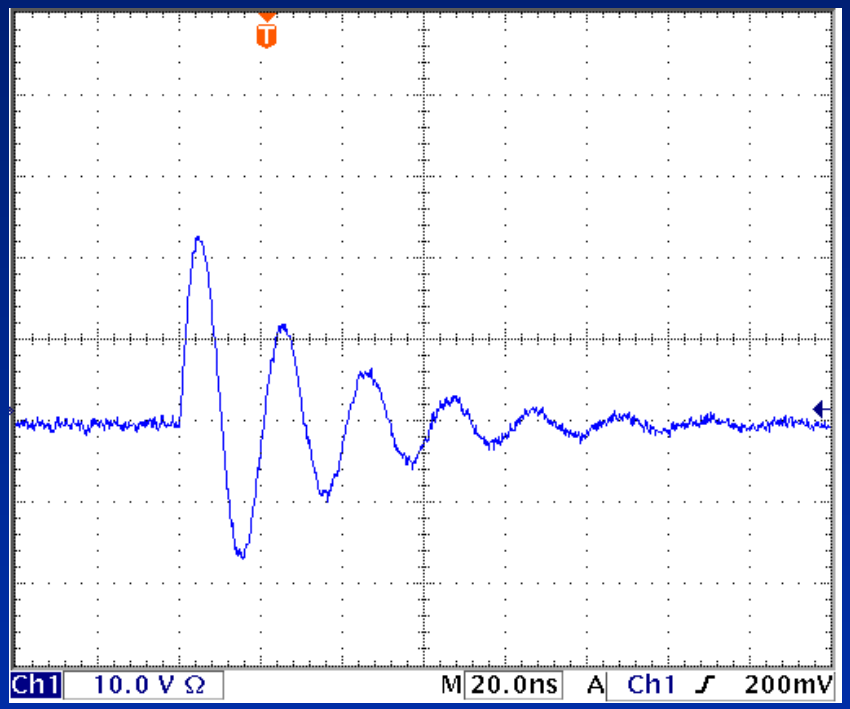


Charged Voltage = 200 V

Peak Current = 28 A

Discharge Current Waveform (2)

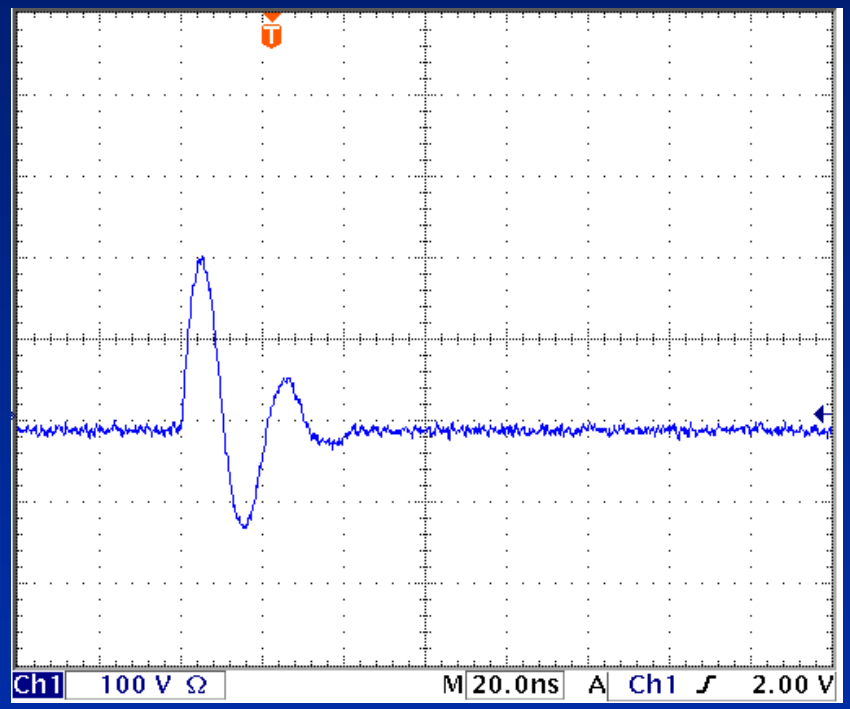
Circuit Board Size: 15 cm x 10 cm



Time (20ns/div.)

Charged Voltage = 20 V

Peak Current = 4.4 A



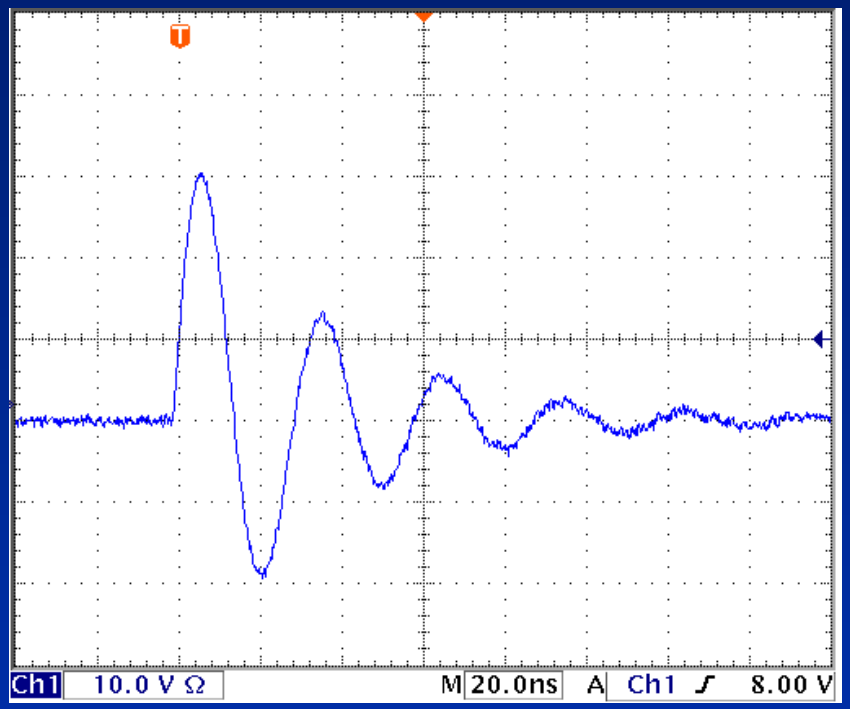
Time (20ns/div.)

Charged Voltage = 200 V

Peak Current = 42 A

Discharge Current Waveform (3)

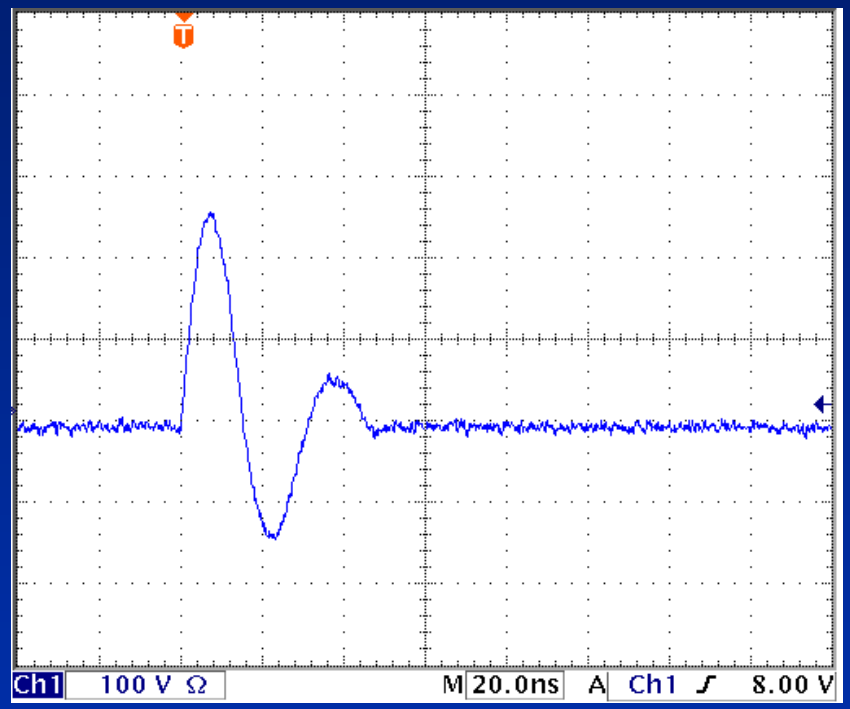
Circuit Board Size: 20 cm x 15 cm



Time (20ns/div.)

Charged Voltage = 20 V

Peak Current = 6 A



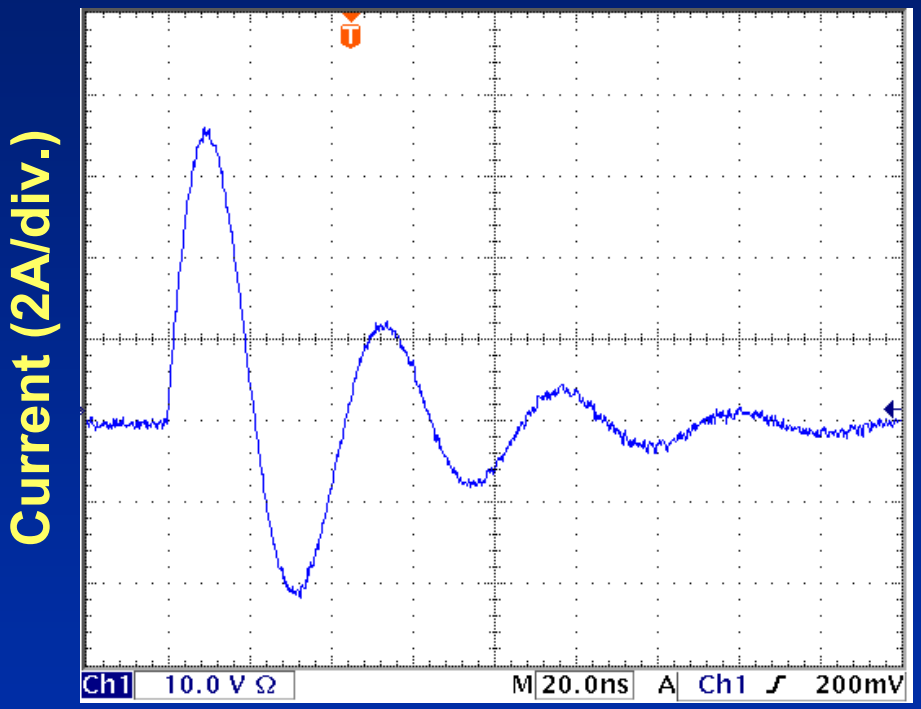
Time (20ns/div.)

Charged Voltage = 200 V

Peak Current = 52 A

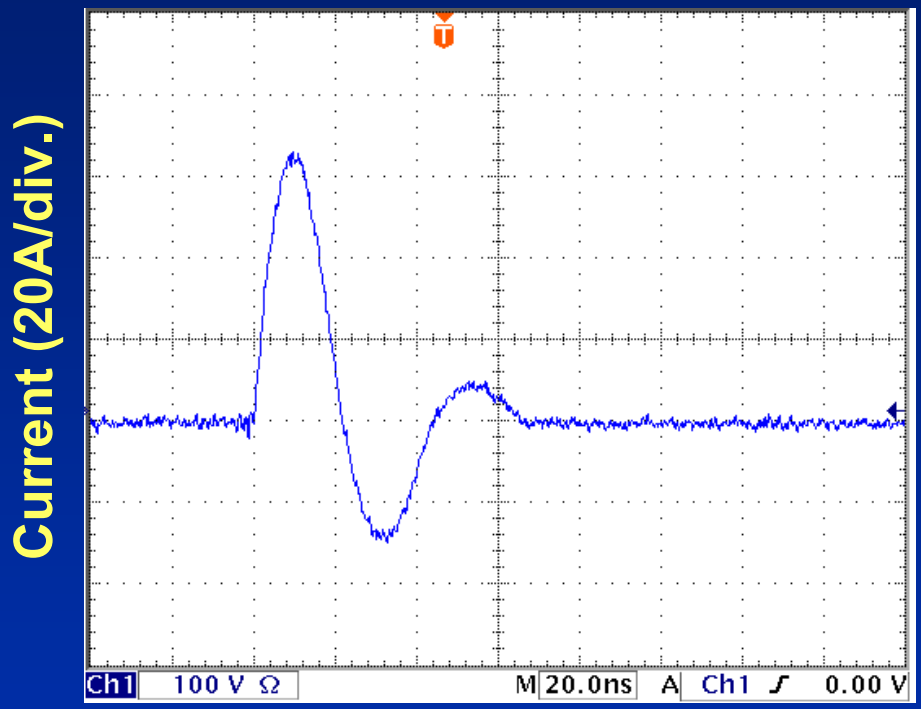
Discharge Current Waveform (4)

Circuit Board Size: 30 cm x 20 cm



Charged Voltage = 20 V

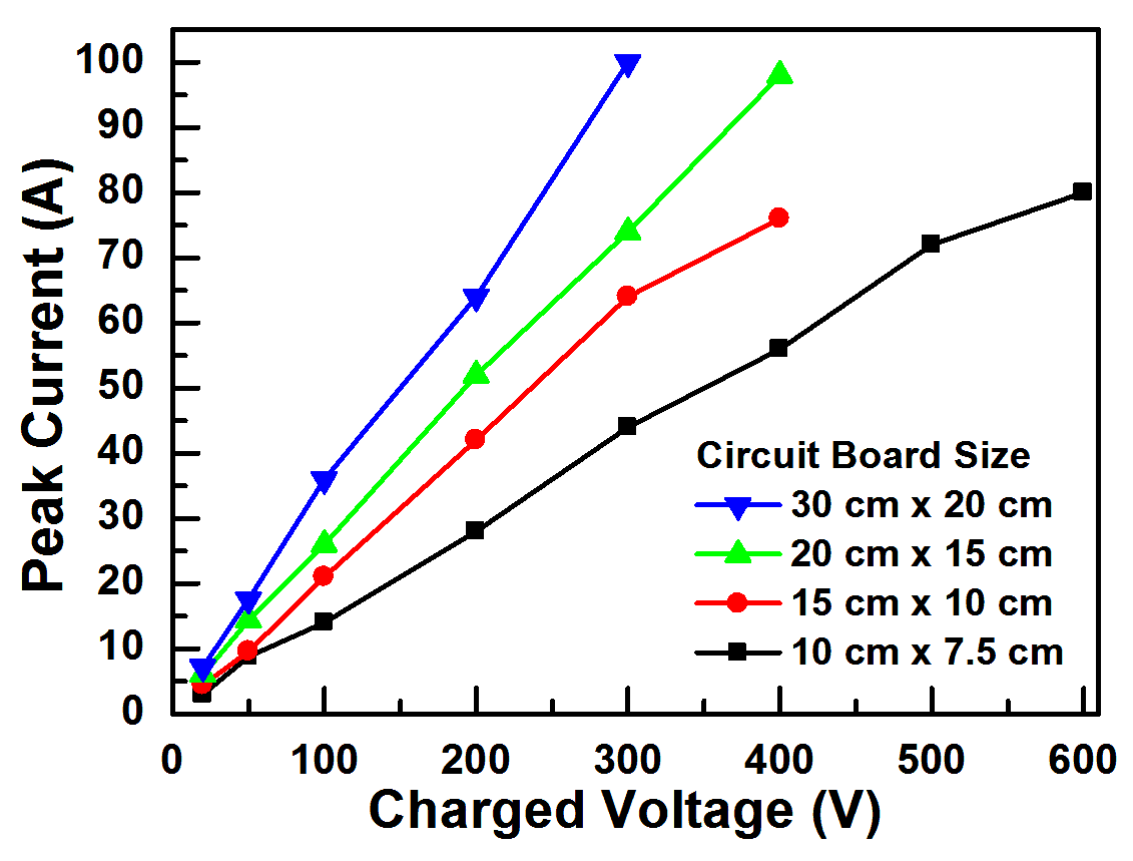
Peak Current = 7.2 A



Charged Voltage = 200 V

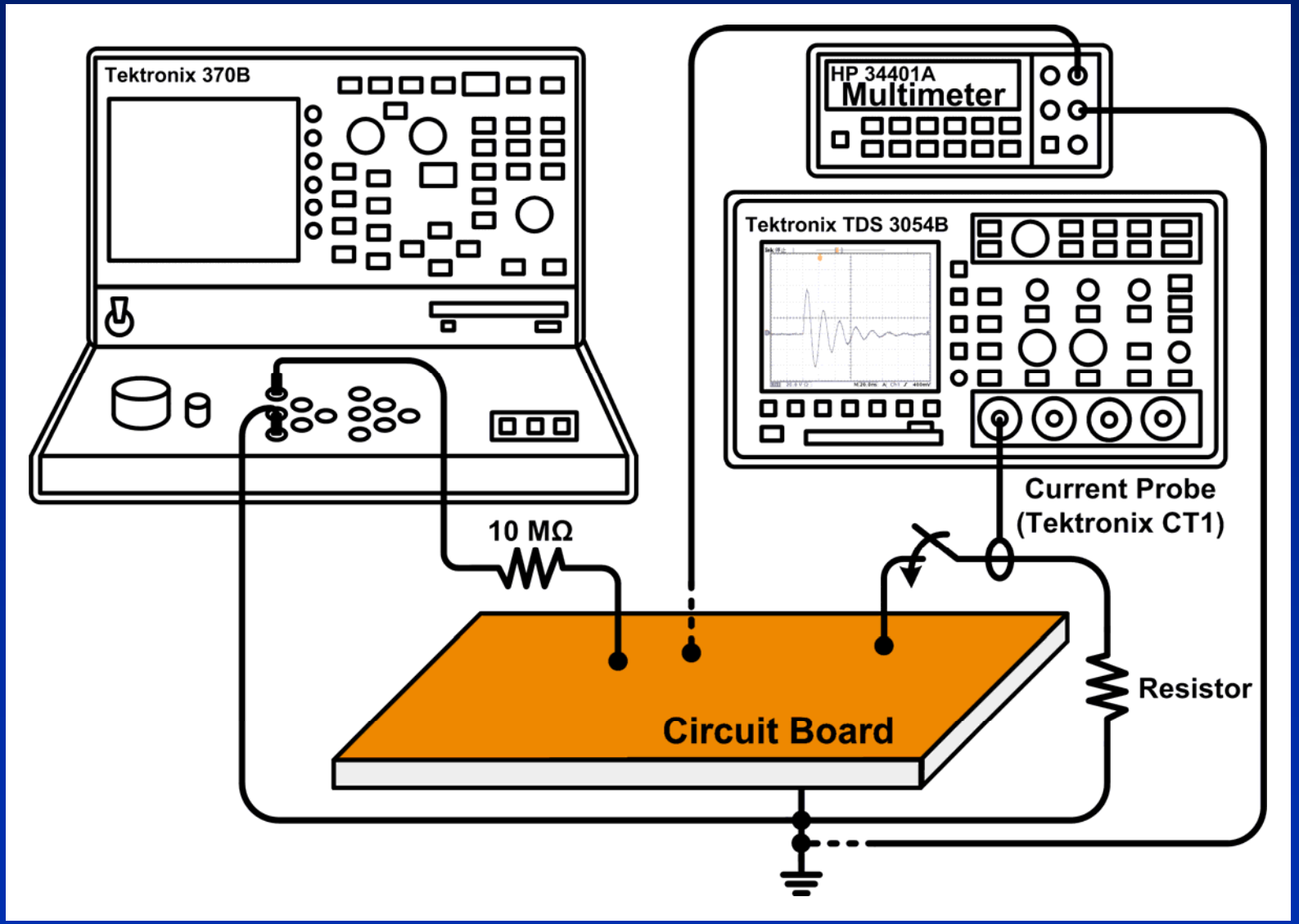
Peak Current = 64 A

Peak Discharge Current Under Different Conditions



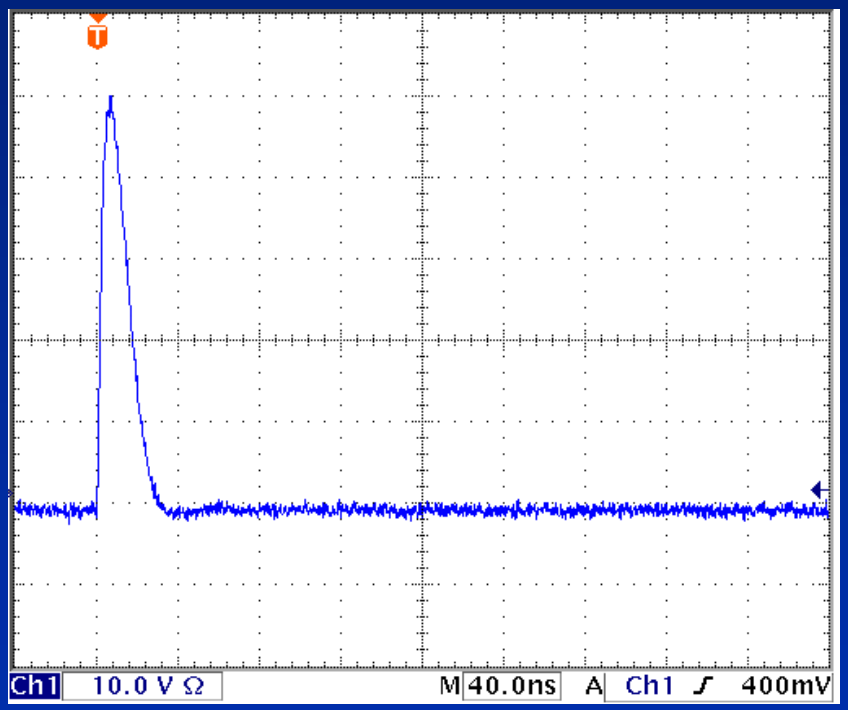
- For the same circuit board size, the peak discharge current is proportional to the charged voltage.

Board-Level CDM With Series Resistor

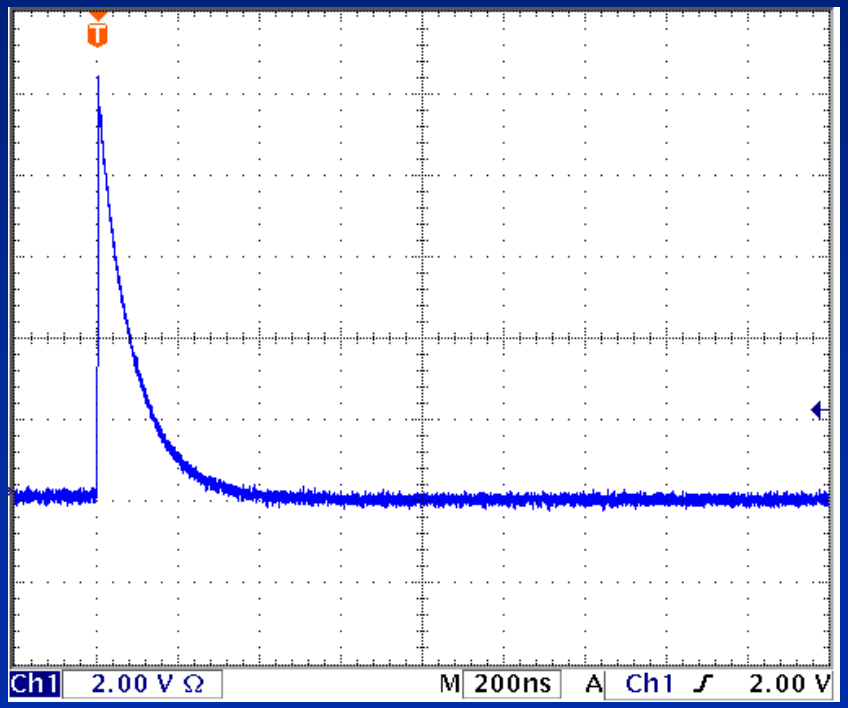


Discharge Current Waveform With Series Resistance (1)

Circuit Board Size: 20 cm x 15 cm
Charged Voltage: 100 V



Time (40ns/div.)
Series Resistance = 10 Ω
Peak Current = 10 A

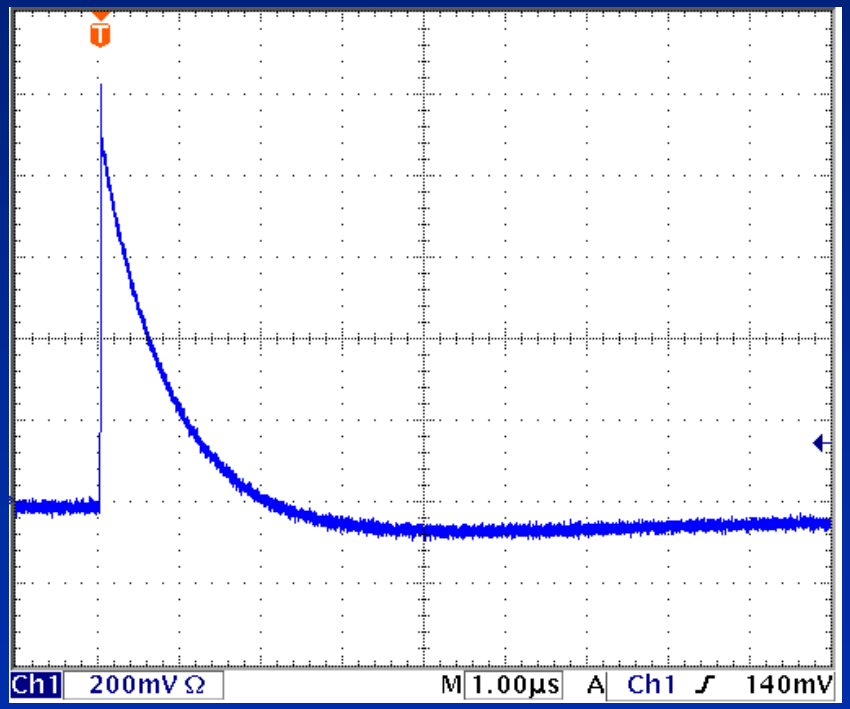


Time (200ns/div.)
Series Resistance = 100 Ω
Peak Current = 2.08 A

Discharge Current Waveform With Series Resistance (2)

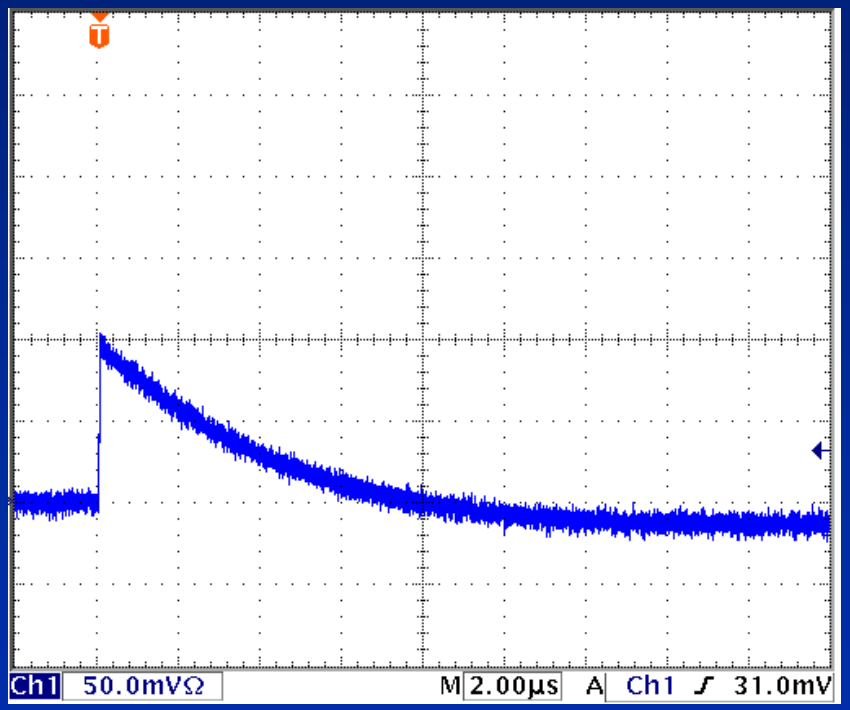
Circuit Board Size: 20 cm x 15 cm
Charged Voltage: 100 V

Current (40mA/div.)



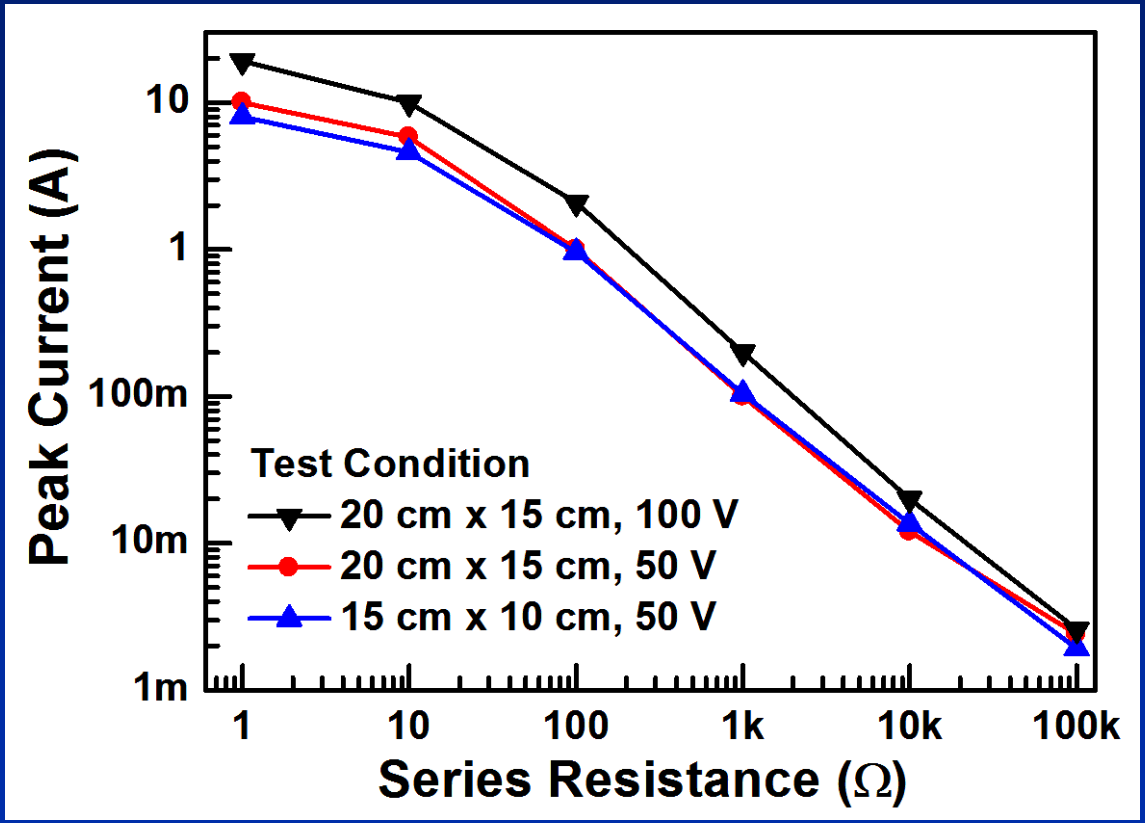
Time (1µs/div.)
Series Resistance = 1 kΩ
Peak Current = 200 mA

Current (10mA/div.)



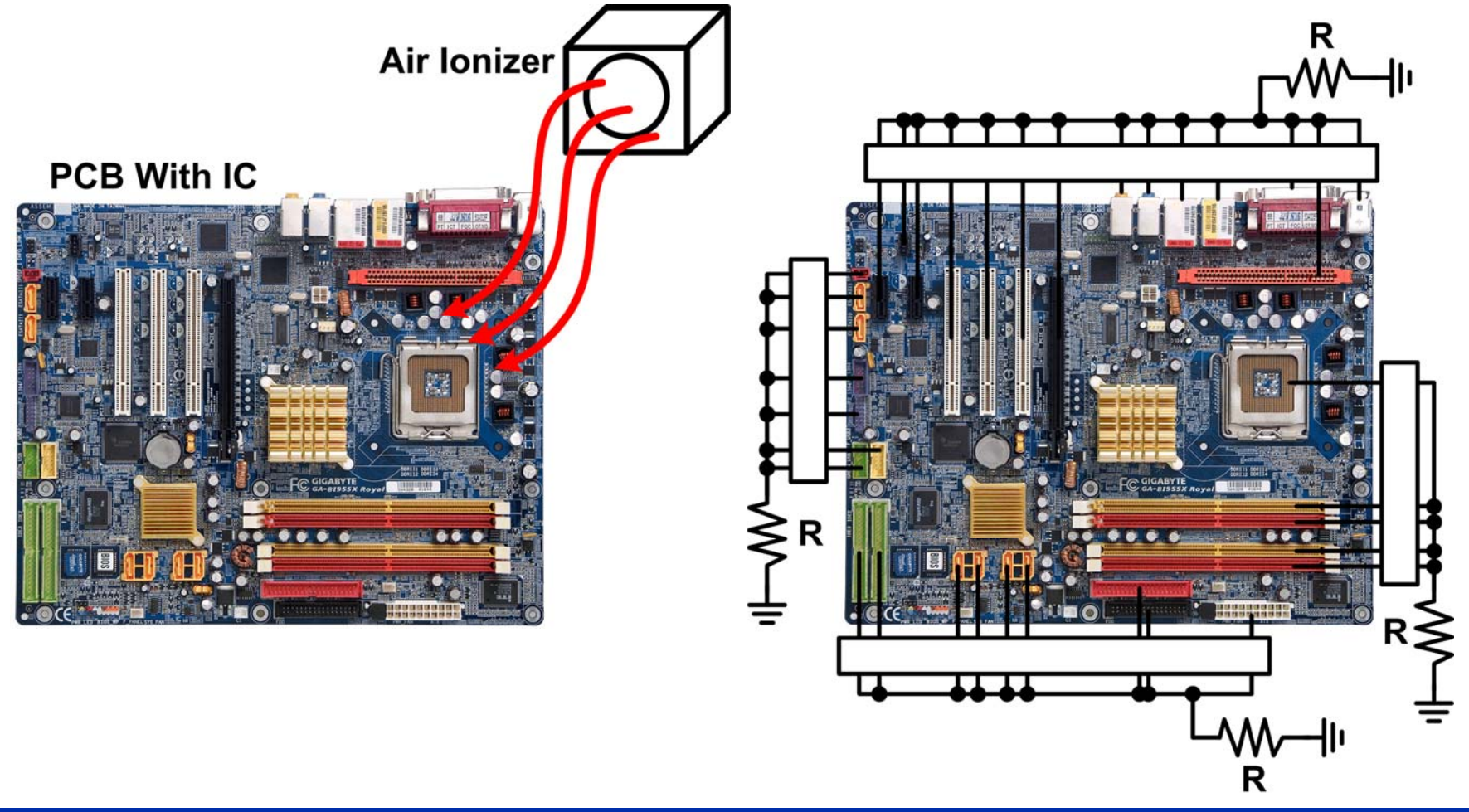
Time (2µs/div.)
Series Resistance = 10 kΩ
Peak Current = 20 mA

Peak Discharge Current Under Different Series Resistances



- The series resistance significantly reduce the peak discharge current.

ESD Protection Against Board-Level CDM



- Using *"ESD Discharger"* to discharge the board through series resistances of kΩ ~ MΩ before it directly grounded.

Conclusions

- Under the same charged voltage, circuit boards with larger dimensions have larger board-level CDM ESD current. Under the same circuit board size, board-level CDM ESD current is proportional to the charged voltage.
- The peak discharge current can be greatly reduced by series resistance.
- Board-level CDM ESD event causes yield loss to IC products. It should be taken into consideration seriously, especially for ICs fabricated in advanced processes.
- A draft standard on board-level CDM ESD test has been proposed in 2007 Taiwan ESD Conference.

References

[1] *Field-induced charged-device model test method for electrostatic discharge withstand thresholds of microelectronic components*, JEDEC Standard JESD22-C101-A, Jun. 2000.

[2] A. Olney, B. Gifford, J. Guravage, and A. Righter, "Real-world charged board model (CBM) failures," in *Proc. EOS/ESD Symp.*, 2003, pp. 34-43.

[3] C.-T. Hsu, J.-C. Tseng, Y.-L. Chen, F.-Y. Tsai, S.-H. Yu, P.-A. Chen, and M.-D. Ker, "Board level ESD of driver ICs on LCD panels," in *Proc. Int. Reliability Physics Symp.*, 2007, pp. 590-591.

[4] T. Reinvuo, T. Tarvainen, and T. Viheriakoski, "Simulation and physics of charged board model for ESD," in *Proc. EOS/ESD Symp.*, 2007, pp. 318-322.

[5] "Draft standard for board-level charged-device model electrostatic discharge test of integrated circuits," presented in *Taiwan ESD Conf.*, 2007.