Optimization on SCR Device With Low Capacitance for On-Chip ESD Protection in UWB RF Circuits

Chun-Yu Lin and Ming-Dou Ker
Nanoelectronics and Gigascale Systems Laboratory, Institute of Electronics, National Chiao-Tung University, Taiwan
Phone: 886-3-5712121#54215 Fax: 886-3-5715412 Email: mdker@ieee.org

Abstract-**Low capacitance (low-C) design on ESD protection device is a solution to mitigate the radio-frequency (RF) performance degradation caused by electrostatic discharge (ESD) protection device. Silicon-controlled rectifier (SCR) device has been used as an effective on-chip ESD protection device in RF ICs due to the smaller layout area and small parasitic capacitance under the same ESD robustness. In this paper, the modified lateral SCR (MLSCR) realized in waffle layout structure is studied to minimize the parasitic capacitance and the variation of the parasitic capacitance within ultra-wide band (UWB) frequencies. With the minimized parasitic capacitance, the degradation on RF circuit performance due to ESD protection devices can be reduced. The waffle MLSCR with low parasitic capacitance is suitable for on-chip ESD protection in UWB RF ICs. Besides, the turn-on speed of MLSCR with waffle layout structure is verified to be better than that with conventional stripe structure.**

I. Introduction

It has been a trend to integrate the whole radio-frequency (RF) circuits into a single chip. With the scaling-down feature size and lower cost, nanoscale CMOS technology is the leading role to integrate RF circuits [1]. However, the thin gate oxide in advanced CMOS processes seriously degrades the electrostatic discharge (ESD) robustness of IC products. Against ESD damages, ESD protection devices must be included in ICs. A general concept of on-chip ESD protection for RF ICs is illustrated in Fig. 1 [2]. The ESD protection devices must be provided for all I/O pads in RF ICs. The parasitic capacitance (C_{ESD}) of ESD protection device is one of the most important design considerations for RF ICs. The parasitic capacitance inevitably contributes capacitive loading to the I/O port, which disturbs the high frequency signals, induces RC delay on the signal path, and causes degradation on RF performance [3]. To mitigate the RF performance degradation caused by ESD protection device, low capacitance (low-C) design on ESD protection device to reduce the parasitic capacitance is a rapid and simple method [4].

With the highest ESD robustness within a smaller layout area and lower parasitic capacitance, the silicon-controlled rectifier (SCR) devices were reported to be useful for RF ESD protection design [5]. The lateral SCR (LSCR) device has been used as the conventional ESD protection device in CMOS technology; however, LSCR has a higher turn-on voltage, which is generally greater than the gate-oxide breakdown voltage of the MOS transistor in input stage. In order to reduce the turn-on voltage of LSCR to provide more effective ESD protection for the internal circuits, the modified lateral SCR (MLSCR) device has been reported [6].

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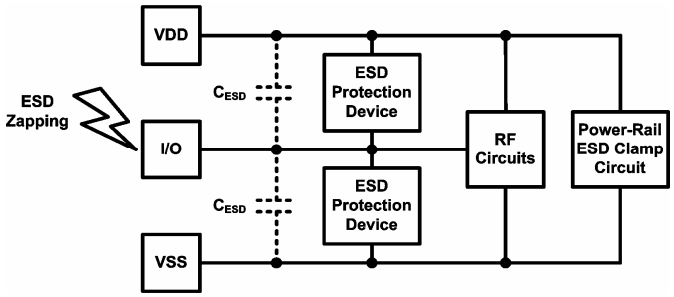

Fig. 1. General concept of on-chip ESD protection for RF ICs.

In this paper, the layout structure of MLSCR device is investigated to minimize the parasitic capacitance. The parasitic capacitance within ultra-wide band (UWB, 3.1~10.6 GHz) frequency band and ESD robustness of MLSCR under different layout structures are presented. The turn-on speed of MLSCR devices under different layout structures are also investigated in this work.

II. MLSCR Devices for RF ESD Protection

Fig. 2 shows the device cross-sectional view of the stripe-structured MLSCR (SMLSCR) and the waffle-structured MLSCR (WMLSCR). Both devices were designed with the same size of 60.62 x 60.62 μm^2. MLSCR devices are basically composed of four regions of P+/N-well/P-well/N+. The anode of MLSCR is electrically connected to P+ and N+ which are formed in the N-well. The cathode is electrically connected to N+ and P+ which are formed in the nearby P-well/P-substrate. The trigger P+ diffusions are added across the N-well/P-well junction in MLSCR device to reduce the junction breakdown voltage and the turn-on voltage. When a positive potential is applied between the anode and the cathode, the N-well/P-well junction is reverse-biased, so MLSCR device is kept off under normal circuit operating conditions. When an ESD stress is zapped to the anode with cathode grounded, MLSCR device will become highly conductive to quickly discharge ESD current due to the turn-on of latchup path. In SMLSCR, it discharges ESD current in only two directions, whereas

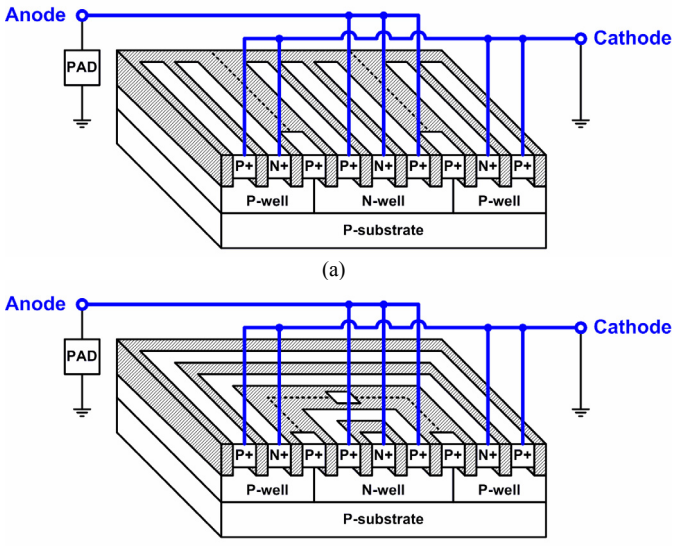

Fig. 2. Device cross-sectional view of (a) stripe-structured MLSCR (SMLSCR) and (b) waffle-structured MLSCR (WMLSCR).

WMLSCR discharges ESD current in four directions. Thus, the ESD robustness can be improved under the same parasitic capacitance by using WMLSCR. In other word, the ratio of the parasitic capacitance to ESD robustness can be minimized by realizing MLSCR device with waffle layout structure.

To investigate the relationship between the trigger P+ diffusion area and the parasitic capacitance, MLSCR devices were implemented with different trigger diffusion areas to evaluate the device characteristics and ESD robustness. The trigger diffusion areas of two SMLSCR devices were 123.2 μm^2 and 242.48 μm^2, and those of two WMLSCR devices were 140.48 μm^2 and 264.96 μm^2, which are listed in Table I. These devices have been fabricated in a 0.18-μm CMOS process for experimental investigations.

III. Measured Device Characteristics

A. Transmission Line Pulsing (TLP) Measurement

The turn-on voltage ($V_{turn\text{-}on}$) and secondary breakdown current (I_{t2}) of the fabricated MLSCR devices are characterized by the TLP system. The TLP-measured I-V curves for all MLSCR are shown in Fig. 3, and the extracted device characteristics are listed in Table I.

B. ESD Robustness

The human-body-model (HBM) ESD levels of the fabricated MLSCR devices are evaluated by the ESD simulator. All MLSCR devices pass the HBM ESD test (V_{HBM}) of 8-kV, which is the measurement limitation of HBM ESD tester. In order to distinguish the ESD robustness of SMLSCR from those of WMLSCR, the machine-model (MM) ESD tests are performed. The MM ESD levels (V_{MM}) of all MLSCR devices are within the range of 1.5~1.7 kV, as listed in Table I. Despite the MM ESD robustness of WMLSCR are slightly worse than those of SMLSCR due to the reduction of N-well area in the waffle layout structure, the parasitic capacitance can be greatly reduced.

Table I
Comparisons on Measured Device Characteristics of MLSCR under Different Layout Structures

Symbol	Trigger Diffusion Area (μm^2)	$V_{turn\text{-}on}$ (V)	I_{t2} (A)	V_{HBM} (kV)	V_{MM} (kV)	ΔC_{ESD} Within 3.1~10.6 GHz (fF)
$SMLSCR_1$	123.2	12.52	> 6	> 8	1.63	53.41
$SMLSCR_2$	242.48	12.54	> 6	> 8	1.68	67.47
$WMLSCR_1$	140.48	11.81	> 6	> 8	1.59	39.36
$WMLSCR_2$	264.96	12.55	> 6	> 8	1.56	49.13

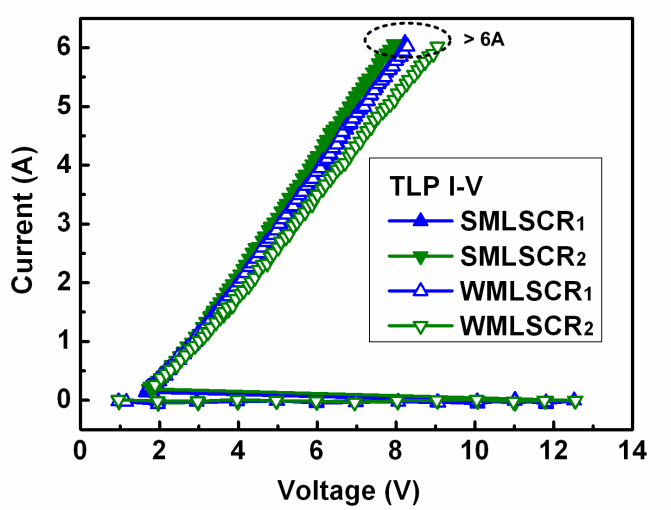

Fig. 3. TLP-measured I-V curves of MLSCR under different layout structures.

C. Parasitic Capacitance

The parasitic capacitance of each MLSCR was obtained from the Y_{11}-parameter, which was transformed from the measured two-port S-parameters. The two-port S-parameters were measured by using the vector network analyzer HP 8510C. To facilitate on-wafer two-port S-parameters measurement, MLSCR devices were implemented with ground-signal-ground (G-S-G) pads. In order to extract the characteristics of the intrinsic device in high frequency, the parasitic effects of the bond pads (PAD in Fig. 2) must be removed. The test patterns, one including the DUT and the other excluding the DUT, as shown in Figs. 4(a) and 4(b), were fabricated in the same experimental test chip. The Y_{11}-parameter can be obtained from the measured two-port S-parameters by using

$$Y_{11} = \frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{Z_0\left((1+S_{11})(1+S_{22})-S_{12}S_{21}\right)}, \quad (1)$$

where Z_0 is the termination resistance and equals to 50 Ω. The measured Y-parameter of the including-DUT pattern is labeled as Y_{11_meas}, and the measured Y-parameter of the

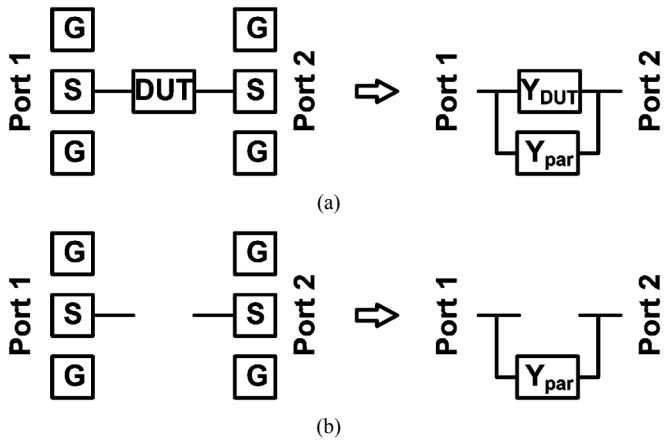

Fig. 4. Layout top view with G-S-G pads and equivalent model of (a) including-DUT pattern and (b) excluding-DUT pattern.

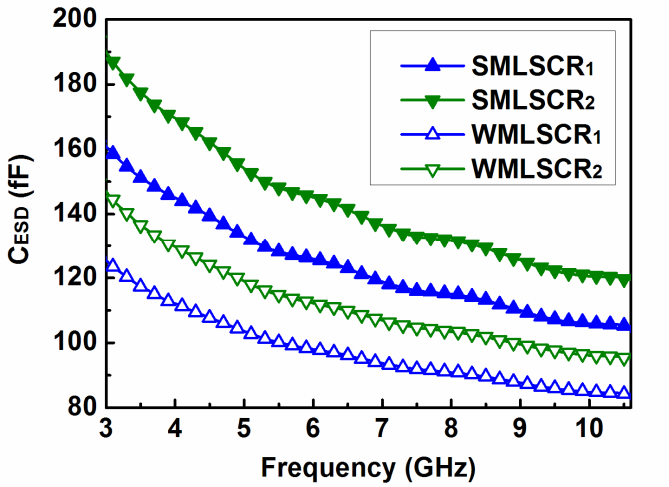

Fig. 5. Extracted parasitic capacitance within 3.1~10.6 GHz of MLSCR devices under different layout structures.

excluding-DUT pattern is labeled as Y_{11_par}. The intrinsic device Y-parameter (Y_{11_DUT}) can be obtained by subtracting Y_{11_par} from Y_{11_meas}. Finally, the intrinsic parasitic capacitance (C_{ESD}) of each MLSCR was extracted from the intrinsic device Y-parameter by using

$$C_{ESD} = \frac{\mathrm{Im}(Y_{11\_DUT})}{2\pi f}, \quad (2)$$

where f is the operating frequency.

Fig. 5 shows the extracted parasitic capacitance within UWB frequencies of all MLSCR devices. During the S-parameters measurement, the anode of each MLSCR was connected to port 1 and biased at 0.9 V, which is VDD/2 in the given 0.18-µm CMOS process, and the cathode was connected to port 2 and biased at 0 V. The parasitic capacitance of SMLSCR and WMLSCR are about 105~190 fF and 85~145 fF, respectively. For each MLSCR, the parasitic capacitance is decreasing as the frequency increasing. Because the parasitic capacitance was in series with a resistor, which is caused by the parasitic N-well resistance and P-well resistance in each MLSCR, the parasitic capacitance in high frequency is decreasing with the increasing

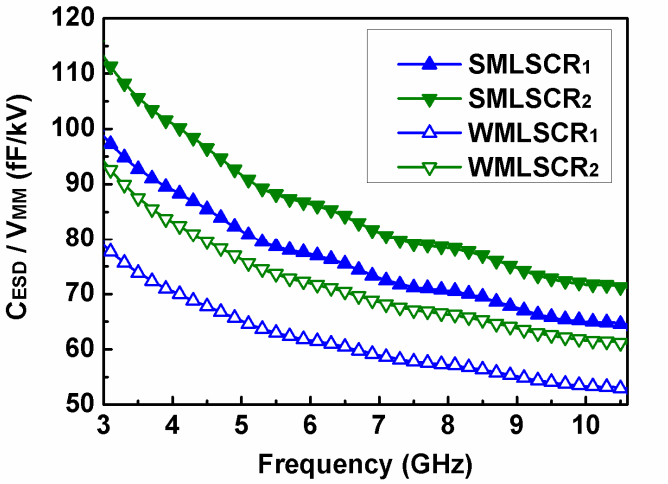

Fig. 6. Ratios of parasitic capacitance to MM ESD robustness within 3.1~10.6 GHz of MLSCR devices under different layout structures.

frequency. The variation of the parasitic capacitance within 3.1~10.6 GHz (ΔC_{ESD}) of SMLSCR and WMLSCR are about 55~65 fF and 40~50 fF, which are summarized in Table I.

D. Comparison on Parasitic Capacitance and ESD Robustness

The ratios of the parasitic capacitance to MM ESD robustness (C_{ESD}/V_{MM}) within UWB frequencies of all MLSCR devices were evaluated and compared in Fig. 6. According to the measured results, the C_{ESD}/V_{MM} ratios of SMLSCR and WMLSCR are about 65~115 fF/kV and 50~95 fF/kV, respectively. The C_{ESD}/V_{MM} ratios are decreased with the decrease of the P+ trigger diffusion area. The C_{ESD}/V_{MM} ratios of WMLSCR have significant decrease of about 30%, as compared with those of SMLSCR. The ratios of ΔC_{ESD} to MM ESD robustness ($\Delta C_{ESD}/V_{MM}$) of SMLSCR and WMLSCR are about 30~40 fF/kV and 20~30 fF/kV, respectively. The $\Delta C_{ESD}/V_{MM}$ ratios of WMLSCR also have significant decrease as compared with those of SMLSCR.

E. Turn-on Speed

To investigate the turn-on speed of MLSCR devices under different layout structures, the experimental setup to measure the required turn-on times of MLSCR devices is illustrated in Fig. 7. The trigger diffusions of MLSCR device were treated as the trigger port, and the trigger pulse was applied to the trigger port to turn on MLSCR device. The pulse with the amplitude of 5 V, rise time of 10 ns, and pulse width of 100 ns was applied to the trigger port. A 5-V voltage bias was connected to the anode of MLSCR through a 10-Ω resistance, which was used to limit the sudden large transient current from power supply when MLSCR device is turned on. The cathode of MLSCR device was grounded. The turn-on time of each MLSCR is defined as the time for MLSCR device to enter its low-voltage holding region and reach 2.5 V. The measured voltage waveforms on the trigger nodes and anodes of MLSCR devices under different layout structures are shown in Fig. 8. The turn-on times of $SMLSCR_1$ and $WMLSCR_1$ are 12.5 ns and 10.9 ns, respectively. The faster turn-on speed is found in WMLSCR.

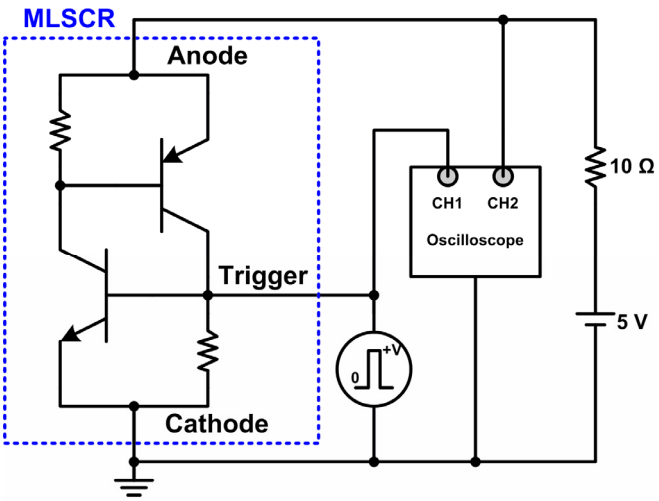

Fig. 7. Measurement setup to find turn-on time of MLSCR.

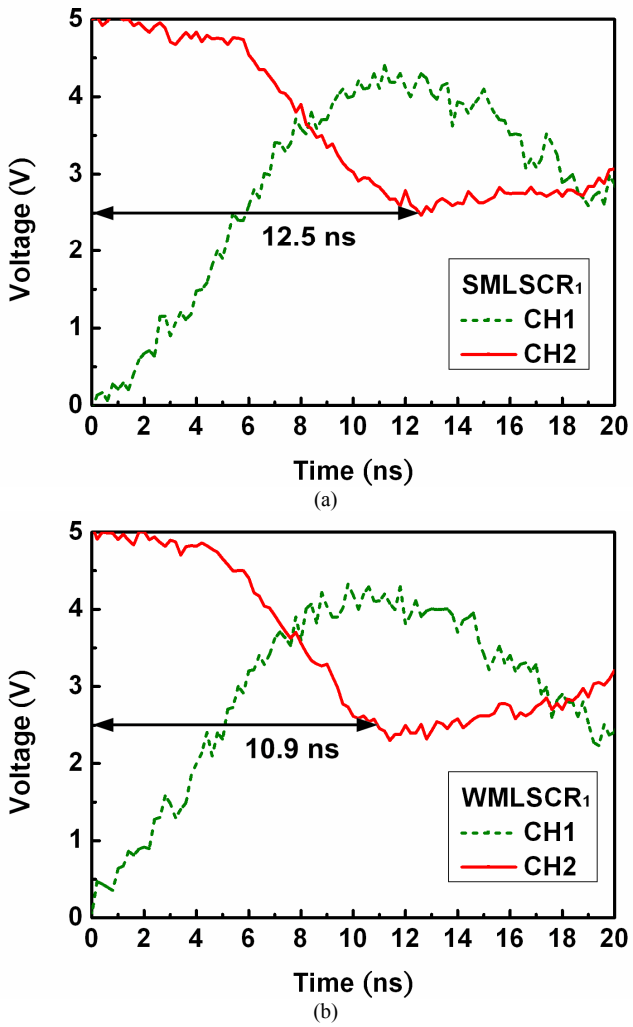

Fig. 8. Measured waveforms for turn-on time of (a) $SMLSCR_1$ and (b) $WMLSCR_1$.

The turn-on speed of MLSCR device was related to the base-emitter resistance (P-well resistance) in the NPN transistor of MLSCR device. MLSCR device with the larger P-well resistance can be turned on by the smaller trigger current, which leads to the smaller turn-on time. Fig. 9 shows the DC I-V curves at the trigger nodes of MLSCR devices with cathode grounded. The larger resistance is found in WMLSCR (R_{WMLSCR_1}), which agrees with the result that the turn-on time is reduced in WMLSCR.

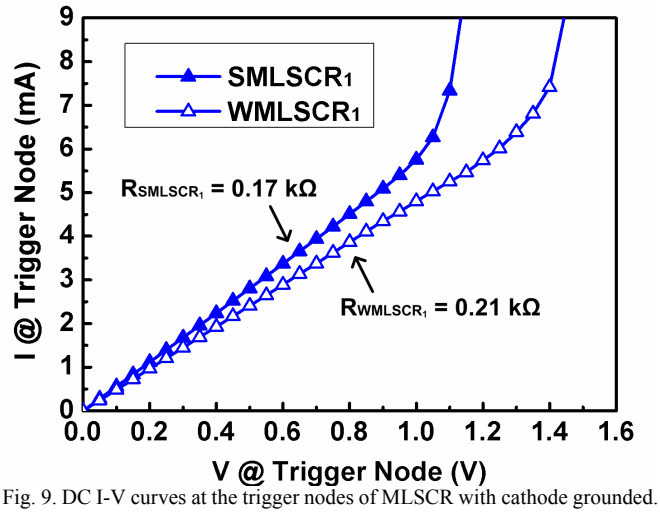

Fig. 9. DC I-V curves at the trigger nodes of MLSCR with cathode grounded.

IV. Conclusion

In this work, SCR devices with the waffle layout structure have been verified to have the reduced parasitic capacitance under the same ESD robustness, and they also have been verified to have the reduced variation of the parasitic capacitance within UWB frequencies. Besides, the faster turn-on speed is found in SCR device with the waffle layout structure. Thus, SCR devices realized in the waffle layout structure are more suitable for RF ESD protection than those realized in the traditional stripe layout structure.

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