Co-Design Strategy With Low-C Consideration for On-Chip ESD Protection in RF ICs

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***Abstract*—Co-design strategy with low-capacitance (low-C) consideration for on-chip ESD protection in RF ICs is a solution to mitigate RF performance degradations caused by ESD protection device. A low-C design on ESD protection device was presented in this paper. An RF power amplifier (PA) co-designed with the low-C ESD protection device was also presented in this paper. Before ESD stress, RF performances of ESD-protected PA were as well as those of the unprotected PA. After ESD stress, the unprotected PA is seriously degraded, whereas the ESD-protected PA still kept the performances well. Co-design strategy with low-C consideration for on-chip ESD protection in RF ICs will continually be the important design task to accomplish RF ESD protection in CMOS technology.**

I. INTRODUCTION

With the scaling-down feature size and lower cost, it has been a trend to integrate the whole RF circuits into a single chip in nanoscale CMOS technology [1]. In the advanced CMOS processes, however, the thinner gate oxide seriously degrades the electrostatic discharge (ESD) robustness of IC products. Against ESD damages, ESD protection devices must be included in ICs. A general concept of on-chip ESD protection for RF ICs is illustrated in Fig. 1 [2]. The ESD protection devices must be provided for all I/O pads in RF ICs. The parasitic capacitance (C_{ESD}) of ESD protection device is one of the most important design considerations for RF ICs [3]. The parasitic capacitance inevitably contributes capacitive loading to I/O port, which disturbs the high frequency signals, induces RC delay on the signal path, and causes other degradations on RF performance. Moreover, the parasitic capacitance degrades the noise figure. For example, the overall noise figure of a low-noise amplifier (LNA) with ESD protection device in Fig. 2 is

$$NF_{total} = NF_{ESD} + \frac{NF_{LNA} - 1}{L^{-1}} = L \cdot NF_{LNA} \quad (1)$$

where L is the power loss of ESD protection device, and NF_{LNA} and NF_{ESD} denote the noise figures of LNA and ESD protection device. The noise figure of ESD protection device is equal to its power loss because ESD protection device is a passive reciprocal network. If ESD protection device provides 1 dB signal loss, the total noise figure will increase 1 dB as well. To mitigate these RF performance degradations caused by ESD protection device, co-design strategy with low-capacitance (low-C) consideration for on-chip ESD protection in RF ICs is a solution [4].

This paper presents a low-C design on ESD protection device. With the comparison between the traditional ESD protection device and the proposed low-C ESD protection device, the improvements from the low-C ESD protection device have been successfully verified in silicon chips [5]. Besides, this paper presents an RF circuit co-designed with the low-C ESD protection device. The effects of ESD protection circuit on RF performances and ESD robustness have been investigated in silicon chip [6].

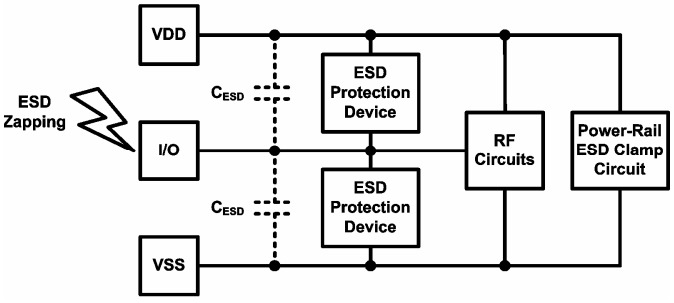

Fig. 1. General concept of on-chip ESD protection in RF ICs.

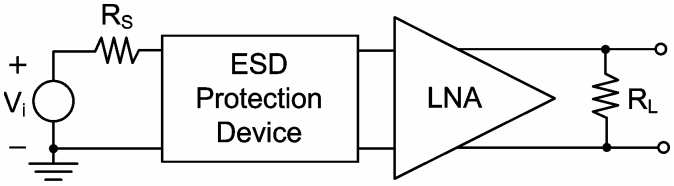

Fig. 2. Low-noise amplifier (LNA) with ESD protection device.

II. ESD PROTECTION WITH LOW-C CONSIDERATION

To mitigate RF performance degradations caused by ESD protection device, low-C design on ESD protection device to reduce the parasitic capacitance is a rapid and straightforward method. A low-C design on the silicon-controlled rectifier (SCR) device is presented in this paper. SCR has been

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Table I
Comparisons on measured device characteristics of SCR under different layout structures

Device	Structure	Layout Area (μm^2)	Trigger P+ Area (μm^2)	$V_{turn-on}$ (V)	V_{HBM} (kV)	V_{MM} (kV)	C_{ESD} @ 2.4GHz (fF)
S-LSCR	Stripe	60.62 x 60.62	0	16.92	> 8	1.80	118.51
S-MLSCR1	Stripe + Trigger	60.62 x 60.62	123.2	12.52	> 8	1.63	178.47
S-MLSCR2	Stripe + Trigger	60.62 x 60.62	242.48	12.54	> 8	1.68	212.81
W-LSCR	Waffle	60.62 x 60.62	0	16.17	> 8	1.53	77.17
W-MLSCR1	Waffle + Trigger	60.62 x 60.62	140.48	11.81	> 8	1.59	139.63
W-MLSCR2	Waffle + Trigger	60.62 x 60.62	264.96	12.55	> 8	1.56	165.25

reported as an useful RF ESD protection element due to its better ESD robustness with smaller parasitic capacitance. SCR device can sustain a much higher ESD level within a smaller layout area, and the smaller layout area introduces less parasitic capacitance; therefore, using SCR device for RF ESD protection can has smaller parasitic capacitance. To further reduce the parasitic capacitance, the different layout structures of SCR devices have been investigated.

A. Lateral SCR (LSCR) With Stripe Layout

Fig. 3(a) shows the traditional stripe-structured LSCR (S-LSCR). The device cross-sectional view of S-LSCR is shown in Fig. 3(e), which is composed of four layers of P+/N-Well/P-Well/N+. Under normal circuit operating condition, S-LSCR is kept off due to the reverse-biased P-Well/N-Well junction. When an ESD stress is zapped to the anode with cathode grounded, S-LSCR will become highly conductive to quickly discharge ESD current due to the turn-on of latchup path. The device characteristics of S-LSCR, such as the layout area, the turn-on voltage ($V_{turn-on}$), the human-body-model (HBM) ESD robustness (V_{HBM}), the machine-model (MM) ESD robustness (V_{MM}), and the parasitic capacitance (C_{ESD}) at 2.4 GHz are all listed in Table I.

B. Modified LSCR (MLSCR) With Stripe Layout

The turn-on voltage of S-LSCR is equal to the breakdown voltage of N-Well/P-Well junction, which is often greater than the breakdown voltage of MOS transistor. To reduce the breakdown voltage of N-Well/P-Well junction, Fig. 3(b) shows the stripe-structured MLSCR (S-MLSCR), which has additional P+ trigger diffusions to reduce the turn-on voltage and improve the turn-on efficiency. The trigger P+ diffusions are added across N-Well/P-Well junctions in S-MLSCR, as shown in Fig. 3(f). Since the lager trigger diffusion may increase the parasitic capacitance, the S-MLSCR was implemented with different trigger diffusion areas to evaluate ESD performance and the device parasitic effects. According to the data listed in Table I, although the parasitic capacitance is increased with the increase of the trigger diffusion area, the trigger voltage can be significantly reduced to effectively protect RF circuits.

C. LSCR With Waffle Layout

In S-LSCR, ESD currents primarily flow through two edges of N-Well, while other two edges do not discharge ESD current, but contribute some parasitic capacitance. The waffle-structured LSCR (W-LSCR) can discharge ESD currents through four edges, which will have the better ESD robustness under the same parasitic capacitance. In other words, the parasitic capacitance of W-LSCR can be reduced under the same ESD robustness. The layout top view of W-LSCR is shown in Fig. 3(c), and the device cross-sectional view of W-LSCR is same as that of S-LSCR. The parasitic capacitance under ESD robustness (C_{ESD}/V_{MM}) of W-LSCR has a decrease of about 25%, as compared with that of S-LSCR.

D. MLSCR With Waffle Layout

With the trigger diffusions added across N-Well/P-Well junctions, the waffle-structured MLSCR (W-MLSCR) is shown in Fig. 3(d). W-MLSCR has the same device cross-sectional view as S-MLSCR, and W-MLSCR also has the better ratios of C_{ESD}/V_{MM} than S-MLSCR. Thus, the waffle layout structure has been demonstrated to reduce the parasitic capacitance under the same ESD robustness. The low-C design on ESD protection device by the waffle layout structure has been proved to be feasible.

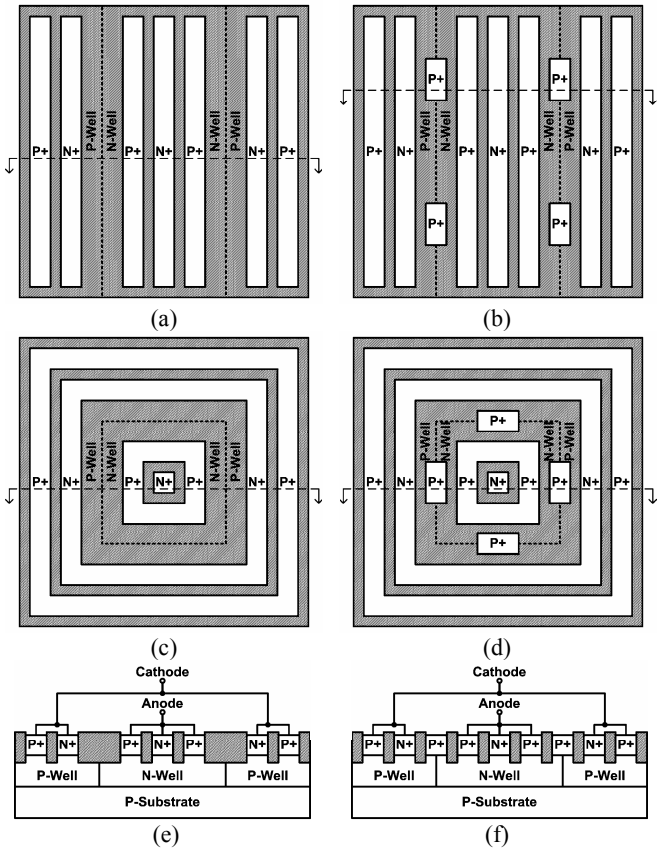


Fig. 3. Layout top view of (a) S-LSCR, (b) S-MLSCR, (c) W-LSCR, and (d) W-MLSCR, and device cross-sectional view of (e) LSCR and (f) MLSCR.

III. ESD Protection With Co-Design Strategy

As the operation frequency of RF circuits increases, the degradations on RF performances due to ESD protection devices become more significant. Therefore, RF front-end circuit and ESD protection circuit must be co-designed to simultaneously optimize RF performances and ESD robustness. The parasitic capacitances of ESD protection devices must be taken into consideration during the design phase of RF circuits.

A. Proposed ESD Protection Technique for RF Circuits

A new ESD protection technique has been proposed to co-design with RF circuits, as shown in Fig. 4. Compared this with Fig. 1, ESD protection devices are composed of a diode from I/O to VDD and a substrate-triggered SCR (STSCR) from I/O to VSS. The trigger current can be injected to enhance the turn-on efficiency to further reduce the turn-on voltage of STSCR [7]. The trigger circuit of STSCR between VDD and VSS is separated from I/O port and does not add any extra loading effects at I/O port. Fig. 4 also shows the discharging path under the positive-to-VSS mode (PS-mode) ESD stress, which is the worse case of ESD events. During PS-mode ESD stress, ESD current will first pass through the diode to VDD, and the trigger circuit will trigger STSCR. Finally, the major ESD current will be discharged by STSCR from I/O pad to VSS. Under other ESD stress modes, including positive-to-VDD (PD-mode), negative-to-VSS (NS-mode), and negative-to-VDD (ND-mode), the proposed ESD protection circuit also provides the corresponding current discharging paths with good ESD robustness.

B. RF Circuit Co-Designed With ESD Protection Circuit

An RF power amplifier (PA) co-designed with the proposed ESD protection circuit has been studied. Fig. 5(a) shows the circuit of this ESD-protected PA. It contains a waffle-structured diode string from output (O/P) to VDD, and a waffle-structured STSCR from O/P to VSS with a RC-inverter as a trigger circuit. The diode string can avoid the signals leak from O/P to VDD since the voltage swing may approach 2 x VDD at the output node. Besides, another set of RC-inverter-STSCR acts as the power-rail ESD clamp circuit to provide the discharging path between VDD and VSS. RC time constants of the trigger circuits were designed in the order of 10^{-6}~10^{-7} s to detect ESD events. Under normal circuit operation, ESD protection circuits were all kept off. During PS-mode ESD stress, with ESD pulses zapping to O/P of ESD-protected PA, ESD current will first flow through the diodes to VDD, and then flow into the RC-inverter to trigger STSCR. ESD current will be discharged by STSCR from O/P to VSS. ESD protection ability of RF circuits can be significantly improved by the co-designed strategy. Besides, the degradations on RF performance due to ESD protection devices can be vanished by the impedance matching during the design phase of RF circuits.

Fig. 5(b) shows the equivalent circuit of the unprotected PA. The operation frequencies of this PA cover the ultra-wide band (UWB, 3.1~10.6 GHz) frequencies. Such unprotected PA is founded to have an worse ESD robustness. Figs. 6(a) and 6(b) show the S_{21}-parameters from 2 to 12 GHz of the unprotected PA and ESD-protected PA, respectively. The S_{21}-parameter is the forward gain of PA. The S_{21}-parameter of the unprotected PA was seriously degraded after HBM ESD zapping. On the contrast, the S_{21}-parameter of ESD-protected PA was still excellent matching even if the 8-kV HBM ESD stress was performed (8-kV is the maximum limitation of ESD simulator). The bandwidths of PAs after each HBM ESD zapping are summarized in Table II. The averaged large signal power gain of the fabricated PAs in 3.1~10.6 GHz are also listed in Table II. The performances of the unprotected PA are seriously degraded after ESD stresses. With the co-design strategy, ESD-protected PA performs good RF performances with strong ESD robustness.

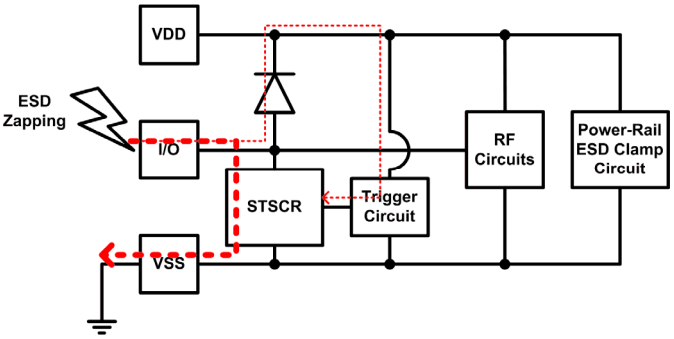


Fig. 4. New ESD protection technique co-designed with RF circuits.

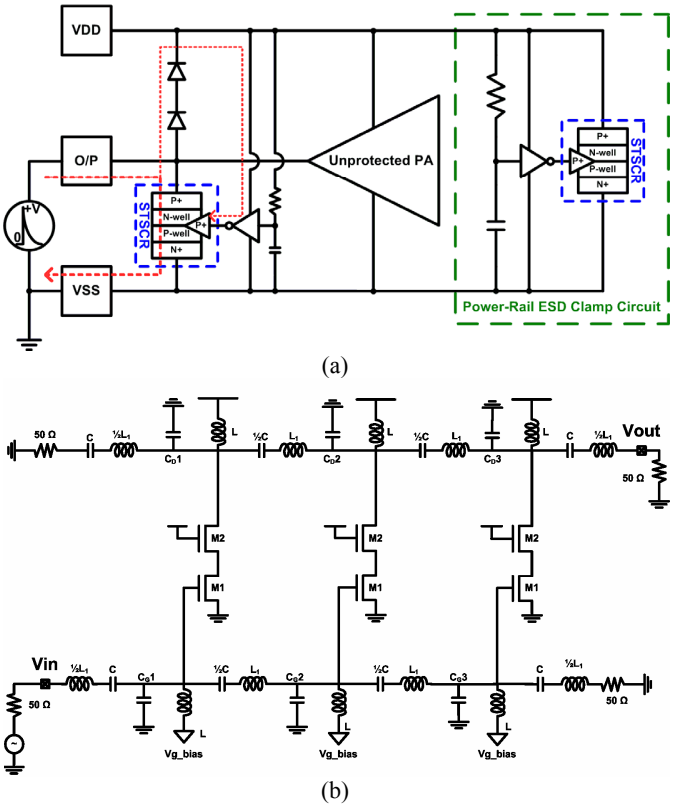
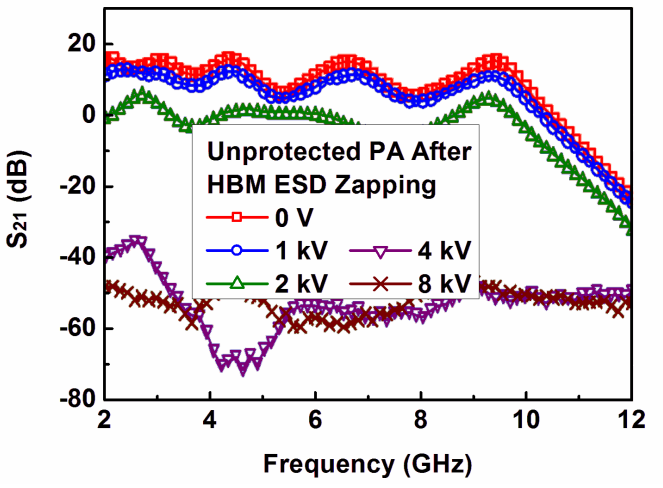


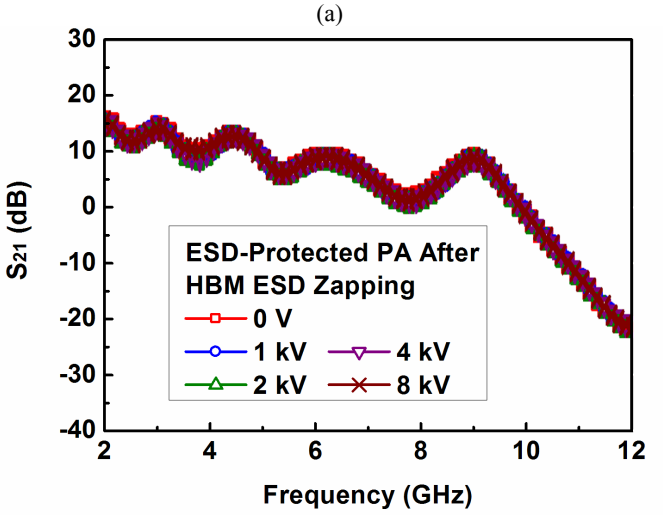
Fig. 5. Equivalent circuits of (a) PA with proposed ESD protection circuit (ESD-protected PA) and (b) unprotected PA.

Table II
Bandwidth and gain of UWB RF PA after HBM ESD zapping

HBM ESD Zapping	Bandwidth		Averaged Gain (3.1~10.6 GHz)	
	Unprotected PA	ESD-Protected PA	Unprotected PA	ESD-Protected PA
0 V	7.8 GHz	7.3 GHz	12.4 dB	9.8 dB
1 kV	7.7 GHz	7.4 GHz	8.9 dB	9.3 dB
2 kV	8.2 GHz	7.3 GHz	-0.4 dB	9.2 dB
4 kV	0 GHz	7.4 GHz	-51.8 dB	8.5 dB
8 kV	0 GHz	7.3 GHz	-55.3 dB	9.5 dB



(a)



(b)

Fig. 6. Measured results on S_{21}-parameters of (a) unprotected PA and (b) ESD-protected PA, after each HBM ESD zapping.

IV. Conclusion

Co-design strategy with low-C consideration to mitigate the degradations on RF performances caused by ESD protection devices is presented in this work. SCR-based devices with the waffle layout structure have been verified to achieve the low-C target. Thus, SCR with the waffle layout structure is more suitable for on-chip ESD protection in RF circuits than that with the stripe layout structure. Besides, PA co-designed with the low-C ESD protection device has been confirmed to have the less negative impacts on RF circuit performance and the well ESD protection capability. Using co-design strategy with low-C consideration, it will continually be the important design task to accomplish on-chip ESD protection in RF ICs.

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