

# HIGH-ROBUST ESD PROTECTION STRUCTURE WITH EMBEDDED SCR IN HIGH-VOLTAGE CMOS PROCESS

Tai-Hsiang Lai<sup>1,2</sup>, Ming-Dou Ker<sup>2</sup>, Wei-Jen Chang<sup>2</sup>, Tien-Hao Tang<sup>1</sup>, and Kuan-Cheng Su<sup>1</sup>

<sup>1</sup> ESD Engineering Department, Reliability Technology & Assurance Division  
United Microelectronics Corp., Science-Based Industrial Park, Taiwan

<sup>2</sup> Nanoelectronics and Gigascale Systems Laboratory  
Institute of Electronics, National Chiao-Tung University, Taiwan

## ABSTRACT

The dependence of device structures and layout parameters on ESD robustness of HV MOSFETs in high-voltage 40-V CMOS process has been investigated by device simulation and verified in silicon test chips. It was demonstrated that a new ESD protection structure with p-type SCR embedded into the HV PMOS has the highest ESD robustness in a given 40-V CMOS process.

## INTRODUCTION

In modern smart power technology, high-voltage (HV) transistors have been extensively used in power management, display driver circuits, and automotive electronics. One critical challenge on reliability issue in HV CMOS process is the ESD robustness of HV MOSFETs [1]-[3]. To improve ESD robustness, the gate-coupling circuit technique has been reported to enhance the ESD performance of HV NMOS [1]. However, it must employ the HV NMOS with a large device dimension and the gate of HV NMOS must be in series with a large resistor, which often occupy a huge silicon area.

In this work, the ESD robustness of MOSFETs in a 0.35- $\mu\text{m}$  40-V process is investigated under different device structures. In addition, a SCR structure embedded into the HV PMOS has been proposed to successfully improve ESD robustness of HV MOSFETs.

## HV ESD DEVICE STRUCTURES

The device cross-sectional views and equivalent circuits of HV NMOS and HV PMOS are shown in Figs. 1(a) and 1(b), respectively. By revising the HV NMOS in Fig. 1(a), the central drain region was replaced by the P<sup>+</sup> diffusion to form the SCR path from drain to source (P<sup>+</sup>/N-Grade/HVPW/N<sup>+</sup>), named HV N-type SCR (NSCR) in Fig. 2(a) [4]-[6]. By revising the HV PMOS in Fig. 1(b), the central drain region was replaced by the N<sup>+</sup> diffusion to develop the SCR path from source to drain (P<sup>+</sup>/HVPW/P-Grade/N<sup>+</sup>), named HV P-type SCR (PSCR) in Fig. 2(b).

## DEVICE SIMULATION

The simulated 2-D current flow-lines of HV NMOS and HV PMOS are illustrated in Figs. 3(a) and 3(b), respectively. For the HV NMOS (HV PMOS), the most currents are not uniformly distributed in the N-Grade (P-Grade) junction, which will cause the current crowding effect around the channel surface to induce the gate-oxide damage during ESD stress. However, the current flows of HV NSCR (HV PSCR) are uniformly distributed along the N-Grade (P-Grade) junction because the vertical p-n-p (lateral p-n-p) BJT and the lateral n-p-n (vertical n-p-n) BJT are simultaneously turned on to conduct more currents into deeper HVPW (HVNW) region, as the flow-lines shown in Figs. 4(a) and 4(b), respectively.

## EXPERIMENTAL RESULTS AND DISCUSSION

Figs. 5(a) and 5(b) show the TLP-measured I-V characteristics of fabricated HV NMOS, HV NSCR, HV PMOS, and HV PSCR, respectively. In Fig. 5(a), the strong snapback characteristics of HV NMOS and HV NSCR are found. The trigger voltage of HV NSCR

is the same as HV NMOS, which is determined by the drain avalanche breakdown voltage of N-Grade/HVPW junction. However, the  $I_{t2}$  of HV NSCR is better than that of HV NMOS under 300- $\mu\text{m}$  device width because the ESD current in the HV NSCR can flow more deeply into the HVPW region when the SCR path is turned on. As shown in Fig. 5(b), no snapback characteristic of the HV PMOS is found. Owing to the inefficient parasitic p-n-p bipolar gain, the  $I_{t2}$  of HV PMOS with 300- $\mu\text{m}$  device width is only 0.07A. The  $I_{t2}$  of HV PSCR can be over 10A, which is much higher than that of all the other HV devices with the same device dimensions.

The HBM and MM ESD levels of HV NMOS, HV NSCR, HV PMOS, and HV PSCR with different device widths are measured and compared in Figs. 6(a) and 6(b), respectively. In Fig. 6(a), the HV PSCR has the highest HBM ESD level (>8kV) among these HV devices, when the device width is only 100 $\mu\text{m}$ . In Fig. 6(b), the MM ESD levels of these HV devices are greater than 200V except for the HV PMOS. Moreover, the HV PSCR under the same device width still has the greatest MM ESD robustness. As shown in Fig. 7, the contact spiking was found in only one finger of multi-finger HV NSCR with 300- $\mu\text{m}$  device width after 2-KV HBM ESD stress. It implies that the ESD robustness of HV NSCR is worse than that of HV PSCR because of the non-uniform turn-on issue in the multi-finger HV NSCR structure.

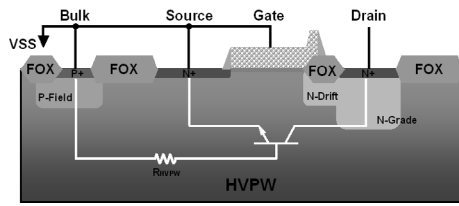
Due to the low holding voltage of HV PSCR, the HV PSCR used in power-rail ESD clamp circuits could be accidentally triggered on by the system-level ESD transient pulses to induce latchup or latchup-like failure in HV CMOS ICs. To overcome the issue, the total holding voltage of HV PSCR should be designed greater than the power supply voltage by adjusting different numbers of stacked HV PSCR [7]. Furthermore, additional trigger circuits should be developed to further enhance ESD protection performance and turn-on speed of the proposed HV PSCR devices in stacked configuration.

## CONCLUSION

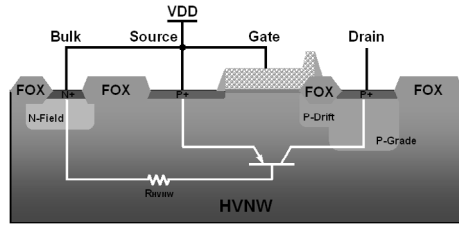
The ESD robustness of ESD protection devices in a 40-V CMOS process has been clearly investigated by TLP, HBM, and MM ESD tests. With very high ESD robustness and uniform current distribution among the fingers in HV PSCR, the ESD robustness of HV PSCR with device width of only 100 $\mu\text{m}$  can sustain ESD stresses of > 8kV for HBM and 700V for MM. The proposed HV PSCR in stacked configuration with trigger circuit can be effectively used for ESD protection in HV CMOS ICs without suffering latchup danger.

## REFERENCES

- [1] C. Duvvury *et al.*, *IEDM*, p. 375, 1997.
- [2] M. P. J. Mergens *et al.*, *IEEE T-ED*, vol. 47, p. 2128, 2000.
- [3] M.-D. Ker *et al.*, *IEEE EDL*, vol. 25, p. 640, 2004.
- [4] S. Pendharkar *et al.*, *ISPSD*, p.341, 2000.
- [5] A. Concannon *et al.*, *ESSDERC*, p. 261, 2004.
- [6] V.A. Vashchenko *et al.*, *IRPS*, p.612, 2005.
- [7] M.-D. Ker *et al.*, *IEEE JSSC*, vol. 40, p. 1751, 2005.

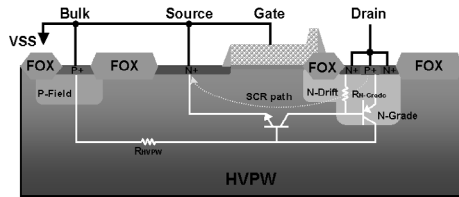


(a)

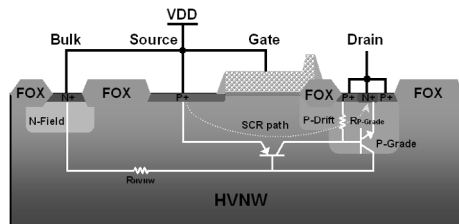


(b)

FIGURE 1. THE CROSS-SECTIONAL VIEWS AND EQUIVALENT CIRCUITS OF (A) HV NMOS AND (B) HV PMOS.

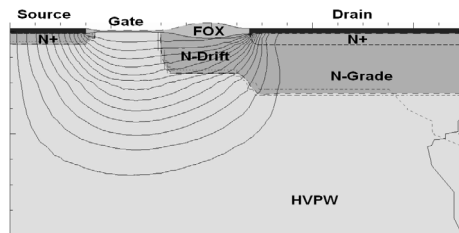


(a)

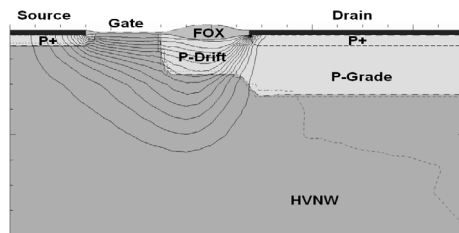


(b)

FIGURE 2. THE CROSS-SECTIONAL VIEWS AND EQUIVALENT CIRCUITS OF (A) HV NSCR AND (B) HV PSCR.

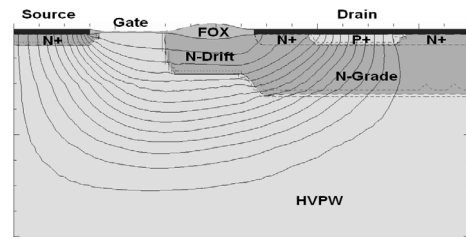


(a)

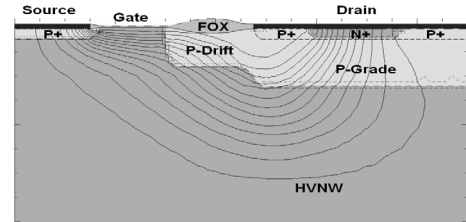


(b)

FIGURE 3. THE SIMULATED 2-D CURRENT DISTRIBUTIONS UNDER TLP STRESS OF (A) HV NMOS AND (B) HV PMOS.

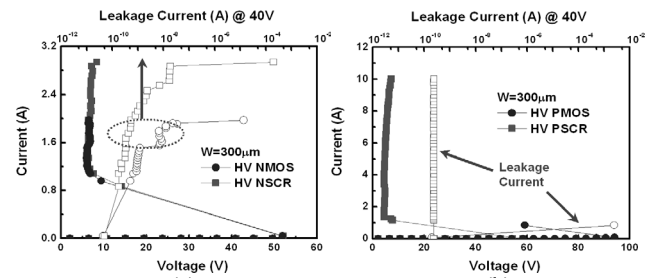


(a)

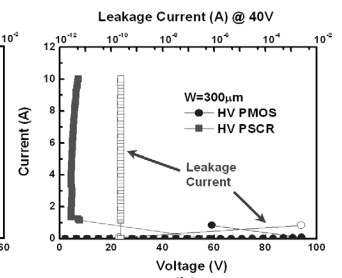


(b)

FIGURE 4. THE SIMULATED 2-D CURRENT DISTRIBUTIONS UNDER TLP STRESS OF (A) HV NSCR AND (B) HV PSCR.

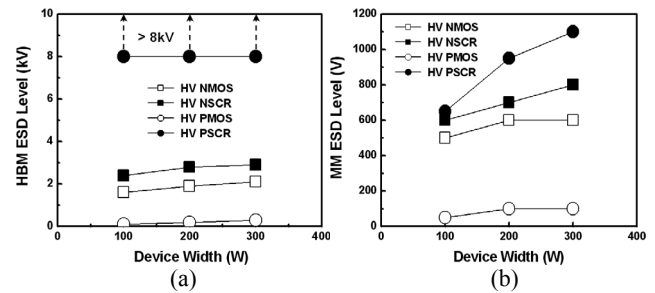


(a)

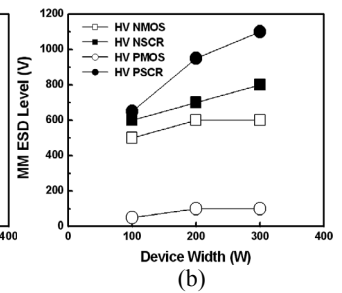


(b)

FIGURE 5. THE TLP MEASURED I-V CHARACTERISTICS OF (A) HV NMOS AND HV NSCR AND (B) HV PMOS AND HV PSCR.



(a)



(b)

FIGURE 6. COMPARISONS OF (A) HBM ESD LEVEL AND (B) MM ESD LEVEL AMONG HV NMOS, HV NSCR, HV PMOS, AND HV PSCR UNDER DIFFERENT DEVICE WIDTHS.

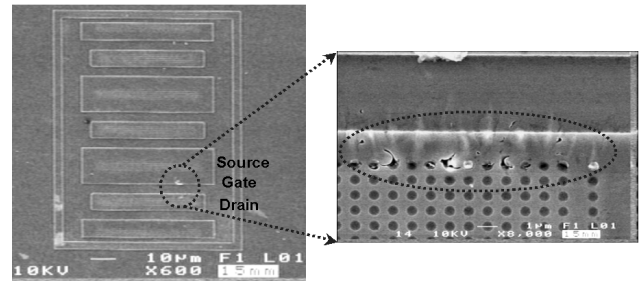


FIGURE 7. THE SEM FAILURE PICTURE OF HV NSCR AFTER 2-kV HBM ESD STRESS.