MECHANISM OF SNAPBACK FAILURE INDUCED BY THE LATCH-UP TEST IN HIGH-VOLTAGE CMOS INTEGRATED CIRCUITS

Jen-Chou Tseng (1), Yu-Lin Chen (1), Chung-Ti Hsu (1), Fu-Yi Tsai (1), Po-An Chen (1), Ming-Dou Ker (2)

(1) Device Technology Development Division, Emerging Technology Center, Winbond Electronics Corporation
E-mail：cthsu1@winbond.com

(2) Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C.
E-mail：mdker@ieee.org

ABSTRACT

An electrical overstress failure induced by a latch-up test is studied in high-voltage integrated circuits. The latchup test resulted in damage to the output NMOSFET due to snapback and also resulted in a latch-up in the internal circuits. These mechanisms are analyzed and solutions are proposed to avoid the triggering of the output NMOSFET and the resulting latchup issue.

[*Keywords:* ESD, EOS, latch-up, high-voltage.]

1. INTRODUCTION

As the device density and the supply voltage increases in high-voltage IC's, parasitic effects induced by latch-up tests are becoming an increasing concern [1]. Such tests could result in mis-triggering of parasitic bipolar-junction transistors (BJTs) and silicon-control rectifiers (SCRs) and can lead to a permanent damage [2-4]. In the operation of high-voltage (HV) n-channel metal-oxide-semiconductor field-effect transistor (NMOSFET), the high drain electric field results in impact ionization inducing large substrate currents [5]. The large-size HV NMOSFET is prone to snapback and non-uniform turn-on of its parasitic bipolar transistor due to the relatively large substrate current and substrate resistance. In this paper, the test-induced snapback damage of the output NMOSFET and the resulting latch-up in the internal circuits were both found after the latch-up trigger duration. The mechanisms of failures were analyzed and design solutions are proposed.

2. FAILURE SYMPTOM AND ANALYSIS

Two versions of a HV pulse width modulation (PWM) ICs were fabricated in a conventional 0.6μm, 13.5V p-substrate CMOS process. For the output-driver pin, the spacing between NMOSFET drain-side contact and poly gate was enlarged to 10um to increase the ballast resistance to enhance the ESD performance (3kV). In version A of the IC, failures occurred at the output-driver pin after negative latch-up current test (-100 mA) performed per JEDEC Standard No. 78. A burnout mark was found at the metal interconnection between power pad (VDDA = 12V) and the source of PMOSFET, and another burnout was found at the metal interconnection to the internal power regulator (VDD = 9V). Figure 1 shows the emission microscopy (EMMI) hot spot of the internal circuits during latch-up test as well as the damage at the metal interconnection of internal power regulator circuit. Based on the failure signatures, latch-up was suspected to have occurred in the parasitic SCR formed between NMOSFET and PMOSFET of the output pin. Then, the substrate current is induced and further triggers the internal parasitic SCR path.

To prevent the latch-up failure, layout revisions were made for the version-B IC. The widths of metal interconnections of output PMOSFET and the internal power regulator were both enlarged to endure higher power. The finger widths of poly-silicon gates of output N/PMOSFETs were reduced and more pick-up rings were used to decrease the parasitic resistances of p-substrate/N-Well. The spacing between the output NMOSFET and PMOSFET was also enlarged 3.75 times to reduce the current gain of the parasitic SCR. However, latch-up failures still occurred after the revision. Figure 2 shows the EMMI hot spots during latch-up test as well as the damage of output NMOSFET. Hot spots appeared at the output NMOSFET and the internal circuits. While, the previous burnout of metal interconnection between power pad and the source of PMOSFET disappeared, another burnout was found at the drain region of output NMOSFET. Since the p-n-p-n SCR path exists always between the source regions of NMOSFET and PMOSEEFT, the burnout is expected to be observed at the source region of N/PMOSFET in a latch-up event. Hence, it can be concluded that the failure is not caused by latch-up of parasitic SCR formed between the output NMOSFET and PMOSFET. The snapback of the parasitic NPN BJT was suspected to be the root cause of the failure and induced a latch-up event at the internal circuits.

3. EXPERIMENTAL RESULTS AND DISCUSSION

A. Effects of the output state and supply voltage

To verify the assumption of snapback of the NMOSFET, the supply voltages and output states were varied for the output pin. Table 1 shows the latch-up test results of -100 mA trigger of version-B IC. As indicated in Table 1, the failure occurred when the PMOSFET is "on" and the voltage applied on the drain of NMOSFET is high. Figure 3 shows the schematic diagrams of the output pin during negative current test. For the failure case, the pad voltage is first pulled low and trigger current is drawn from the channel of PMOSFET. This in turn results in the pad voltage being pulled high very fast by the big PMOSFET. The resulting large voltage surge is applied to the drain of NMOSFET. Simultaneously, a large displacement current may be also induced due to the transient change of applied voltage that flows through the source and bulk of the NMOSFET. As the voltage drop across the emitter/base junction of parasitic NPN BJT of the NMOSFET exceeds the cut-in voltage, the parasitic NPN BJT enters snapback operation. Large current is therefore conducted from the PMOSFET channel to the parasitic NPN BJT, and the inherent non-uniform current distribution finally destroys this big NMOSEFT.

Based on the on-chip measurement and HSPICE simulation, it is evident that the PMOSFET's current driving capability is greater than 100mA. All the injected currents I_{inj} (-100mA) will be sunk by PMOSFET to *VDDA*. The pad voltage will equal to "VDDA – I_{inj} $\times R_{PMOSFET}$" and always keeps above 0V. No current will flow through the N+/PW diode. On the contrary, if the driving capability of PMOSFET is less than 100mA, the N+/PW diode will start to sink a part of the injected trigger currents. The pad voltage will then be clamped by the N+/PW diode to below 0V.

B. Effect of the substrate noise and resistance

To simulate the effect of parasitic substrate noise on the snapback voltage, different substrate currents were forced into the bulk (VSSA pad) of NMOSEFT from the adjacent VSSD pad. Figure 4 shows the I-V curves of the parasitic NPN BJT of NMOSFET in version-B IC under different injected substrate currents measuring by Tektronix–370A curve tracer. The snapback voltage can be reduced below 12V when the substrate current exceeds 1.85mA. The holding voltages are less than 12V even without injected substrate current. Thus, the device can be triggered into self-biased region by the injected substrate current and large current can be drawn from the power supply. Figure 5 shows the I-V measurement results of the parasitic NPN BJTs of NMOSFETs

978-1-4244-2050-6/08/$25.00 ©2008 IEEE

with different device sizes and parasitic substrate resistances. The small-size NMOSFET has the smaller parasitic substrate resistance than the large-size NMOSFET due to the smaller distance between source and substrate pick-up ring. For the same channel width, the revised device in version-B IC has a smaller parasitic substrate resistance than the original device in version-A IC because of the larger number of pick-up rings. Consequently, the large-size NMOSFET in version-A IC has the lowest snapback voltages than the other devices.

C. Design considerations

To resolve the latch-up test issue in this case, the standby state of this output pin had better be changed from "high" to "low" to turn off the big PMOSFET buffer. This in turn avoids the undershoot noise from power supply after the current test.

4. Conclusion

In this study, the mechanism of latch-up-test-induced failures in the HV PWM ICs is investigated. During the negative current test, the voltage of output pin is first pulled low by the external trigger source and then transiently pulled high by the big PMOSFET buffer. This results in a large undershoot voltage surge and a large substrate noise is induced. This substrate noise results in snapback damage of the parasitic NPN BJT of the big NMOSFET buffer. In addition, the snapback event produces additional substrate currents which further trigger the parasitic SCR path in internal circuits. To avoid this issue, it is recommended that the standby state of output pin be changed to turn off the big PMOSFET buffer. This avoids the undershoot noise from power supply during the latch-up current test.

References

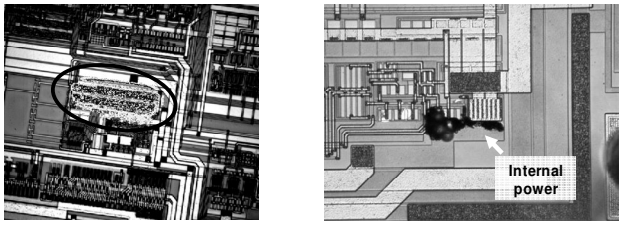
[1] V. Khemka, et al., *IEEE Trans. on Device and Materials Reliability*, vol. 7, no. 1, pp. 69–73, 2007.

[2] M. D. Ker and K. H. Lin, *IEEE Electron Device Letters*, vol. 25, no. 9, pp. 640–642, 2004.

[3] I. C. Lin, et al., *EOS/ESD Symposium 2004*, pp. 160–165.

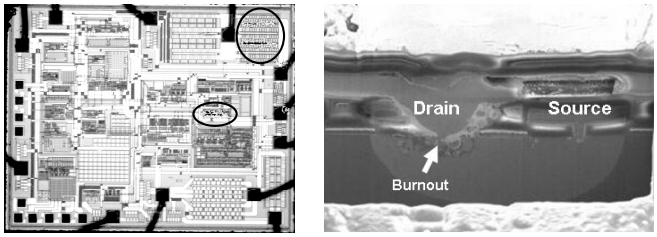
[4] J. S. Suner, et al., *International Reliability Physics Symposium 2003,* pp. 85-91.

[5] Y. Fong, et al., *IEEE Trans. on Electron Devices*, vol. 37, no. 9, pp. 2101–2103, 1990.



(a) (b)

FIGURE 1. (a) The EMMI hot spot of the internal circuits during latch-up test as well as (b) the damage at the metal interconnection of internal power regulator circuit.



(a) (b)

FIGURE 2. (a) The EMMI hot spots during latch-up test of version-B IC. (b) The cross-section view of the damage of output NMOSFET.

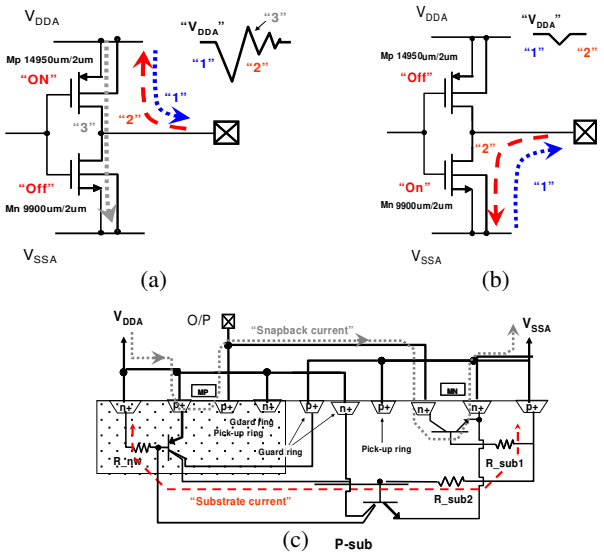


FIGURE 3. The schematic diagrams of the output pin during negative current test when the output state is (a) "high" and (b) "low." (c) paths of substrate current and snapback current as the output is "high."

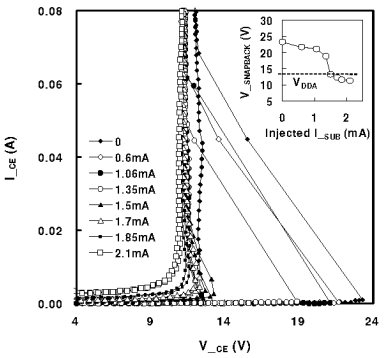


FIGURE 4. The I-V curves of the parasitic NPN BJT of NMOSFET in version-B IC under different injected substrate currents.

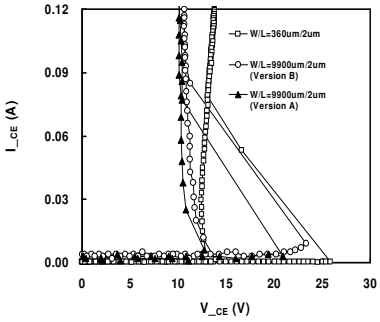


FIGURE 5. The I-V measurement results of the parasitic NPN BJTs of different NMOSFETs. The small-size device has the smallest parasitic substrate resistance due to the smallest distance between source and substrate pick-up ring. And, the revised device in version-B IC has a smaller parasitic substrate resistance than the original device in version-A IC because of the larger number of pick-up rings.

V_{DDA}	Output	NMOSFET	PMOSFET	Test result
6V	High	Off	On	Pass
7V	High	Off	On	Fail
12V	High	Off	On	Fail
12V	Low	On	Off	Pass

TABLE 1. The supply voltages and output states were split for the output pin of version-B IC during -100mA latch-up test. The failure occurred as the PMOSFET is "on" and supply voltage is higher than 7V.