2xVDD-Tolerant Crystal Oscillator Circuit Realized With 1xVDD CMOS Devices Without Gate-Oxide Reliability Issue

Ming-Dou Ker, Tzu-Ming Wang, and Hung-Tai Liao
Nanoelectronics and Gigascale Systems Laboratory
Institute of Electronics, National Chiao-Tung University
1001 Ta-Hsueh Road, Hsinchu, Taiwan 300, R.O.C.

***Abstract*—A new 2xVDD-tolerant crystal oscillator circuit realized with 1xVDD CMOS devices without suffering gate-oxide reliability issue is proposed, which is one of the key mixed-voltage I/O cells in a cell library. The proposed circuit is realized with only thin gate-oxide devices with floating n-well technique. The proposed 2xVDD-tolerant crystal oscillator circuit has been designed and verified in a 90-nm 1-V CMOS process to serve 1/2-V mixed-voltage interface applications.**

I. INTRODUCTION

In modern CMOS technology, the CMOS processes have been scaled down to reduce the silicon cost and increase the performance of transistors. In order to reduce the power consumption, the lower power supply voltage is used and the thickness of gate oxide also becomes thinner. Therefore, the maximum tolerable voltage across the transistor terminals (drain, source, gate, and bulk) should be correspondingly decreased to ensure lifetime. The normal lifetime is typically 5-10 years with continuous operation under specified worst-case operating conditions. That means the circuits or transistors are supposed to be operated correctly without function error or leakage issue at least for 5-10 years at normal power supply voltage level.

Some standardized protocols or other integrated circuits (ICs) in a microelectronic system could be still operated at the higher voltage levels, such as 3.3-V or 5-V [1]–[4]. In other words, this microelectronic system would have several components operated at different voltage levels. In order to interface these components with different voltage levels, the mixed-voltage I/O interface circuit must be designed to overcome several problems between these components, such as the gate-oxide breakdown [5], the hot-carrier degradation [6], and the undesirable leakage current paths [7].

The conventional Pierce-type crystal oscillator circuit used in the I/O interface circuit is shown in Fig. 1 [8]. The inverting amplifier supplies a voltage gain and 180 degree phase shift. The crystal combined with C1 and C2 to form a feedback network that tends to stabilize the frequency and 180 degree phase shift. The feedback resistance, Rf, is used to bias the inverting amplifier. The condition for proper start-up and sustaining oscillation is that the closed loop gain should be over or equal to one. In addition, the circuit should have an overall phase shift around 360 degree in steady state so the oscillation can be sustained.

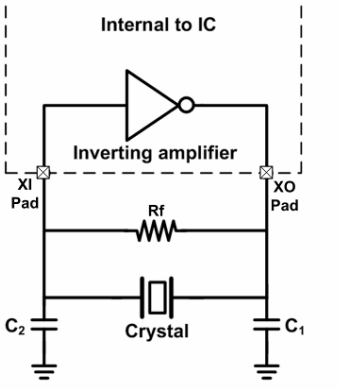


Figure 1. Pierce-Type crystal oscillator circuit [8].

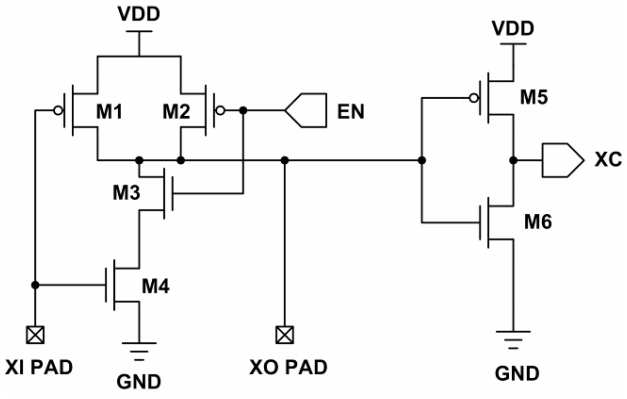


Figure 2. The conventional crystal oscillator circuit realized with the 1xVDD devices.

In the advanced CMOS process, the thin-oxide devices can be operated at a higher operating frequency under a lower supply voltage. But components on the board are still operated at the higher voltage level. Therefore, the mixed-voltage I/O library, which includes the digital and analog I/O cells, power/ground/cells and crystal oscillator cells, should be designed with consideration on gate-oxide reliability problem. Fig. 2 shows the conventional crystal oscillator circuit realized with the 1xVDD devices. When the EN signal is kept at VDD and the external input clock signal at the XI pad rises up to 2x VDD. M1 and M4 would suffer the gate-oxide overstress problem. In order to avoid the gate-oxide problem, one way is to replace M1 and M4 to the thick-oxide devices in the chip. However, the fabrication cost of CMOS process is increased. Circuit solution to solve this mixed-voltage application on crystal pad is highly requested by IC industry.

In this paper, a new 2xVDD-tolerant crystal oscillator circuit with only thin-oxide CMOS devices is proposed. The proposed circuit uses the gate tracking circuit and floating n-well technique without extra control signal to solve the gate-oxide reliability problem. The proposed mixed-voltage-tolerant crystal oscillator circuit has been designed and verified in a 90-nm 1-V CMOS process to serve 1/2-V mixed-voltage interface application.

II. Proposed 2xVDD-Tolerant Crystal Oscillator Circuit

Fig. 3 shows the proposed 2xVDD-tolerant crystal oscillator realized with only 1xVDD thin-oxide devices. XI pad and XO pad are the input and output pads of the proposed 2xVDD-tolerant crystal oscillator circuit, respectively. Signal EN is controlled by the internal circuits of IC, as that used in Fig. 2. XC is the clock signal which is produced by crystal oscillator circuit or to receive the external clock signal into the IC. The transistors MN2, MN3, MP2, and MP3 form the inverting amplifier of the proposed 2xVDD-tolerant crystal oscillator circuit. Inverters INV4 and INV5 can transfer the sinusoidal-wave signal to a square signal or pass the external clock signal into the internal input node XC.

A. Oscillation mode

It is operated to generate the sinusoidal-wave signal at both XI pad and XO pad, when the proposed 2xVDD-tolerant crystal oscillator circuit is with crystal and two load capacitances (C1 and C2). Transistors MP4 and MP5 are turned off and transistor MN4 is turned on with the gate terminals connected to power supply (VDD). The sinusoidal-wave signal whose voltage level is less than VDD-Vt can pass through the transistor MN1 to the input terminal (N01) of the nand gate, and oscillation starts up. When the low voltage level is at the input terminal (N01) of the inverter INV1, the transistor MN5 is turned on to bias the gate terminal of the transistor MP1 at GND and the inverters INV2 and INV3 hold the voltage level. The sinusoidal-wave signal, even if the voltage level is over VDD-Vt, can pass through the transistor MP1 to the input terminal (N01) of the nand gate. It means that the sinusoidal-wave signal could completely pass through the transistors MN1 and MP1 to the gate terminal of the nand gate without distortion. Transistor MP6 is turned on to bias the floating N-well (FNW) at VDD.

B. Receiving mode

For the mixed-voltage interface applications, the proposed 2xVDD-tolerant crystal oscillator circuit will be used to receive an external clock input signal whose voltage level could be 1xVDD or 2xVDD. In order to limit the voltage level of clock input signal reaching to the gate oxide of the nand gate, transistor MP4 is used to track the signal at the XI pad and control the gate voltage of transistor MP1. When the voltage level at the XI pad exceeds VDD+|Vtp|, such as 2xVDD, transistor MP4 is turned on to charge the gate terminal of transistor MP1 up to 2xVDD.

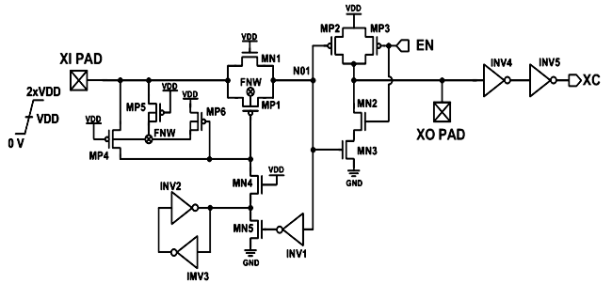
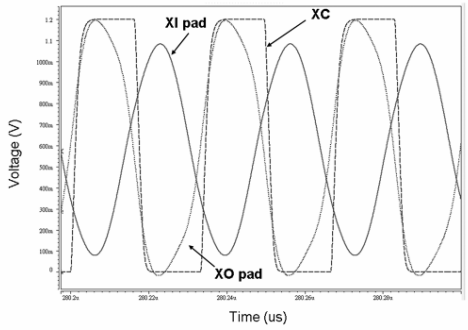
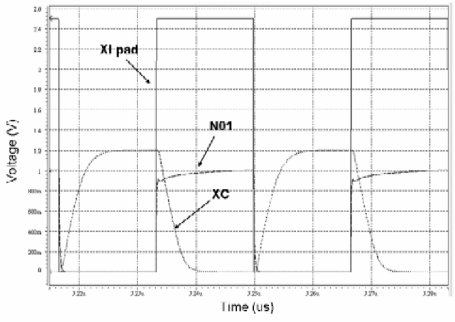


Figure 3. The proposed 2xVDD-tolerant crystal oscillator circuit realized with 1xVDD CMOS devices.



(a)



(b)

Figure 4. The simulated waveforms of the new proposed 2xVDD-tolerant crystal oscillator circuit with (a) a crystal of fundamental frequency 30-MHz, load capacitance 20-pF at the XI and XO pad, and load capacitance 5-pF at the XC pad, and (b) 30-MHz external clock signal of 2xVDD into XI pad with 20-pF load capacitance at XC pad.

Transistor MP1 is completely turned off to prevent the voltage level at the input terminal (N01) of the nand gate from rising up to 2xVDD. Transistor MP5 is turned on and transistor MP6 is turned off to bias the floating N-well (FNW) at 2xVDD. Besides, when the voltage level of XI pad is at GND, the transistor MN5 will be turned on by inverter INV1 to turn on the transistor MP1. Transistor MP5 is turned off and transistor MP6 is turned on to bias the floating N-well (FNW) at VDD.

C. *Simulation results*

Fig. 4 shows the simulation waveform of the proposed 2xVDD-tolerant crystal oscillator circuit in a 90-nm 1-V CMOS process to serve 1/2-V mixed-voltage interface. In Fig. 4 (a), the proposed 2xVDD-tolerant crystal oscillator circuit with the crystal of 30-MHz fundamental frequency, load capacitance 20-pF at the XI and XO pad, and load capacitance 5-pF at the XC pad, can successfully generate the clock signal of 30-MHz at the XC node under the power supply of 1xVDD. As shown in Fig. 4 (b), with the 30-MHz external clock signal of 2xVDD into XI pad with 20-pF load capacitance at XC pad, the input terminal (N01) voltage of the nand gate can be limited and biased at the voltage level (0.8V). The final signal voltage level reaching to the XC node is successfully shifted down to 1xVDD. From the simulation results, the desired functions of the proposed 2xVDD-tolerant crystal oscillator circuit have been verified.

III. EXPERIMENTAL RESULTS

Fig. 5 shows the layout view of the new proposed 2xVDD-tolerant crystal oscillator circuit implemented in a 90-nm 1-V CMOS process. The cell size of XI, as well as XO, is only 190.5μm x 60μm (including the bond pad), which is the same as that of digital or analog I/O cell in a standard I/O cell library. The feedback resistor Rf, implemented by poly resistor, is also included into the layout. ESD protection is also provided with the ESD design rules given by the foundry to draw the layout for NMOS and PMOS devices which are directly connected to the pads.

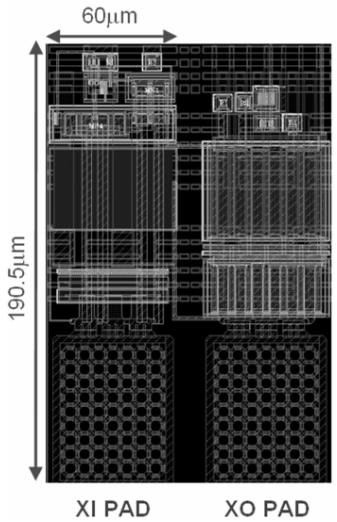


Figure 5. The layout view of proposed 2xVDD-tolerant crystal oscillator circuit.

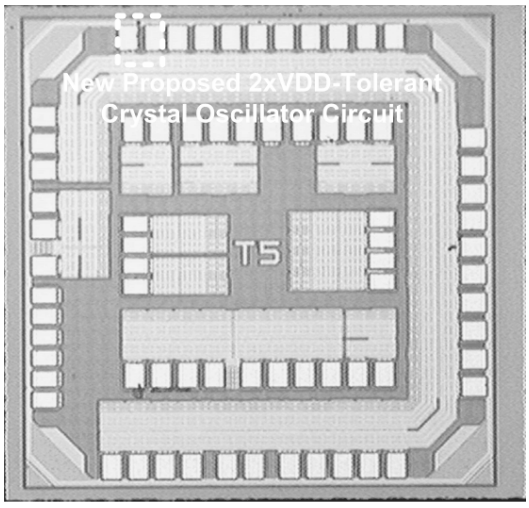


Figure 6. The die photo of new proposed 2xVDD-tolerant crystal oscillator circuit farbricated in a 90-nm CMOS process.

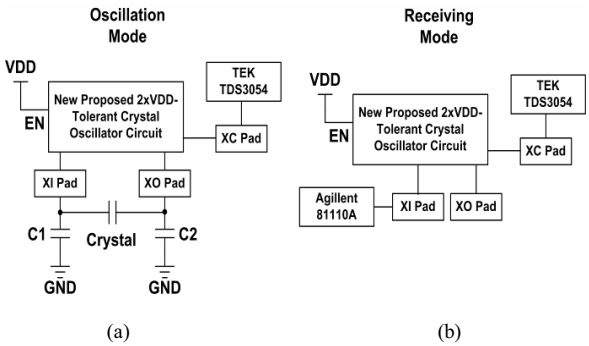


Figure 7. The measurement setup of the new proposed 2xVDD-tolerant crystal oscillator circuit in (a) oscillation mode and (b) receiving mode.

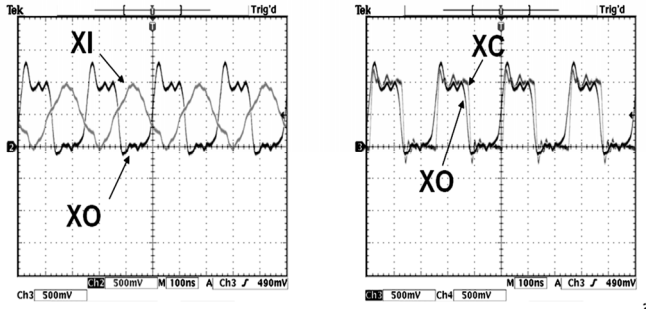
Fig. 6 is the die photo of the new proposed 2xVDD-tolerant crystal oscillator circuit implemented in a 90-nm CMOS process. Fig. 7 shows the measurement setup in (a) oscillation mode and (b) receiving mode.

To test the function of the new proposed 2xVDD-tolerant crystal oscillator circuit in oscillation mode for the external crystal of fundamental frequency 4-MHz and 20-MHz, an external crystal is connected between the input pad (XI) and the output pad (XO) of the fabricated 2xVDD-tolerant crystal oscillator circuit with two external capacitors (C1=C2=20-pF) respectively connected in the input pad (XI) and the output pad (XO). The control signal EN is biased at VDD.

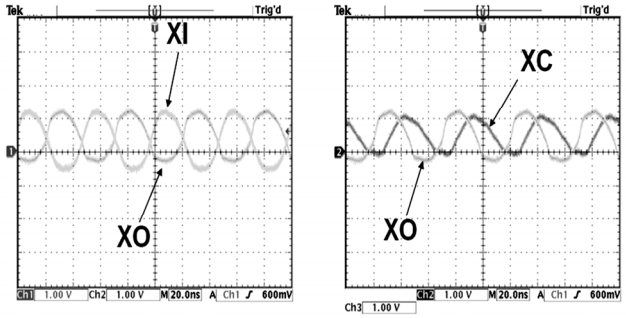
The measurement results are shown in Fig. 8. In Fig. 8 (a) and (b), the new proposed 2xVDD-tolerant crystal oscillator circuit can successfully transmit the 0/1-V clock signal of frequency 4-MHz and 20-MHz to the XC node, respectively.

To test the function of the new proposed 2xVDD-tolerant crystal oscillator circuit in receiving mode for 0/1-V and 0/2-V external clock signals of frequency 4-MHz at the input pad (XI), the XI pad is used as the input pad to receive the external clock signal from the pulse generator and the external clock signal will be transmitted to XC pad, which is monitored in oscilloscope. The control signal EN is kept at VDD.

The measurement results shown in Fig. 9 and Fig. 10, the new proposed 2xVDD-tolerant crystal oscillator circuit can successfully transmit the 0/1-V external clock signal of frequency 4-MHz to the XC node with the input clock signal of 0/1-V and 0/2-V external clock signals, respectively.



(a)



(b)

Figure 8. The measurement results of the new proposed 2xVDD-tolerant crystal oscillator circuit. In oscillation mode with a crystal of fundamental frequency at (a) 4-MHz, and (b) 20-MHz.

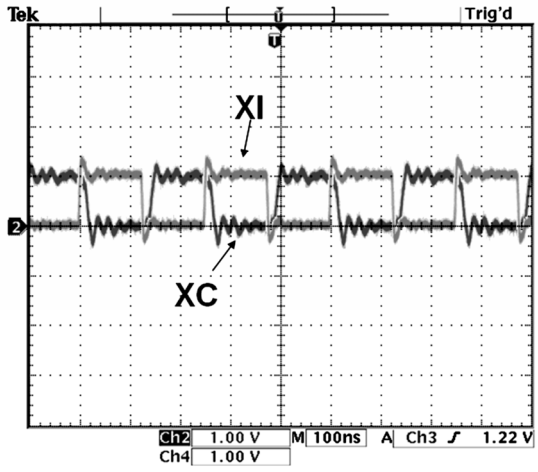


Figure 9. The measurement results of the new proposed 2xVDD-tolreant crystal oscilllator circuit in receiving mode with a 4-MHz 0/1-V external input clock signal.

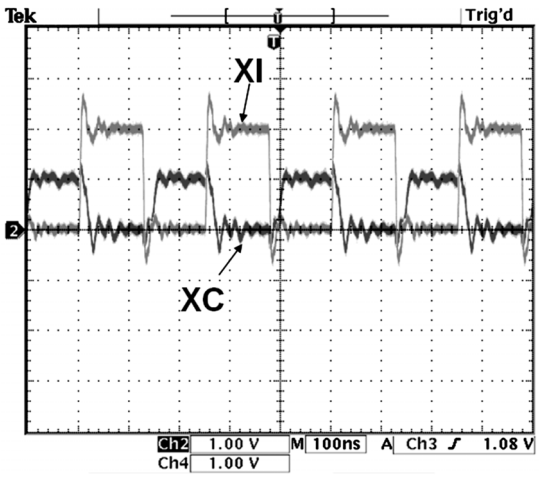


Figure 10. The measurement results of the new proposed 2xVDD-tolerant crystal oscillator circuit in receiving mode with a 4-MHz 0/2-V external input clock signal.

IV. Conclusion

A new proposed 2xVDD-tolerant crystal oscillator circuit has been successfully designed and implemented in a 90-nm 1-V CMOS process, which can be operated in the 1/2-V signal environment without the gate-oxide reliability problem. The new mixed-voltage-tolerant crystal oscillator circuit can be applied for external clock signal in the input pad (XI) without the gate-oxide reliability problems. The new mixed-voltage-tolerant crystal oscillator circuit realized with 1xVDD devices can be applied in 1xVDD/2xVDD mixed-voltage interface.

References

[1] J. Williams, "Mixing 3V and 5V ICs," *IEEE Spectrum*, pp. 40-42, 1993.

[2] G. P. Singh and R. B. Salem, "High-voltage-tolerant I/O buffers with low-voltage CMOS process," *IEEE J. Solid-State Circuits*, vol. 34, no. 11, pp. 1512-1525, Nov. 1999.

[3] M.-D. Ker and C.-H. Chung, "Electrostatic discharge protection design for mixed-voltage I/O buffers," *IEEE J. Solid-State Circuits*, vol. 37, no. 8, pp. 1046–1055, Aug. 2002.

[4] M.-D. Ker, S.-L. Chen, and C.-S. Tsai, "Overview and design of mixed-voltage I/O buffers with low-voltage thin-oxide CMOS transistors," *IEEE Trans. on Circuits and Systems I*, vol. 53, no. 9, pp. 1934-1945, Sept. 2006.

[5] R. S. Scott, N. A. Dumin, T. W. Hughes, D. J. Dumin, and B. T. Moore, "Properties of high-voltage stress generated traps in thin silicon oxide," *IEEE Trans. Electron Devices*, vol. 43, no. 7, pp. 1133–1143, Jul. 1996.

[6] I.-C. Chen, J. Y. Choi, and C. Hu, "The effect of channel hot-carrier stressing on gate-oxide integrity in MOSFETs," *IEEE Trans. Electron Devices*, vol. 35, no. 12, pp. 2253–2258, Dec. 1988.

[7] S. Voldman, "ESD protection in a mixed voltage interface and multi-rail disconnected power grid environment in 0.5- and 0.25-µm channel length CMOS technologies," in *Proc. EOS/ESD Symp.*, 1994, pp. 125–134.

[8] A. Pauptit and E. Nordberg, "X-tal oscillators on 8-bit microcontrollers," Philips Semiconductors, Netherlands, Application Note AN96103, Sep. 1996.