ESD Protection Design for Fully Integrated CMOS RF Power Amplifiers With Waffle-Structured SCR

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***Abstract*—Waffle-structured SCR (silicon-controlled rectifier) has been studied as an effective on-chip ESD (electrostatic discharge) protection device for CMOS RF (radio-frequency) circuits. In this work, a novel on-chip ESD protection strategy using the waffle-structured SCR is proposed and co-designed with a CMOS UWB (ultra-wideband) PA (power amplifier). Before ESD stress, the RF performances of the ESD-protected PA have been demonstrated to be as well as that of the unprotected PA. After ESD stress, the unprotected PA was seriously degraded, whereas the ESD-protected PA was keeping the performances well.**

I. INTRODUCTION

It has been a trend to integrate the whole RF (radio-frequency) circuits into a single chip [1]. CMOS technology is the leading role to integrate RF circuits. A power amplifier (PA) is an important building block of RF transmitter. With the scaling-down feature size and lower cost, nanoscale CMOS technology has become suitable to implement RF PA. However, the thin gate oxide in advanced CMOS processes seriously degrades the reliability of IC (integrated circuit) products. The major reliability issue for IC products is the damage caused by ESD (electrostatic discharge) zapping. Against ESD damages, on-chip ESD protection circuit must be included in IC products.

A general concept of on-chip ESD protection for RF ICs is illustrated in Fig. 1 [2]-[4]. The ESD protection devices at I/O pad and the power-rail ESD clamp circuit must be provided in RF ICs to accomplish the whole-chip ESD protection. The parasitic capacitance (C_{ESD}) of ESD protection device certainly contributes capacitive loading to the I/O port, which will induce impedance mismatch, power gain degradation, output power loss, and noise figure degradation. The parasitic capacitance of ESD protection circuits is an important design consideration for RF ICs [4], [5]. To reduce the negative impact of ESD protection circuit on RF circuit performance, waffle-structured layout for ESD protection devices had been studied [6]. As compared to the stripe-structured devices, the waffle-structured devices have been demonstrated to lower the parasitic capacitance under the same ESD robustness. To further reduce the negative impact from ESD device on RF performance, the better solution is to co-design the RF circuit with the ESD protection device. If it is possible to integrate the ESD protection circuit into the RF core circuit, the negative impact on RF performance may vanish.

This paper presents a fully integrated UWB (ultra-wideband) class-AB PA co-designed with ESD protection circuit. The PA with and without the proposed ESD protection circuit are designed and fabricated in a 0.13-μm CMOS process. The effects of ESD protection circuit on RF performances and ESD robustness are investigated and verified in the silicon chip.

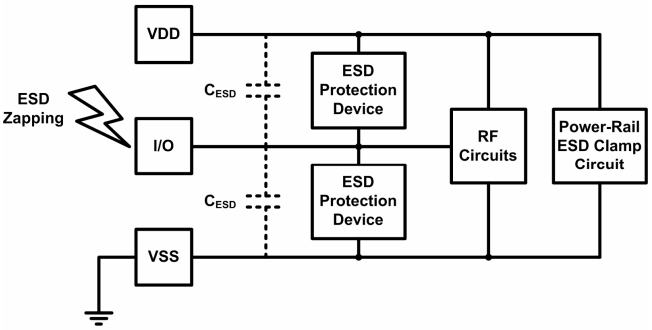


Figure 1. A general concept of on-chip ESD protection in RF ICs.

II. CIRCUIT DESIGN

A. UWB Class-AB PA

The presented UWB class-AB PA is a three-stage DA (distributed amplifier). The UWB applications cover the frequency band from 3.1 GHz to 10.6 GHz. The DA is intrinsically suitable for this bandwidth and widely used for PA [7]. Fig. 2 shows the equivalent circuit of the presented PA. The active core devices (M1 and M2) of each stage are in cascode topology. The cascode topology provides good voltage gain and good isolation. It also prevents drain overstress since the voltage swing may approach two times of

This work was supported by United Microelectronics Corporation (UMC), Taiwan.

VDD at the output node. The PA was simulated by using Agilent ADS (Advanced Design System) simulation tool. The device size and voltage/current bias of the cascode pair is designed to produce a particular current that gives the active core device with a 50-Ω loading for its optimal load-line resistance within its operational dynamic range. With such a manner, the DA can simultaneously satisfy a 50-Ω conjugate match and optimal load-line match.

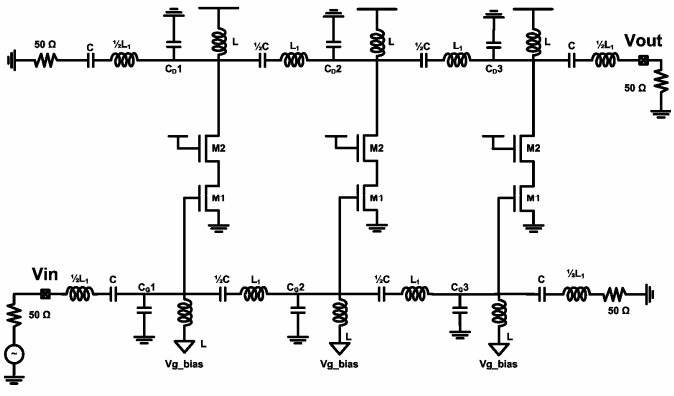


Figure 2. The equivalent circuit of the presented PA.

B. *UWB Class-AB PA with ESD Protection*

In general ESD protection architecture for RF circuits, as shown in Fig. 3, diode strings were connected from VSS to I/O and I/O to VDD, along with a power-rail ESD clamp circuit to provide the on-chip ESD protection. However, this kind of ESD protection strategy often suffers the worse PS-mode (positive-to-VSS) ESD robustness due to its too long discharging path [8]. To shorten the discharging path and improve ESD robustness, the UWB class-AB PA with the proposed ESD protection circuit is shown in Fig. 4. It contains a waffle-structured diode string from O/P to VDD, and a waffle-structured SCR from O/P to VSS with a RC-inverter as a trigger circuit. Besides, another set of RC-inverter-triggered SCR acts as the power-rail ESD clamp circuit to provide the discharging path when the ESD was zapping from VDD to VSS. The RC time constants of the trigger circuits were designed in the order of microsecond to detect ESD events. Under normal circuit operation, ESD protection circuits were all kept off. During PS-mode ESD stress, with ESD pulses zapping to the protected PA, ESD current will first pass through the diodes to VDD and then RC-inverter to trigger the waffle-structured SCR. The major ESD current will be discharged by the waffle-structured SCR from the O/P pad to VSS. Therefore, the ESD protection ability can be significantly improved. Under other ESD events, including PD-mode (positive-to-VDD), NS-mode (negative-to-VSS), ND-mode (negative-to-VDD), positive VDD-to-VSS, and negative VDD-to-VSS, the proposed ESD protection circuit also provides the corresponding current discharging paths with good ESD robustness.

The waffle-structured SCR and diodes were applied in this ESD protection design. The layout top view and the device cross-sectional view of the waffle-structured SCR are shown in Figs. 5(a) and 5(b). The waffle-structured SCR can conduct ESD current through four edges rather than two edges of the stripe-structured SCR. Therefore, the discharging capability can be increased by using the waffle layout structure to implement SCR. The waffle-structured SCR with a smaller device size and a lower parasitic capacitance is more suitable as ESD protection device to co-design with the RF PA.

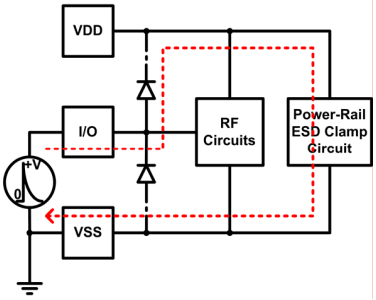


Figure 3. The ESD protection strategy for RF circuits, and its discharging path under PS-mode ESD zapping.

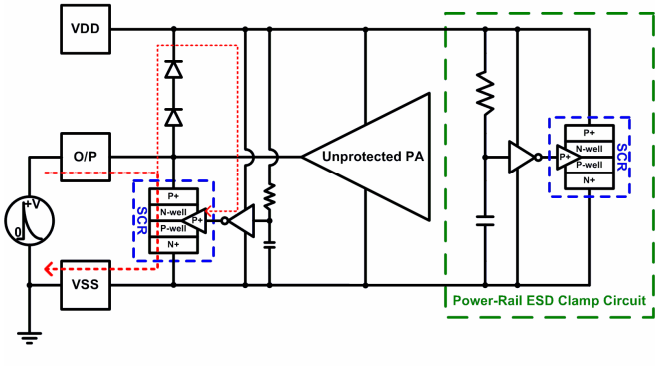
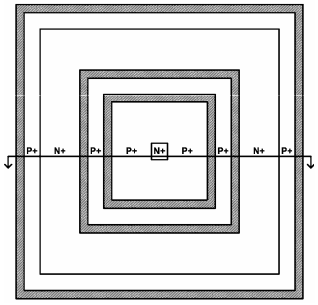
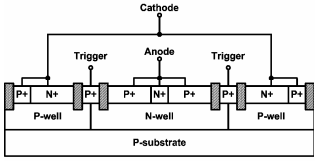


Figure 4. The equivalent circuit of the presented PA with the proposed ESD protection circuit, and its discharging path under PS-mode ESD zapping.



(a)

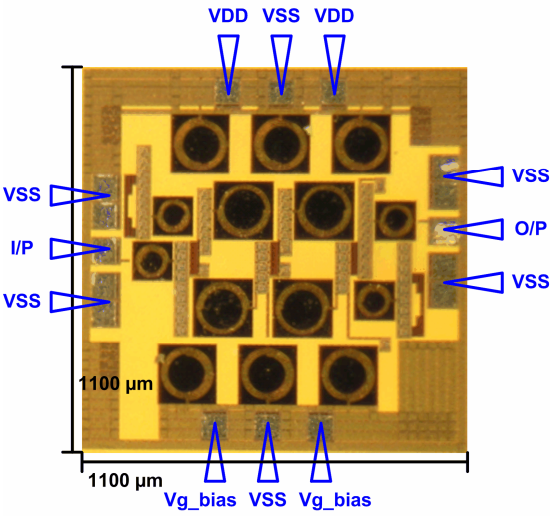


(b)

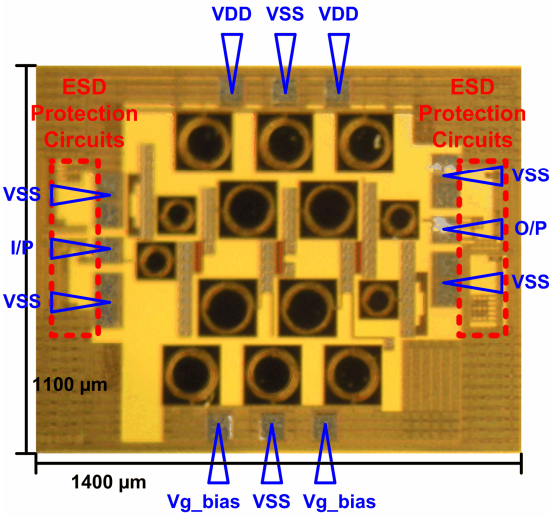
Figure 5. (a) Layout top view, and (b) device cross-sectional view, of the waffle-structured SCR.

III. Experimental Results

The die photos of the fabricated chips of the unprotected PA and ESD-protected PA are shown in Figs. 6(a) and 6(b), respectively. The S-parameters of the PAs were measured by using the Agilent E8364B PNA. An Agilent E4448A spectrum analyzer and an Agilent E8257D signal generator were used to evaluate the large signal characteristics of the PAs. To compare the ESD protection capability, the RF performance of PA was measured again after each human body model (HBM) ESD zapping. The HBM ESD pulses were zapped by the ESD simulator.



(a)

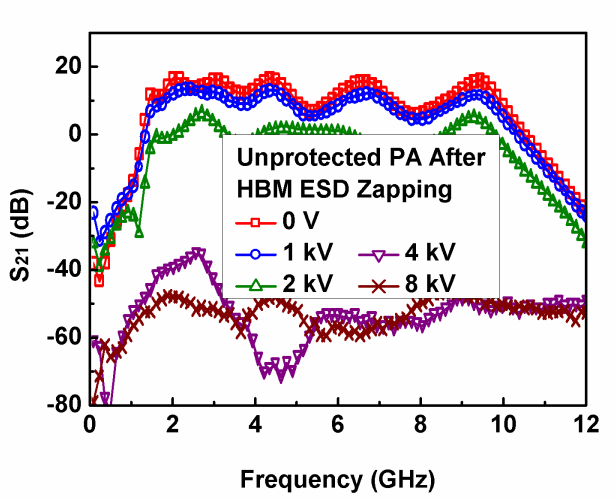


(b)

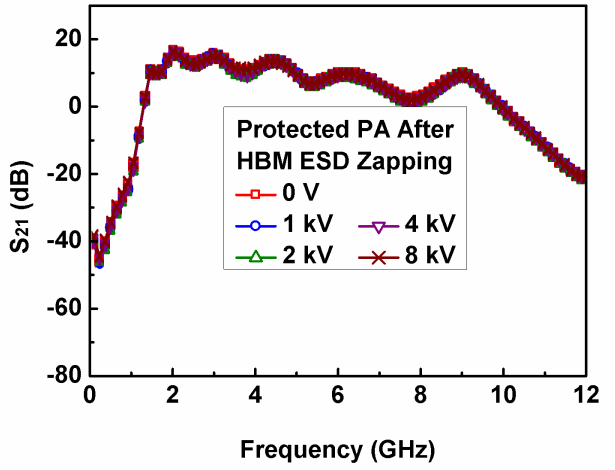
Figure 6. Die photos of the fabricated (a) unprotected PA and (b) ESD-protected PA.

The S_{21}-parameter is the forward gain of the PA. The measured results of the S_{21} from 0 to 12 GHz of the unprotected PA and ESD-protected PA are shown in Figs. 7(a) and 7(b). The S_{21} of the unprotected PA was severely degraded after HBM ESD zapping, as seen in Fig. 7(a). On the contrast, the S_{21} of the ESD-protected PA was still excellent matching even if the 8-kV HBM ESD test was performed (8-kV is the maximum limitation of ESD simulator). The bandwidths of the PAs after each HBM ESD zapping are summarized in Table I.

The averaged large signal power gain of the fabricated PAs in 3.1~10.6 GHz are listed in Table II. When the output power increases, the output swing would be compressed. The output power at 1-dB compression point, OP1dB, can be treated as the maximum linear output power capability of the PA. Figs. 8(a) and 8(b) show the measured results on the OP1dB of the unprotected PA and ESD-protected PA, respectively. The OP1dB of the unprotected PA was seriously degraded after HBM ESD zapping. The OP1dB of the ESD-protected PA was not degraded even after 8-kV HBM ESD test. The failure die photo of the unprotected PA after 8-kV HBM ESD zapping is shown in Fig.9. The failure point was located at the output inductor due to VIA melting.

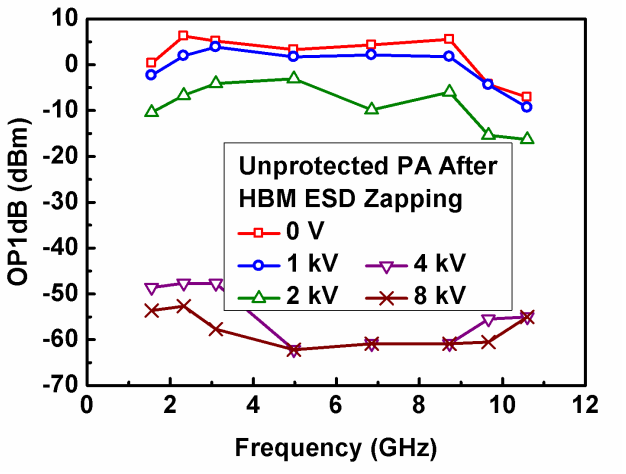


(a)

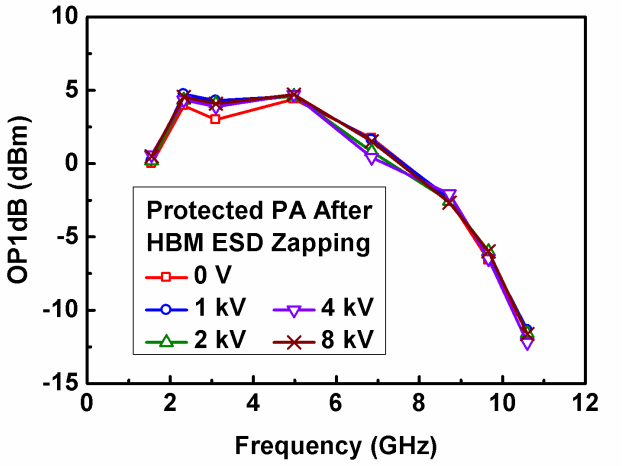


(b)

Figure 7. Measured results on the S_{21}-parameter of the (a) unprotected PA and (b) ESD-protected PA, after each HBM ESD zapping.



(a)



(b)

Figure 8. Measured results of output power 1-dB compression point of the (a) unprotected PA and (b) ESD-protected PA, after each HBM ESD zapping.

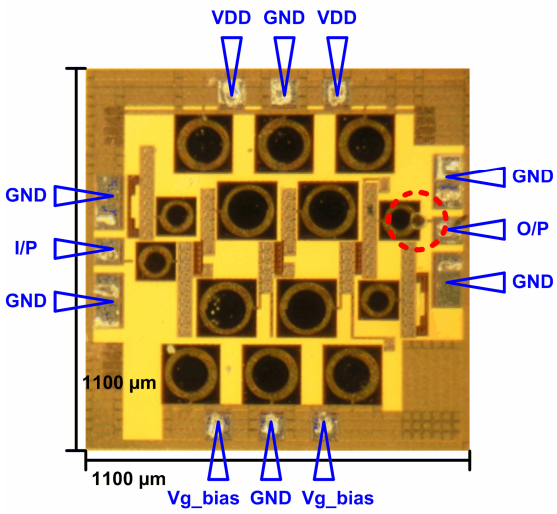


Figure 9. Die photo of the unprotected PA after 8-kV HBM ESD zapping. The failure point is at the output inductor due to VIA melting.

TABLE I. BANDWIDTH OF PA AFTER HBM ESD ZAPPING

HBM ESD Zapping	Bandwidth	
	Unprotected PA	*ESD-Protected PA*
0 V	7.8 GHz	7.3 GHz
1 kV	7.7 GHz	7.4 GHz
2 kV	8.2 GHz	7.3 GHz
4 kV	0 GHz	7.4 GHz
8 kV	0 GHz	7.3 GHz

TABLE II. GAIN OF PA AFTER HBM ESD ZAPPING

HBM ESD Zapping	Averaged Gain (3.1~10.6 GHz)	
	Unprotected PA	*ESD-Protected PA*
0 V	12.4 dB	9.8 dB
1 kV	8.9 dB	9.3 dB
2 kV	-0.4 dB	9.2 dB
4 kV	-51.8 dB	8.5 dB
8 kV	-55.3 dB	9.5 dB

IV. CONCLUSION

The experimentally measured results have confirmed that the performance of the unprotected PA is seriously degraded after ESD zapping. The PA co-designed with the proposed ESD protection circuit can minimize the negative impact of ESD protection devices on RF circuit performance. The proposed ESD protection strategy by using the waffle-structured SCR, diodes, and the power-rail ESD clamp circuit provides excellent ESD protection capability, which can sustain 8-kV HBM ESD zapping with silicon verification.

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