

ESD PROTECTION DESIGN FOR RF CIRCUITS IN CMOS TECHNOLOGY WITH LOW-C IMPLEMENTATION

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ABSTRACT

To mitigate the radio-frequency (RF) performance degradation caused by electrostatic discharge (ESD) protection device, low capacitance (low-C) design on ESD protection device is a solution. With the smaller layout area and small parasitic capacitance under the same ESD robustness, silicon-controlled rectifier (SCR) device has been used as an effective on-chip ESD protection device in RF ICs. In this paper, the modified lateral SCR (MLSCR) with the waffle layout structure is studied to minimize the parasitic capacitance and the variation of the parasitic capacitance within ultra-wide band (UWB) frequencies. With the minimized parasitic capacitance, the degradation on RF circuit performance can be reduced. Besides, the fast turn-on design on MLSCR without extra parasitic capacitance from the trigger circuit adding on the I/O pad is also investigated in this work.

INTRODUCTION

It has been a trend to integrate the whole radio-frequency (RF) circuits into a single chip. CMOS technology is the leading role to integrate RF circuits. With the scaling-down feature size and lower cost, nanoscale CMOS technology has become suitable to implement RF circuits. However, the thin gate oxide in advanced CMOS processes seriously degrades the reliability of IC products. The major reliability issue for IC products is the damage caused by electrostatic discharge (ESD). Against ESD damages, on-chip ESD protection circuit must be included in IC products. A general concept of on-chip ESD protection for RF ICs is illustrated in Fig. 1 [1]. The ESD protection devices at I/O port and the power-rail ESD clamp circuit must be provided in RF ICs to accomplish the whole-chip ESD protection. However, the parasitic capacitance (C_{ESD}) of ESD protection device inevitably contributes capacitive loading to the I/O port, which disturbs the high frequency signals, induces RC delay on the signal path, and causes degradation on the RF circuit performance [2]. To mitigate the RF performance degradation caused by ESD protection device, low capacitance (low-C) design on ESD protection device to reduce the parasitic capacitance is a solution [3].

Silicon-controlled rectifier (SCR) device has been reported as the useful RF ESD protection element [4]. Because SCR device has much higher ESD robustness

within smaller device size [5], using SCR device as the ESD protection device introduces less parasitic capacitance. The lateral SCR (LSCR) device has been used as the conventional ESD protection device in CMOS technology; however, LSCR has a higher turn-on voltage which is generally greater than the gate-oxide breakdown voltage of the input stages. In order to reduce the turn-on voltage of LSCR to provide more effective ESD protection for the internal circuits, the modified lateral SCR (MLSCR) device has been reported [5].

The different layout structures of MLSCR device to minimize its parasitic capacitance have been studied [6]. The parasitic capacitance within ultra-wide band (UWB, 3.1~10.6 GHz) frequency band and ESD robustness of MLSCR under different layout structures are discussed in this work. To further improve the turn-on efficiency of MLSCR, the fast turn-on design on MLSCR without extra parasitic capacitance from the trigger circuit adding on the I/O port is also investigated. With the low-C and fast turn-on MLSCR, ESD protection design for RF circuits in CMOS technology can be accomplished.

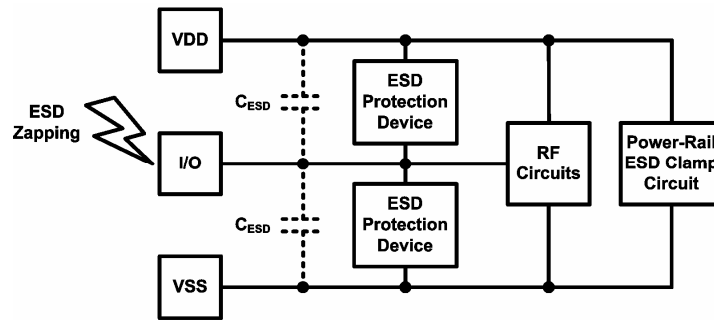


Fig. 1 General concept of on-chip ESD protection for RF ICs.

MLSCR DEVICES FOR RF ESD PROTECTION

Fig. 2 shows the device cross-sectional view of the stripe-structured MLSCR (SMLSCR) and waffle-structured MLSCR (WMLSCR). Both devices are designed with the same size of $60.62 \times 60.62 \mu\text{m}^2$. The MLSCR devices are basically composed of four regions of P+/N-well/P-well/N+. The anode of MLSCR is electrically connected to P+ and N+, which are formed in the N-well. The cathode is electrically connected to N+ and P+, which are formed in the nearby P-well/P-substrate. The trigger P+ diffusion is added across the N-well/P-well junction in the MLSCR to reduce the junction breakdown voltage and the turn-on voltage. When a positive potential is applied between the anode and the cathode, the N-well/P-well junction is reverse-biased, so the MLSCR device is kept off under normal circuit operating conditions. When an ESD stress is zapped to the anode with cathode grounded, the MLSCR device will become highly conductive to quickly discharge ESD current due to the turn-on of latchup path. In the SMLSCR, it discharges ESD current in only two directions, whereas the WMLSCR discharges ESD current in four directions. Thus, the ESD robustness can be improved under the same parasitic capacitance by using the WMLSCR. In other word, the ratio of the parasitic capacitance to ESD robustness can be minimized by realizing the MLSCR with waffle layout structure.

To investigate the relationship between trigger P+ diffusion area and parasitic capacitance, the MLSCR were implemented with different trigger diffusion areas to evaluate the device characteristics and ESD robustness. The trigger diffusion areas of two SMLSCR devices are $123.2 \mu\text{m}^2$ and $242.48 \mu\text{m}^2$, and those of two WMLSCR devices are $140.48 \mu\text{m}^2$ and $264.96 \mu\text{m}^2$, respectively. These devices have been fabricated in a $0.18\text{-}\mu\text{m}$ CMOS process for experimental investigations.

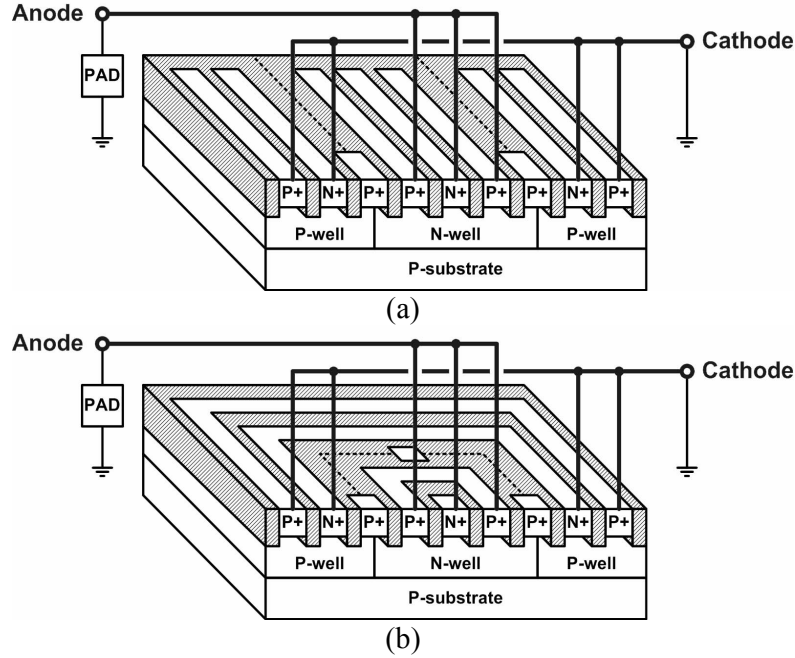


Fig. 2 Device cross-sectional view of (a) stripe-structured MLSCR (SMLSCR) and (b) waffle-structured MLSCR (WMLSCR).

MEASURED DEVICE CHARACTERISTICS

A. Transmission Line Pulsing (TLP) Measurement

The turn-on voltage ($V_{\text{turn-on}}$) and secondary breakdown current (I_{I2}) of the fabricated MLSCR devices are characterized by the TLP system. The TLP-measured I-V curves for all MLSCR are shown in Fig. 3(a), and the extracted device characteristics are listed in Table 1.

B. ESD Robustness

The human-body-model (HBM) ESD robustness of the fabricated MLSCR devices are evaluated by the ESD simulator. All MLSCR devices pass the HBM ESD test (V_{HBM}) of 8-kV, which is the measurement limitation of HBM ESD tester. In order to distinguish the ESD robustness of SMLSCR from WMLSCR, the machine-model (MM) ESD tests are performed. The MM ESD levels (V_{MM}) of all MLSCR devices are within the range of 1.5~1.7 kV, as listed in Table 1. Despite the MM ESD robustness of WMLSCR are slightly worse than those of SMLSCR due to the reduction of N-well area in the waffle layout structure, the parasitic capacitance can be greatly reduced.

C. Parasitic Capacitance

The parasitic capacitance of each MLSCR was obtained from the Y_{11} -parameter which was transformed from the measured two-port S-parameters. To facilitate on-wafer measurement, the MLSCR are arranged with ground-signal-ground (G-S-G) pads. The parasitic effects of the bond pads (PAD in Fig. 2) must be removed to extract the intrinsic device characteristics. The test patterns, one is MLSCR with G-S-G pads and another is the stand-alone G-S-G pads, were fabricated in the same experimental test chip. Then the intrinsic device characteristics can be obtained by subtracting these two measured Y-parameters. Finally, the intrinsic parasitic capacitance (C_{ESD}) of each MLSCR can be extracted. Fig. 3 (b) shows the extracted parasitic capacitance within UWB frequencies of all MLSCR devices.

D. Comparison on Parasitic Capacitance and ESD Robustness

According to the measured results, the ratios of the parasitic capacitance to MM ESD robustness (C_{ESD}/V_{MM}) of WMLSCR have the decrease of about 30% as compared with those of SMLSCR. The variation of the parasitic capacitance within 3.1~10.6 GHz (ΔC_{ESD}) of SMLSCR and WMLSCR are summarized in Table 1.

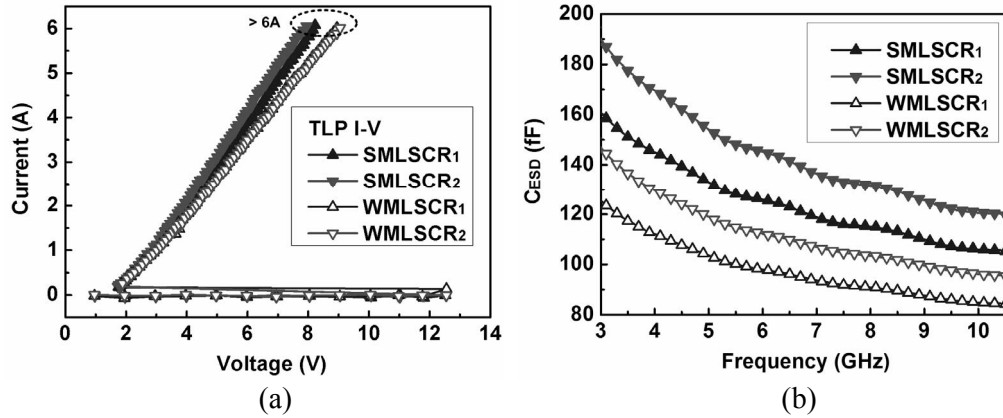


Fig. 3 (a) TLP-measured I-V characteristics and (b) extracted parasitic capacitance within 3.1~10.6 GHz of MLSCR devices under different layout structures.

FAST TURN-ON DESIGN ON MLSCR DEVICES

To further reduce the turn-on voltage of MLSCR, the P+ trigger diffusion can be treated as the trigger port, and the trigger current can be injected to enhance the turn-on efficiency. The equivalent circuit of the P+ triggered MLSCR is shown in Fig. 4 (a). In order to build the trigger circuit to trigger MLSCR without increasing the I/O loading capacitance, the ESD protection strategy with trigger circuit for MLSCR in RF ICs is shown in Fig. 4 (b). Compared this with Fig. 1, the ESD protection devices are composed of a diode from I/O to VDD and a MLSCR from I/O to VSS. The trigger circuit of MLSCR between VDD and VSS is separated from the I/O port and does not add any extra loading effects at the I/O port. Fig. 4 (b) also shows the discharging path under positive-to-VSS mode (PS-mode) ESD zapping, which is the worse case of ESD events. During PS-mode ESD stress, ESD current will first pass through the diode to VDD, and the trigger circuit will trigger MLSCR. The major ESD current will be discharged by MLSCR from the I/O pad to VSS.

To demonstrate the function of the fast turn-on design on MLSCR devices, the experimental setup to measure the TLP I-V characteristics of the triggered SMLSCR and WMLSCR are shown in Fig. 5 (a). The trigger circuit was composed of a 20-pF capacitance and a 20-k Ω resistance. The RC time constant of the trigger circuit is designed in the order of 10^{-6} ~ 10^{-7} s to detect ESD events. Under normal circuit operation, the trigger port of the MLSCR is biased at VSS to keep the device off. When the ESD pulse is zapping, the trigger port is coupled to high potential by the ESD energy. Therefore, the trigger current will be injected into the trigger port by the CR trigger circuit, and the MLSCR will be quickly turned on. The TLP-measured I-V curves for CR-triggered SMLSCR and WMLSCR are shown in Fig. 5 (b). The turn-on voltage of all CR-triggered SMLSCR and WMLSCR ($V_{\text{turn-on}}^*$) are reduced to about 6 V, as listed in Table 1. The 6-V turn-on voltage of CR-triggered MLSCR devices is much lower than the breakdown voltage of the internal circuits in a 0.18- μm CMOS process, so the fast turn-on design is proved to be feasible.

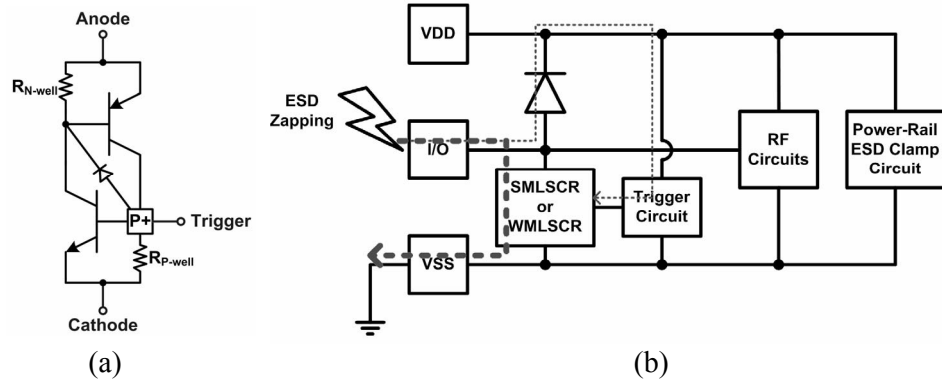


Fig. 4 (a) Equivalent circuit of the P+ triggered MLSCR and (b) ESD protection strategy with trigger circuit for MLSCR in RF ICs.

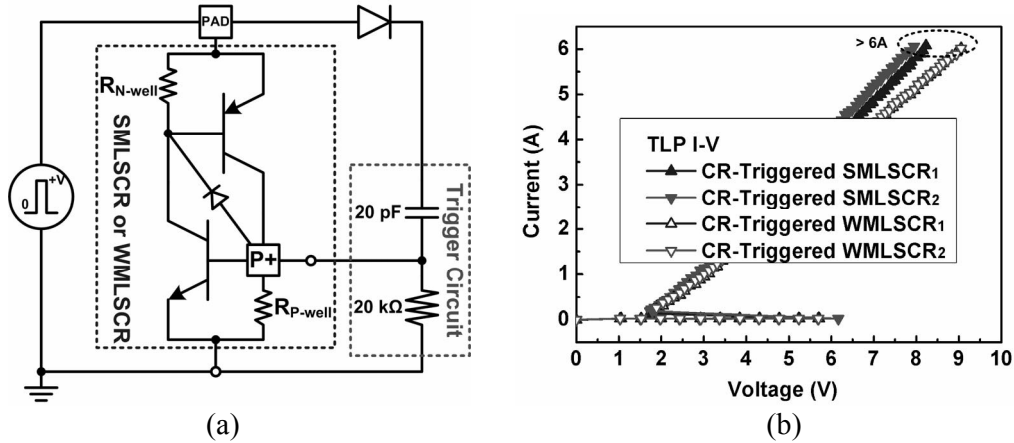


Fig. 5 (a) Measurement setup and (b) TLP-measured I-V characteristics of CR-triggered MLSCR.

CONCLUSION

In this work, SCR devices with the waffle layout structure have been verified to have reduced parasitic capacitance under the same ESD robustness. The ratios of the

parasitic capacitance to MM ESD robustness of WMLSCR have the decreases of about 30% as compared to SMLSCR. WMLSCR are also verified to reduce the variation of the parasitic capacitance within UWB frequencies. Thus, SCR devices realized in the waffle layout structure are more suitable for on-chip ESD protection in RF circuits than those realized in the traditional stripe layout structure. Besides, the fast turn-on design on MLSCR without extra parasitic capacitance from the trigger circuit adding on the I/O port is also studied to more effectively protect the RF circuits.

Table 1 Comparisons on measured device characteristics of MLSCR under different structures

Type	Symbol	Trigger Diffusion Area (μm^2)	$V_{\text{turn-on}}$ (V)	$V_{\text{turn-on}}^*$ (V)	I_{t2} (A)	V_{HBM} (kV)	V_{MM} (kV)	ΔC_{ESD} Within 3.1~10.6GHz (fF)
Stripe	SMLSCR ₁	123.2	12.52	5.71	> 6	> 8	1.63	53.41
Stripe	SMLSCR ₂	242.48	12.54	6.16	> 6	> 8	1.68	67.47
Waffle	WMLSCR ₁	140.48	11.81	5.69	> 6	> 8	1.59	39.36
Waffle	WMLSCR ₂	264.96	12.55	5.70	> 6	> 8	1.56	49.13

* Turn-on voltage of CR-triggered SMLSCR and WMLSCR.

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