P-61: Temperature Coefficient of Diode-Connected LTPS Poly-Si TFTs and its Application on the Bandgap Reference Circuit

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Abstract

The temperature coefficient (TC) of n-type diode-connected polycrystalline silicon thin-film transistors (poly-Si TFTs) is investigated. The relationship between TC and the activation energy is observed and explained. It is also found that TC is not sensitive to the deviation of the laser crystallization energy. On the contrary, channel width can effectively modulate TC. By using the diode-connected poly-Si TFTs with different channel widths, a new bandgap reference circuit for precise analog circuit design on glass substrate is proposed and realized. From the experimental results in a LTPS process, the output voltage reference exhibits a very low TC of 195 ppm/℃, between 25℃ and 125℃.

1. Introduction

Polycrystalline silicon thin-film transistors (Poly-Si TFTs) have been widely investigated for active-matrix liquid-crystal displays (AMLCDs) and their peripheral driving circuitry due to the increased carrier mobility [1,2]. However, even with the advanced crystallization technologies such as the excimer laser annealing (ELA) or the sequential laser solidification (SLS) process, it is still observed that the carrier transport in poly-Si TFTs is dominated by the thermionic emission effect [3,4]. The energy barriers at grain boundaries confine the carrier movement, reduce the field-effect mobility, and make the device characteristics to be strongly dependent on temperature. As a result, to reduce the impact of temperature variation on the performance of analog circuits in the low-temperature polycrystalline silicon (LTPS) process is a very important design challenge. In CMOS technology, the bandgap reference (BGR) circuit is the major design to provide a stable voltage reference with low sensitivity to temperature and supply voltage [5-8]. The key idea is to use the temperature-dependent voltage drop across the diode-connected BJTs or across the diodes to modulate and stabilize the output voltage. The BGR circuit has been widely used in analog and digital circuits, such as DRAM, flash memory, analog-to-digital converter (ADC), and so on.

Though the BGR circuit is important to provide a stable output voltage, the LTPS BGR circuit on glass substrate was never reported in the past. The conventional CMOS BGR circuit incorporated with BJTs or p-n junction diodes is a great challenge for LTPS process since the characteristics of the poly-Si BJTs or the poly-Si p-n junction diodes are still unknown or lack of reliable control. On the contrary, the characteristics of LTPS TFTs are strongly dependent on temperature even when the devices are operated in saturation region [3,4]. Therefore, the LTPS BGR circuit can be realized by using only LTPS TFT devices.

In this paper, the temperature coefficient (TC) of diode-connected LTPS TFT devices is first analyzed. The relationship between the activation energy and the TC is investigated. Then, the influences from the laser energy density of the ELA process on the TC of diode-connected devices are discussed. Followed by the investigation of the channel width effect on the TC, a combination of a narrow-width device and a wide-width device is proposed to generate a positive TC by an appropriate circuit arrangement. The positive TC can be used to compensate the negative TC of devices to achieve the design of a stable output voltage with low sensitivity to the temperature. Finally, this concept has been demonstrated on a new LTPS BGR circuit. The output voltage reference is found to exhibit a low temperature coefficient of 195 ppm/°C, which is 85% much lower than that of the conventional diode-connected TFTs.

2. Device Fabrication

For device analysis, the typical top-gate, coplanar self-aligned n-type poly-Si TFTs with 1.25-μm-length LDD structure were used in this study. First, the buffer layer was deposited on the glass substrate. Then, the undoped 50-nm-thick a-Si layer was deposited and crystallized by XeCl excimer laser with a laser energy density varied from 340 mJ/ cm^2 to 420 mJ/ cm^2. The recrystallized poly-Si films were patterned into the active islands. Afterward, the 60-nm-thick oxide layer was deposited as the gate insulator. Then, the 200-nm-thick Molybdenum was deposited and patterned as the gate electrode. The n^- doping was performed self-aligned to the gate electrode. The n^+ source/drain region was defined by an additional mask. The dopants were activated by thermal process. After the deposition of nitride passivation and the formation of contact holes, the 550-nm-thick Titanium/Aluminum/Titanium tri-layer metal was deposited and patterned to be the metal pads. The channel length of the devices keeps as 6 μm while the channel width changes from 30 μm to 6 μm. For the BGR circuit verification, the devices (L = 6 μm) fabricated by the 3-μm LTPS process are used.

 ISSN/008-0966X/08/3903-1410-$1.00

3. Measured Results and Temperature Model

Since the temperature response of the LTPS devices is mostly influenced by the thermionic emission effect with an activation energy associated with the grain boundary barrier height, the relationship between the activation energy and the temperature coefficient is first investigated. As shown in Fig. 1, the activation energy (E_a) extracted from the Arrhenius plot of the drain current is depicted as a function of the gate bias (V_{GS}). The drain bias (V_{DS}) is equal to V_{GS} for the diode-connected devices. Devices with three different channel widths are measured. It is found that, similar to the three-terminal LTPS devices, E_a of the diode-connected devices is strongly dependent on V_{GS}. Under small gate bias, E_a is high. When V_{GS} is increased, E_a decreases drastically.

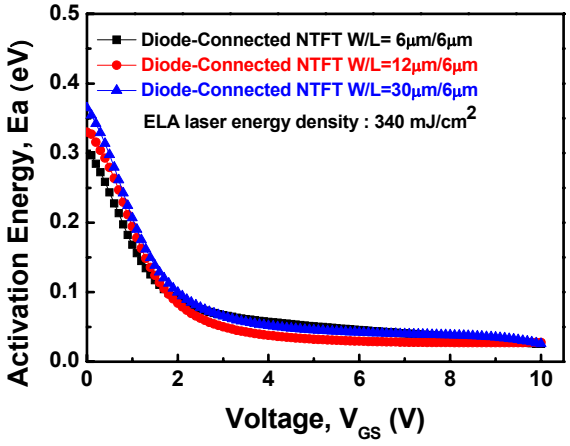


Figure 1. The activation energy as a function of V_{GS} for diode-connected NTFTs with W/L as 6μm/6μm, 12μm/6μm, and 30μm/6μm .

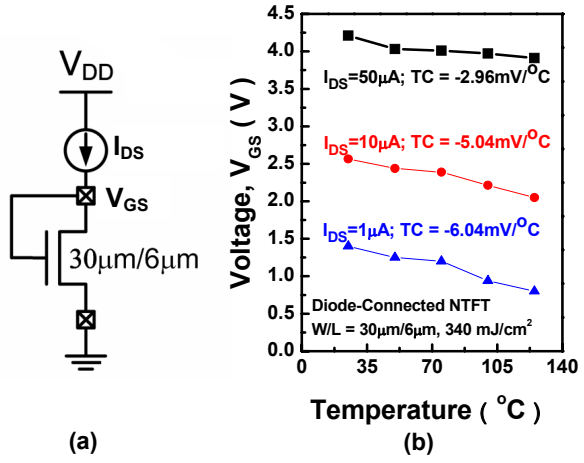


Figure 2. (a) The setup to measure V_{GS} under the bias of I_{DS}. (b) The relationship between V_{GS} and temperature under three different current levels (1 μA, 10 μA, and 50 μA).

Then, to extract the temperature coefficient, V_{GS} of the fabricated devices under the bias of three different current levels (1 μA, 10 μA, and 50 μA) are measured at different temperatures as shown in Fig. 2(a). The measured V_{GS} of the device with channel width of 30 μm is plotted as a function of temperature in Fig. 2(b). When temperature increases, V_{GS} is decreased. Linear relationship between V_{GS} and temperature can be observed in Fig. 2(b), the slope represents the temperature coefficient (TC). Obviously, the TC is negative. Additionally, the magnitude of TC decreases with increased bias current. When the bias current increases from 1 μA, 10 μA, to 50 μA, the TC varies from -6.04 mV/°C, -5.04 mV/°C, to -2.96 mV/°C. It is noted that for one identical diode-connect device, the increase of bias current gives rise to the increase of operation voltage. As a result, the larger bias current makes the devices operated under larger V_{GS} with smaller E_a and smaller magnitude of TC. This result clearly demonstrates the relationship between the activation energy and the TC. The above discussion can be expressed by the following derivation.

For LTPS TFTs, the drain current I_D of devices operated in saturation region can be expressed as

$$I_{DS} = \frac{W}{2L}\mu_0 C_{ox}(V_{GS} - V_{TH})^2 \exp(-\frac{V_B}{V_T}), \quad (1)$$

where μ_0 is the carrier mobility within the grain, L denotes the effective channel length, W is the effective channel width, C_{ox} is the gate oxide capacitance per unit area, V_{TH} is the threshold voltage of TFT devices, and V_{GS} is the gate-to-source voltage of TFT devices. V_B is the potential barrier at grain boundaries and is associated with the crystallization quality of the poly-Si film. When we extract the activation energy from the Arrhenius plot of the drain current, E_a is equal to qV_B. Under small V_{GS}, V_B is large. When the V_{GS} increases, V_B decreases rapidly. When the devices in circuit are operated under small V_{GS}, it is found that the drain current I_D of devices is dominated by the exponential term and can be simplified by

$$I_{DS} = W\alpha \exp(-\frac{V_B}{V_T}), \quad (2)$$

where α is only weakly dependent on V_{GS} and is insensitive to temperature. Then, the following equations can be derived:

$$V_B = V_T \ln(\frac{W\alpha}{I_{DS}}) = \frac{kT}{q}\ln(\frac{W\alpha}{I_{DS}}). \quad (3)$$

When there is a variation of temperature ΔT, the variation of V_B is

$$\Delta V_B = \frac{k\Delta T}{q}\ln(\frac{W\alpha}{I_{DS}}) . \quad (4)$$

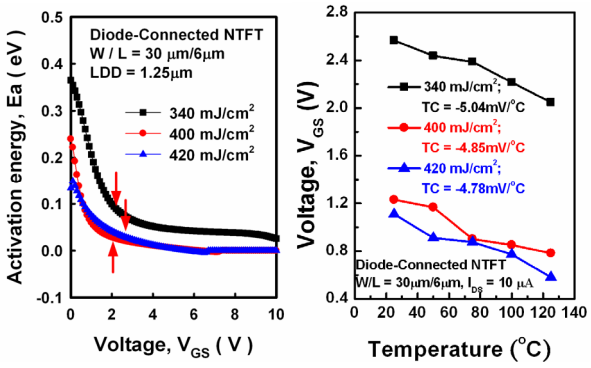
As shown in Fig. 1, the variation of V_B is related to the variation of V_{GS}. Assume that the variation of V_{GS} (ΔV_{GS}) is very small that an negative linearity approximation can be given between ΔV_B and ΔV_{GS} as

$$\Delta V_{GS} = -\frac{1}{m}\Delta V_B = -\frac{k\Delta T}{mq}\ln(\frac{W\alpha}{I_{DS}}), \quad (5)$$

where m is the absolute value of the slope of the linear approximation between ΔV_B and ΔV_{GS}. Finally, the temperature coefficient (TC) can be found as

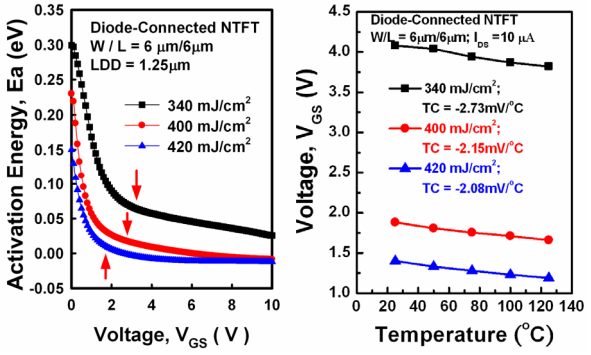
$$TC = \frac{\Delta V_{GS}}{\Delta T} = -\frac{k}{mq}\ln(\frac{W\alpha}{I_{DS}}) = -\frac{\Delta V_B}{m\Delta T}. \quad (6)$$

Even though the increase of V_B accompany with the increase of m, the variation of V_B can be more significant than that of m under a proper design.



(a) (b)

Figure 3. (a) The activation energy as a function of V_{GS} for diode-connected NTFTs with poly-Si film crystallized by laser energy density as 340 mJ/cm^2, 400 mJ/cm^2, and 420 mJ/cm^2. (b) The relationship between V_{GS} and temperature under identical I_{DS} of 10 μA for three devices in (a). Devices have the same W/L of 30μm/6μm.



(a) (b)

Figure 4. (a) The activation energy as a function of V_{GS} for diode-connected NTFTs with poly-Si film crystallized by laser energy density as 340 mJ/cm^2, 400 mJ/cm^2, and 420 mJ/cm^2. (b) The relationship between V_{GS} and temperature under identical I_{DS} as 10 μA for three devices in (a). Devices have the same W/L of 6μm/6μm.

The activation energy, as well as the grain boundary barrier, should be related to the grain structure and the grain boundary property. It is therefore presumed that the laser energy density of the ELA process influences the grain structure and affects the TC of the devices. Figure 3(a) compared the activation energies of the diode-connected devices with the poly-Si film crystallized under different laser energies (340, 400, and 420 mJ/cm^2). The channel width of the devices is studied in Fig.3(a) is 30 μm. The activation energy is found to be reduced with increasing laser energy density. As a result, the TC of the devices with higher laser energy density is also smaller than those with lower laser energy density as shown in Fig. 3(b). However, the influence of laser energy density on the TC is not significant. When the laser energy density changes ±10%, the TC changes only about ±2.75%. The reason can be explained by identifying the biasing points of three devices in Fig. 3(a). The operation voltages of three devices under the bias of 10-μA I_{DS} are indicated by the arrow symbols in Fig. 3(a). It is found that the activation energies of the three biasing points are similar. This makes the TC insensitive to the deviation of the laser energy density in the ELA process. Similar results can be also observed for the devices with small channel width of 6 μm in Fig. 4(a) and Fig. 4(b).

The influence of the channel width on the TC, however, is found to be significant. When the diode-connected devices are biased under a constant current of 10 μA, V_{GS} of devices with channel widths of 6 μm and 30 μm are plotted as a function of temperature in Fig. 5. Obviously, the wide-channel-width devices exhibit more negative TC than the narrow-channel-width devices. From Fig. 1, it has been observed that the channel width has little influence on the device activation energy. However, when all the devices are biased by identical current source, the wide-channel-width devices are operated under small V_{GS} and the narrow-channel-width devices are operated under large V_{GS}. When V_{GS} is reduced, the activation energy is drastically enlarged as shown in Fig. 1. As a result, the absolute value of the TC is significantly enlarged by increasing the channel width. Such a phenomenon can also be explained by Eq. (6).

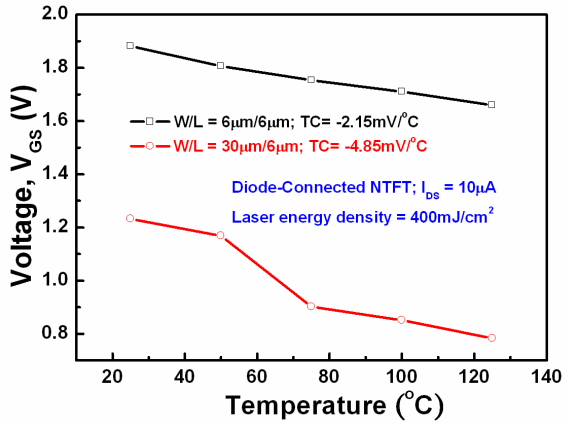


Figure 5. The relationship between V_{GS} and temperature under identical I_{DS} of 10 μA. Devices with different channel widths are compared.

4. Application

The difference of TCs between the wide-channel-width device and the narrow-channel-width device can be very useful if an appropriate design is proposed to extract the V_{GS} of the wide-channel-width device from the V_{GS} of the narrow-channel-width device. This positive TC can be used to compensate the negative TC from the V_{GS}. The following proposed BGR circuit is a demonstration of this concept. The new proposed bandgap reference circuit fabricated by a 3-μm LTPS technology is shown in Fig. 6(a). In this circuit, the output voltage reference (V_{REF}) is the sum of a gate-source voltage of the n-type diode-connected TFT (V_{GS8}) and the voltage drop across the resistor R_2 (V_{R2}). If M6 is a wide-channel-width TFT and M7 is a narrow-channel-width TFT, the voltage drop across the resistor R_1 (V_{R1}) is proportional to the absolute temperature (PTAT). Also, V_{R2} is proportional to V_{R1} by a ratio of (R_2/R_1), which is used to compensate the negative temperature coefficient of V_{GS8}. Fig. 6(b) shows the measured results of the BGR circuit. The measured temperature coefficient of the new proposed bandgap reference circuit is around 195 ppm/°C under the supply voltage of 10 V. The variation of V_{REF} and V_{GS8} from 25°C to 125°C are compared

in Fig. 6(b). The proposed BGR circuit successfully provides a stable voltage reference with very low sensitivity to temperature.

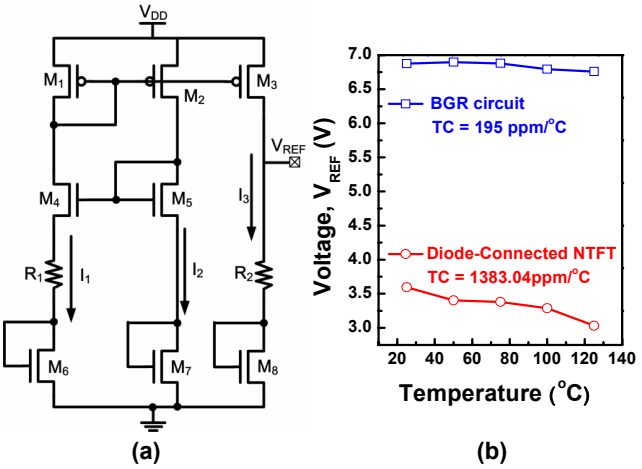


Figure 6. (a) The new proposed bandgap reference circuit in LTPS process. (b) The measured result of the reference output voltage of the new proposed bandgap reference circuit. The voltage across the diode-connected NTFT (V_{GS8}) as a function of temperature is also plotted for comparison.

Finally, the TCs of the n-type diode-connected devices biased under a 10-μA current are plotted in Fig. 7. It can be concluded that the influence of ELA laser energy density or the poly-Si thin film property on the TC is relatively small. This makes the LTPS BGR circuit not sensitive to the deviation of the laser annealing process. On the contrary, changing the device channel width can effectively change the TC of the diode-connected device. This enables the circuit designer easily modulate the TC of the diode-connected devices.

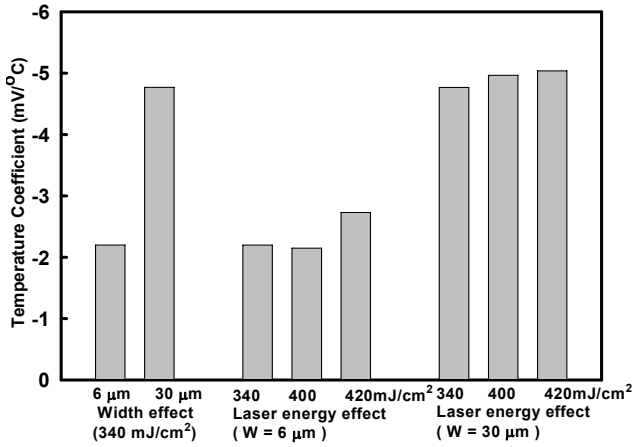


Figure 7. The TCs of the n-type diode-connected devices biased under a 10-μA current.

5. CONCLUSION

In this study, it has been found that the temperature coefficient of LTPS TFTs is strongly dependent on the activation energy of the devices. With a suitable control, higher activation energy gives rise to higher absolute value of the temperature coefficient. The influence of the laser energy density in ELA process on the temperature of the devices is not significant. On the other hand, the bias current level and the channel width have a strong impact on the device temperature coefficient. As a result, the temperature coefficient of devices can be controlled by designing the channel width of the devices. With an appropriate circuit design, a positive temperature coefficient can be generated by using the voltage drop between devices those have different temperature coefficients. Then, the positive temperature coefficient can be used to compensate the negative temperature coefficient from the devices.

A new bandgap reference circuit has been successfully verified in a 3-μm LTPS process. The measured reference output voltage is 6.87 V with a temperature coefficient of 195 ppm/°C. The proposed bandgap reference circuit consumes a maximum current of only 8.97 μA under the supply voltage of 10 V. This new temperature-compensated voltage reference generator can be used to realize precise analog circuits in LTPS process for System-on-Glass (SoG) applications.

6. Acknowledgment

The authors would like to thank for the project (NSC96-2221-E-009-127-MY2) support from the National Science Council, the AU Optronics Corporation, Taiwan, and the project (MOEA-96-EC-17A-O7-S1-046) from the Ministry of Economic Affairs, Taiwan.

7. References

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