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# The Impact of BIGFET Clamp Device Layout on ESD Protection Circuit Robustness

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# Author's Biography

- **Chih-Ting Yeh was born in Hsinchu, Taiwan, R.O.C., in 1982. He received the B.S. degree in electrophysics and the M.S. in electronics engineering, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 2004 and 2006, respectively.**

- **In 2007, he joined Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan, R.O.C. as a Design Engineer. His main research includes the I/O interface circuit design and ESD application for RF.**

# Abstract

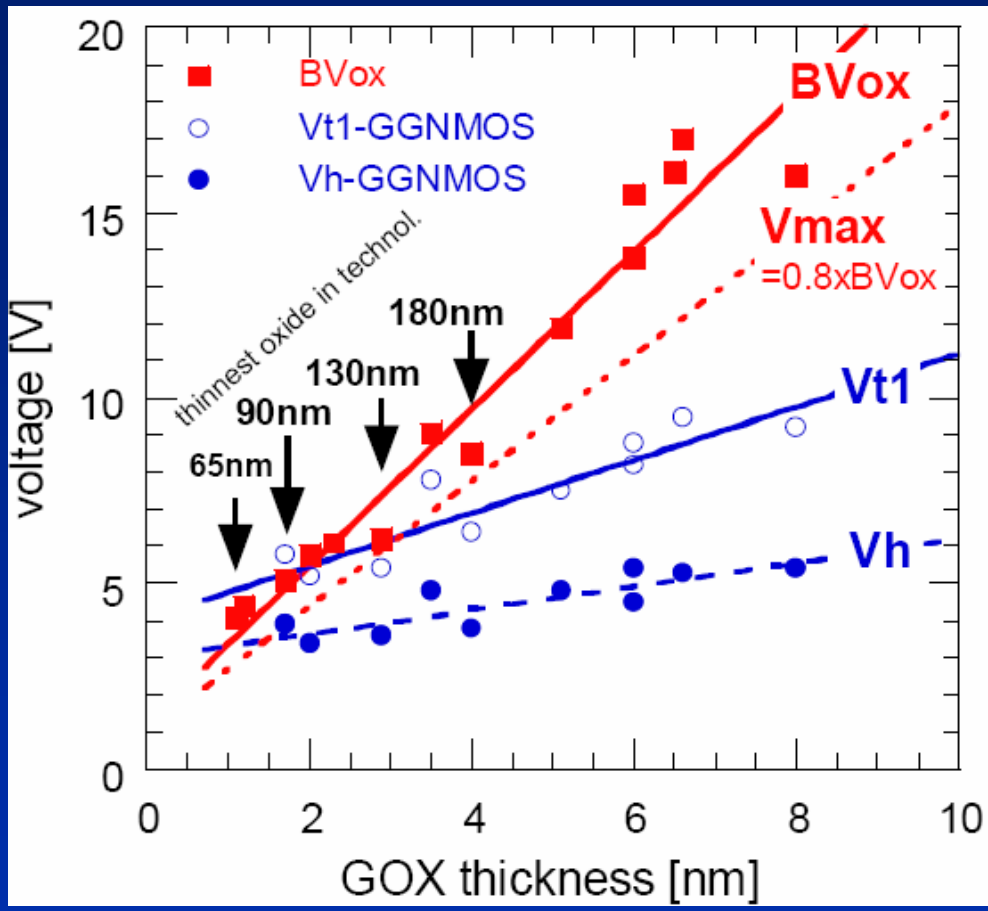

- In CMOS ICs, it is a challenging topic to effectively improve ESD robustness with limited layout area.
- In this paper, the power-rail ESD clamp circuit with BIGFET clamp device has been designed and fabricated in a 0.13-㎛m CMOS technology to investigate the impacts of some circuit and layout parameters on its ESD robustness.
- The measured results reveal that there is an optimized RC time constant to get better ESD robustness from the power-rail ESD clamp circuit.

# Outline

- Introduction
- Design Concern
  - RC Time Constant
  - Device Layout of BIGFET
  - Simulation
- Results and Discussion
  - Turn-on Verification
  - TLP I-V Measurement
  - ESD Robustness
- Conclusion

# Technology Road Map

- Rapid decay of the gate oxide breakdown voltage $BV_{ox}$.
- The ESD design window of input gate oxide protection is dramatically narrowing down.

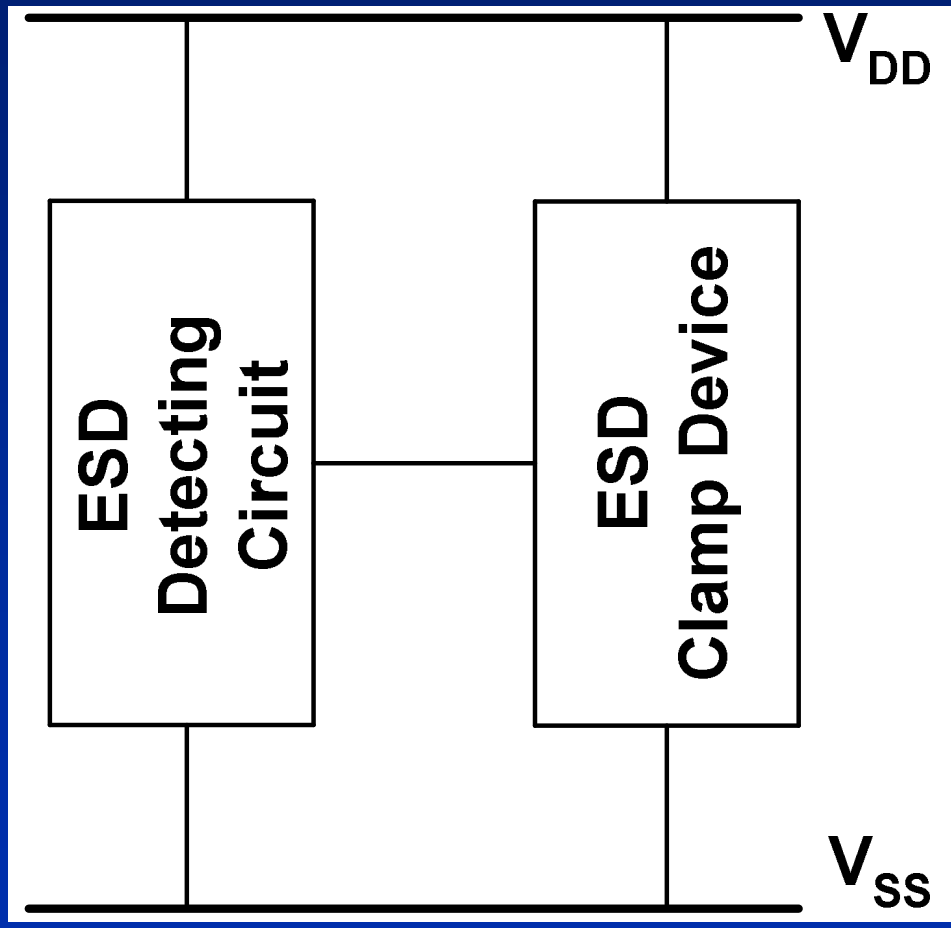



Ref.: M. Mergens, et al., "ESD protection circuit design for ultra-sensitive IO application in advanced sub-90nm CMOS technologies," in *Proc. of ISCAS*, 2005, pp. 1194-1197.

# Power-Rail ESD Clamp Circuit

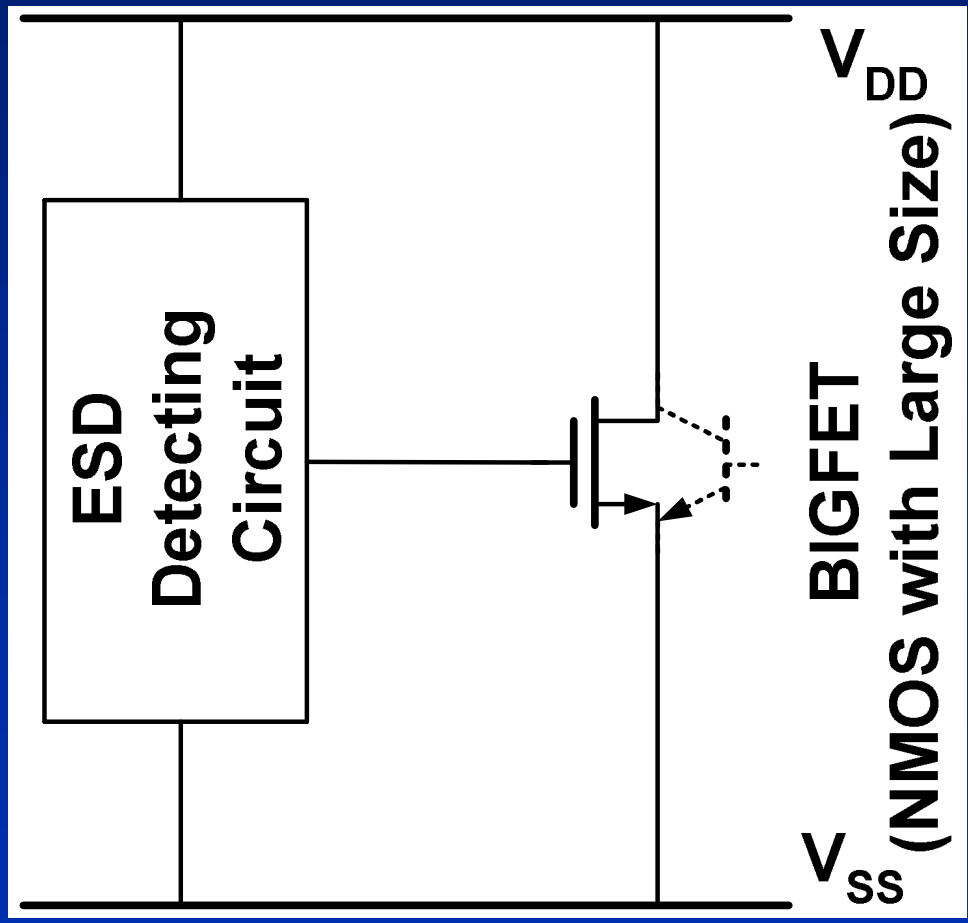
- ESD detecting circuit can distinguish the difference of the raising edges between power-on and ESD-stress conditions.

- ESD clamp device is designed to conduct huge ESD current during ESD events.



# ESD Clamp Device

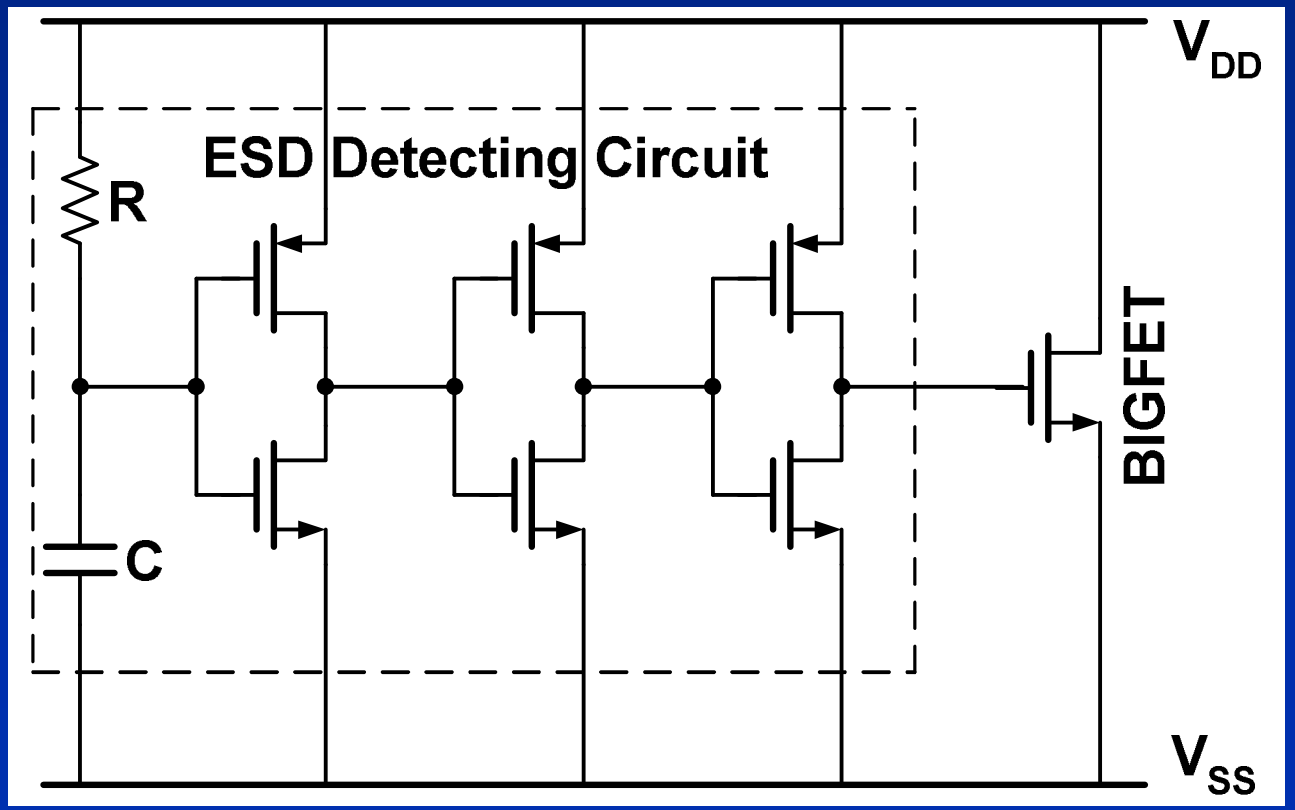
- In this work, the ESD clamp device was implemented by a NMOS transistor with a large channel width, also called as BIGFET.




- Such device has two conduction paths:
  - ü surface channel of NMOS
  - ü parasitic npn BJT in NMOS

# ESD Detecting Circuit

- ESD detecting circuit is composed of RC and inverter string.
- The sizes of the inverter string were gradually increased.



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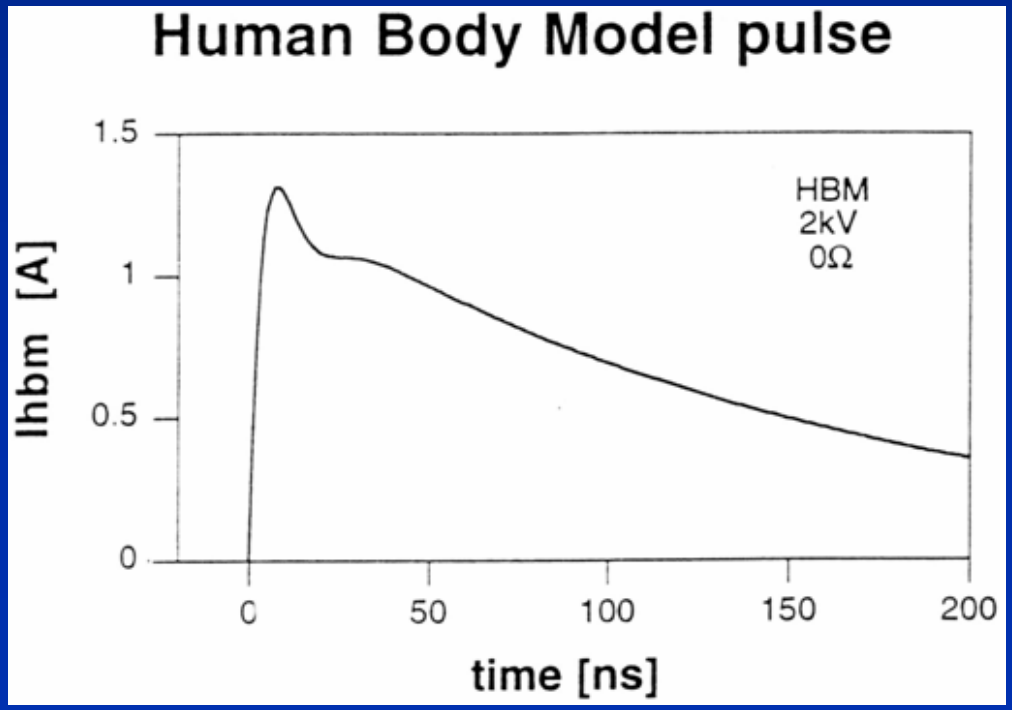
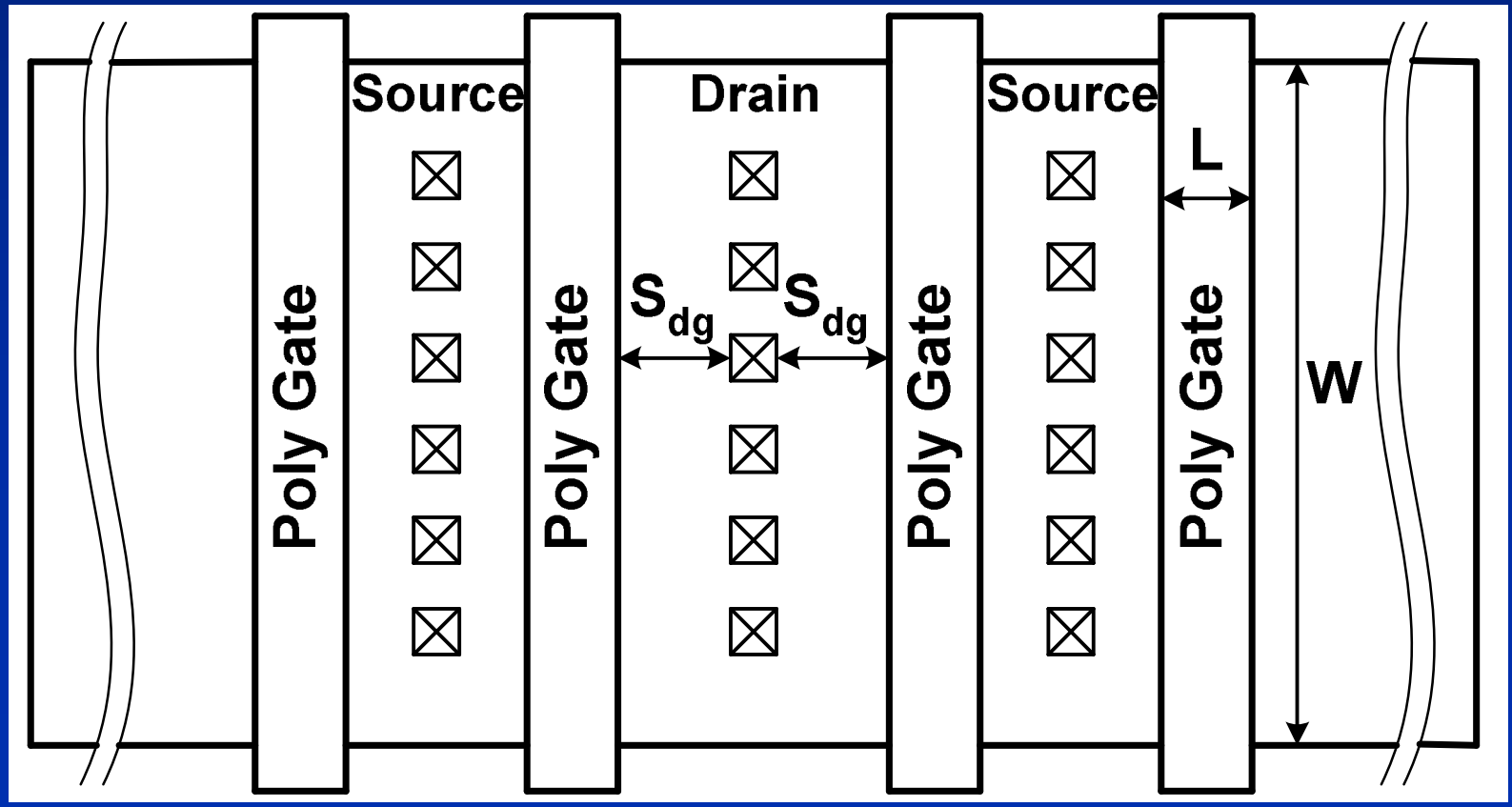
# RC Time Constant

- HBM pulse width is about 100 ns (half-energy period).
- RC time constant was designed at 0.1~1 ㎳.
- RC time constants of 0.1 ㎳, 0.5 ㎳, and 1.0 ㎳ are investigated in this work.

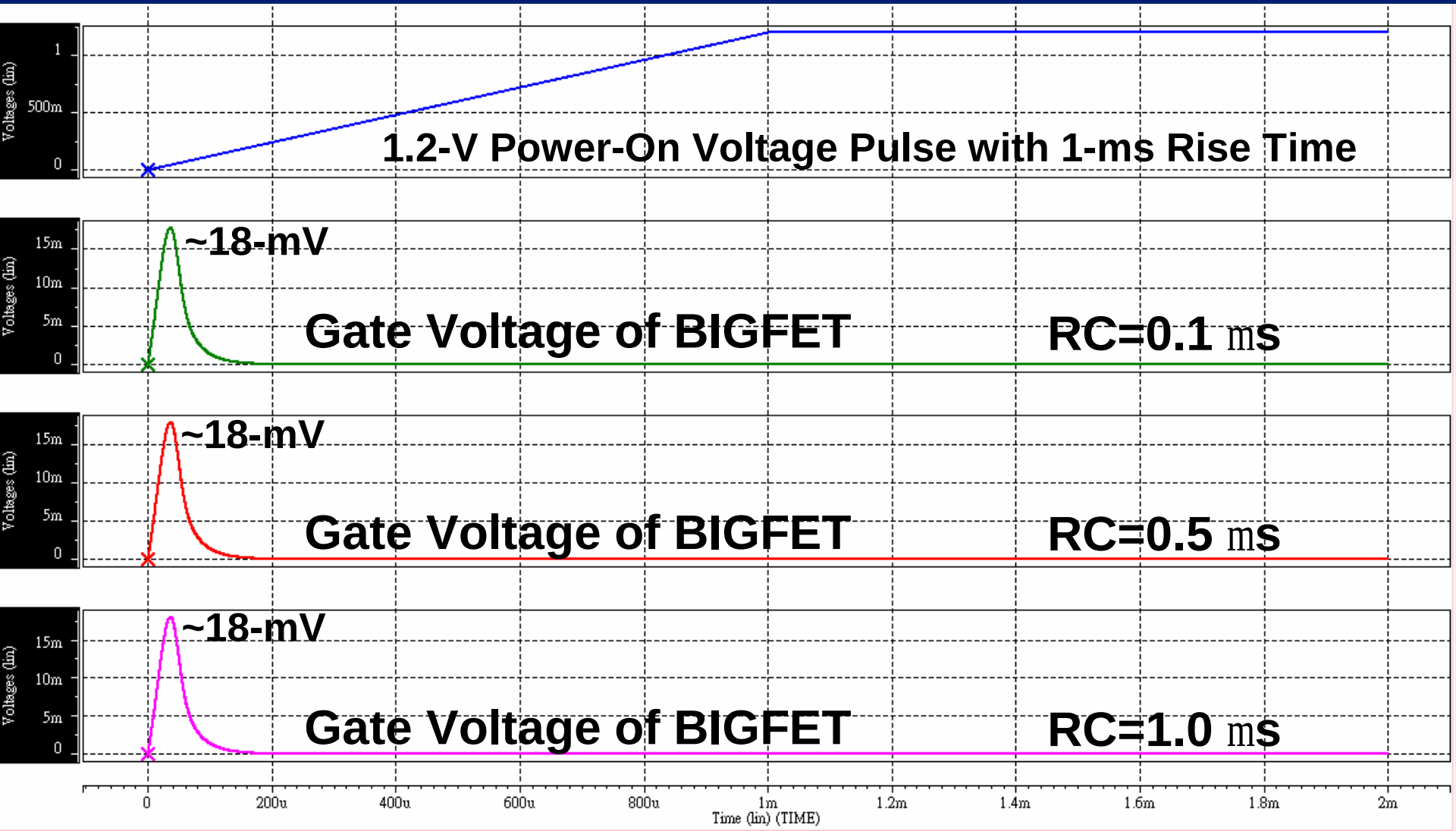


# Device Layout of BIGFET

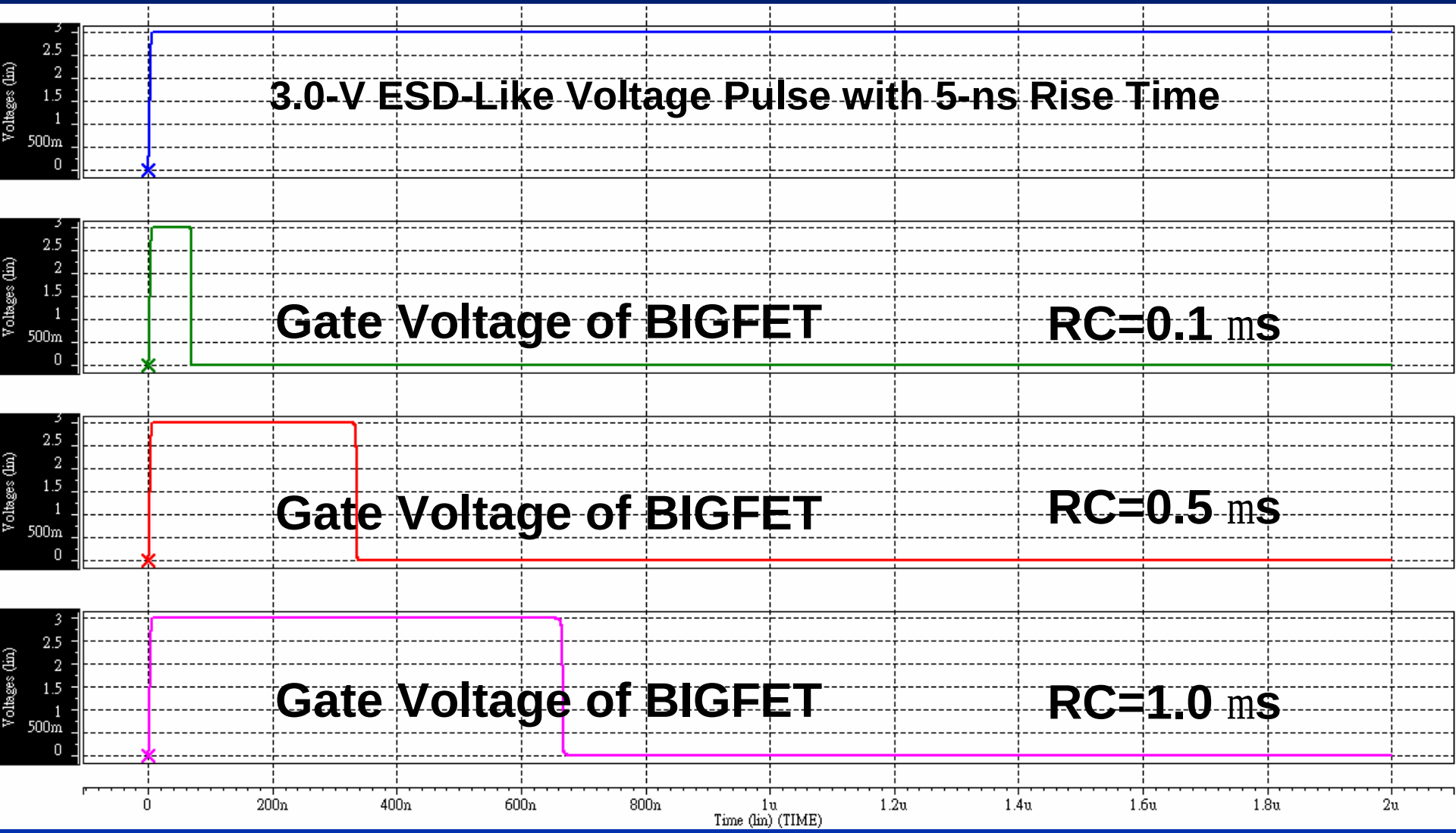
- L= 0.18 μm, $W_{total}$= 2000 μm.
- $S_{dg}$ is split as 0.22 μm, 0.33 μm, and 0.44 μm in the test chip fabricated in a 0.13-μm CMOS Process.



# Simulation (1/2)



# Simulation (2/2)



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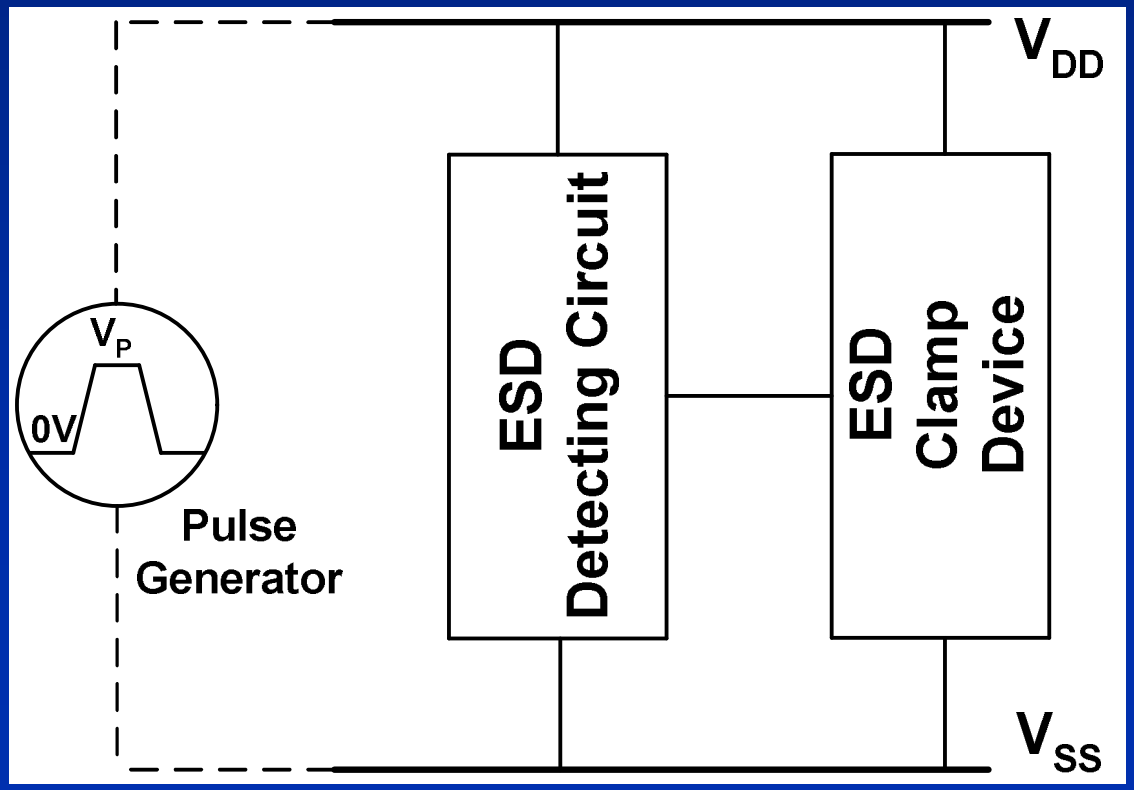
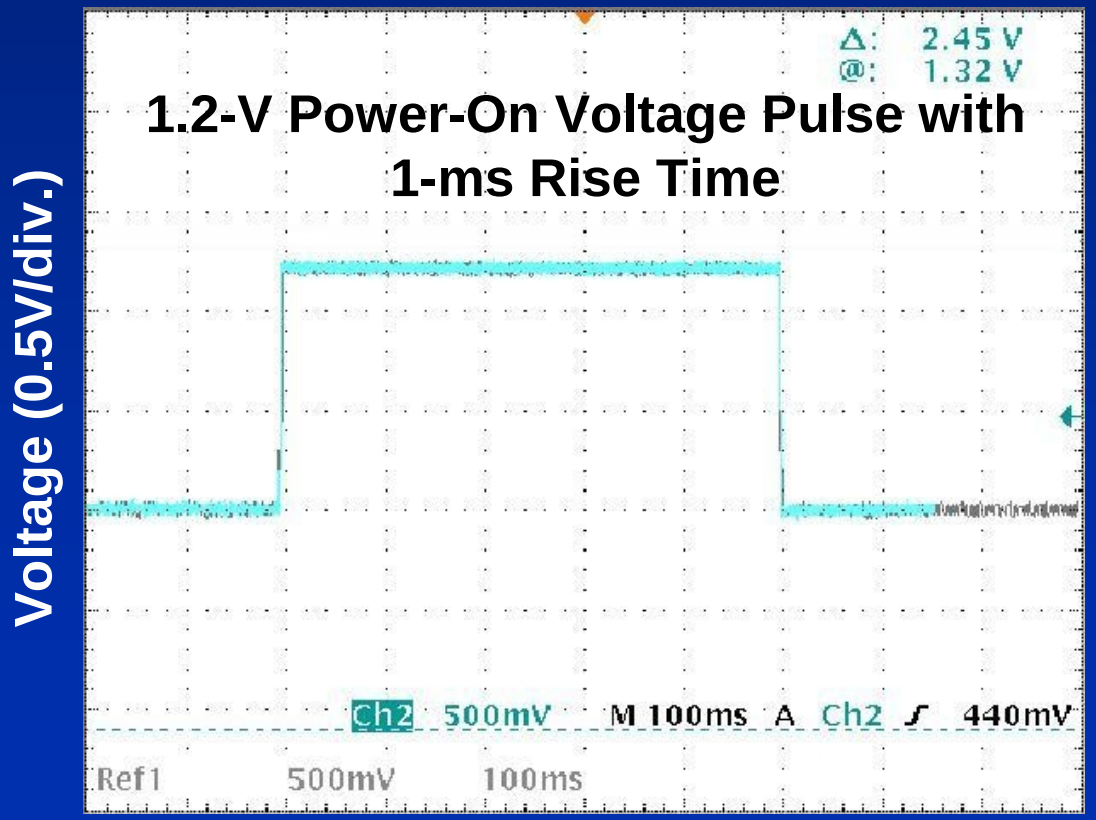
# Measurement Setup for Turn-On Verification

- Power-on : a 1.2-V ramp voltage with rise time (tr) of 1 ms.
- ESD-like Event : a 3.0-V voltage pulse with tr= 5 ns.



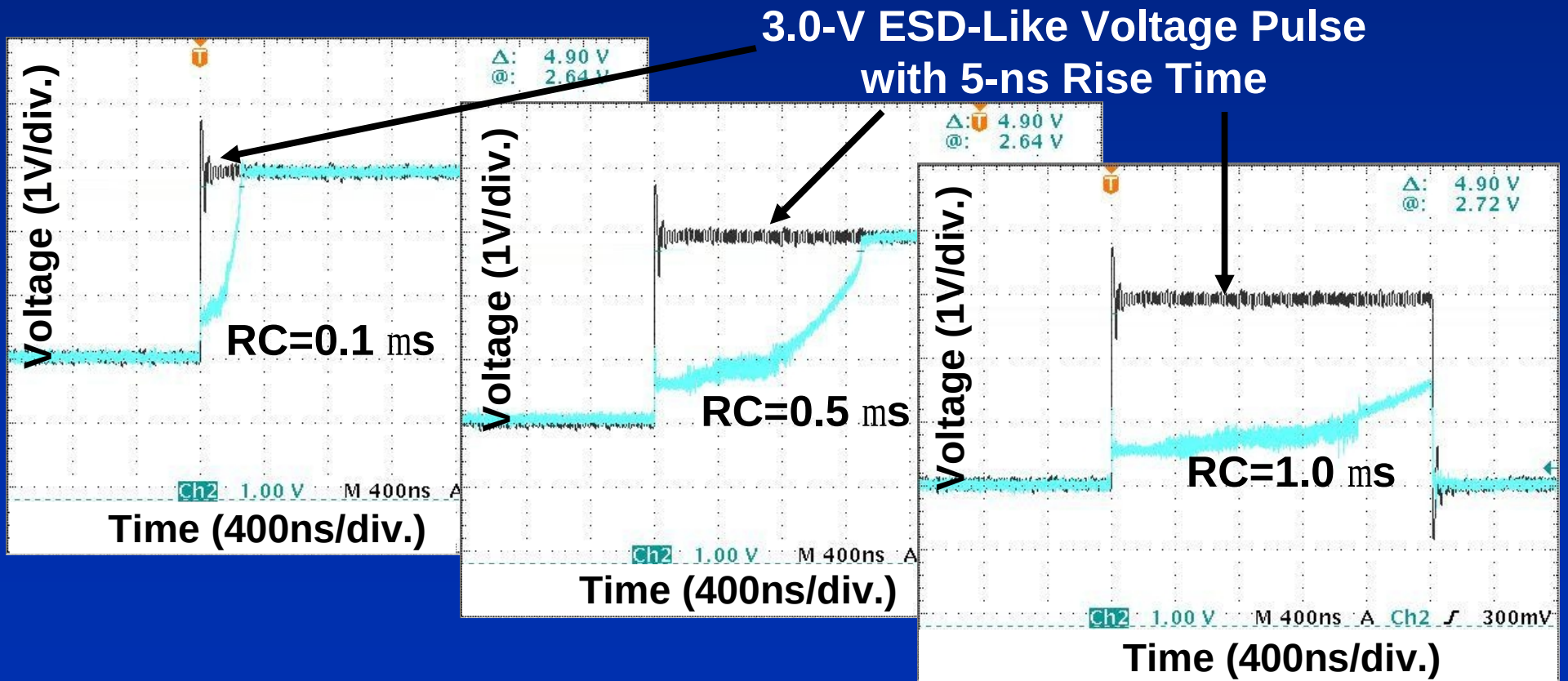
# Measured Results of Turn-On Verification (1/2)

- During normal power-on operation, the voltage waveform across the ESD clamp circuit follows the power-on waveform generated from power supply.



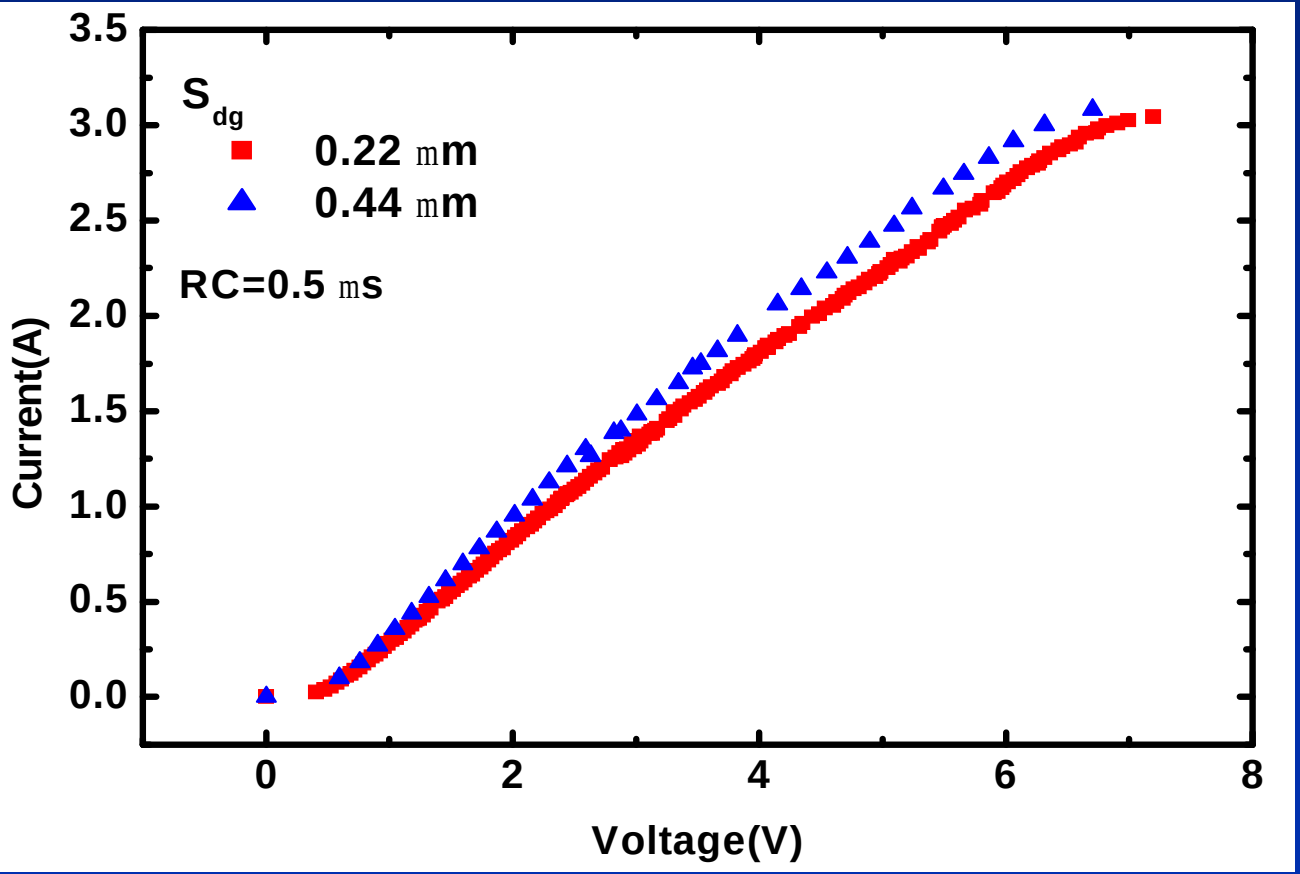
# Measured Results of Turn-On Verification (2/2)

- For ESD-like event, ESD clamp circuit can clamp the overstress voltage pulse and the turn-on duration is longer when ESD detecting circuit is designed with larger RC time constant.



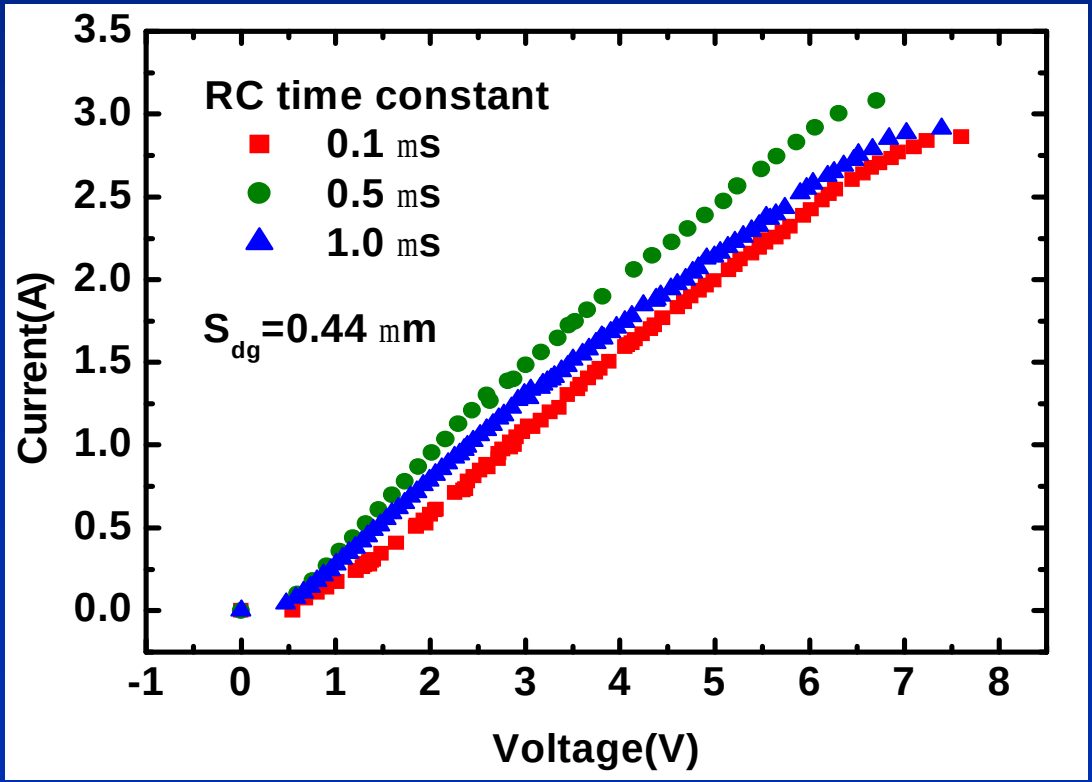
# TLP Measured Results (1/2)

- The BIGFET drawn with a large $S_{dg}$ performs a lower turn-on resistance.



# TLP Measured Results (2/2)

- For a given $S_{dg}$= 0.44 μm, there is an optimized result in the testkeys among three kinds of time constants.
- When RC= 0.5 μs, the turn-on resistance of clamp circuit is the lowest one and It2 is the highest one.

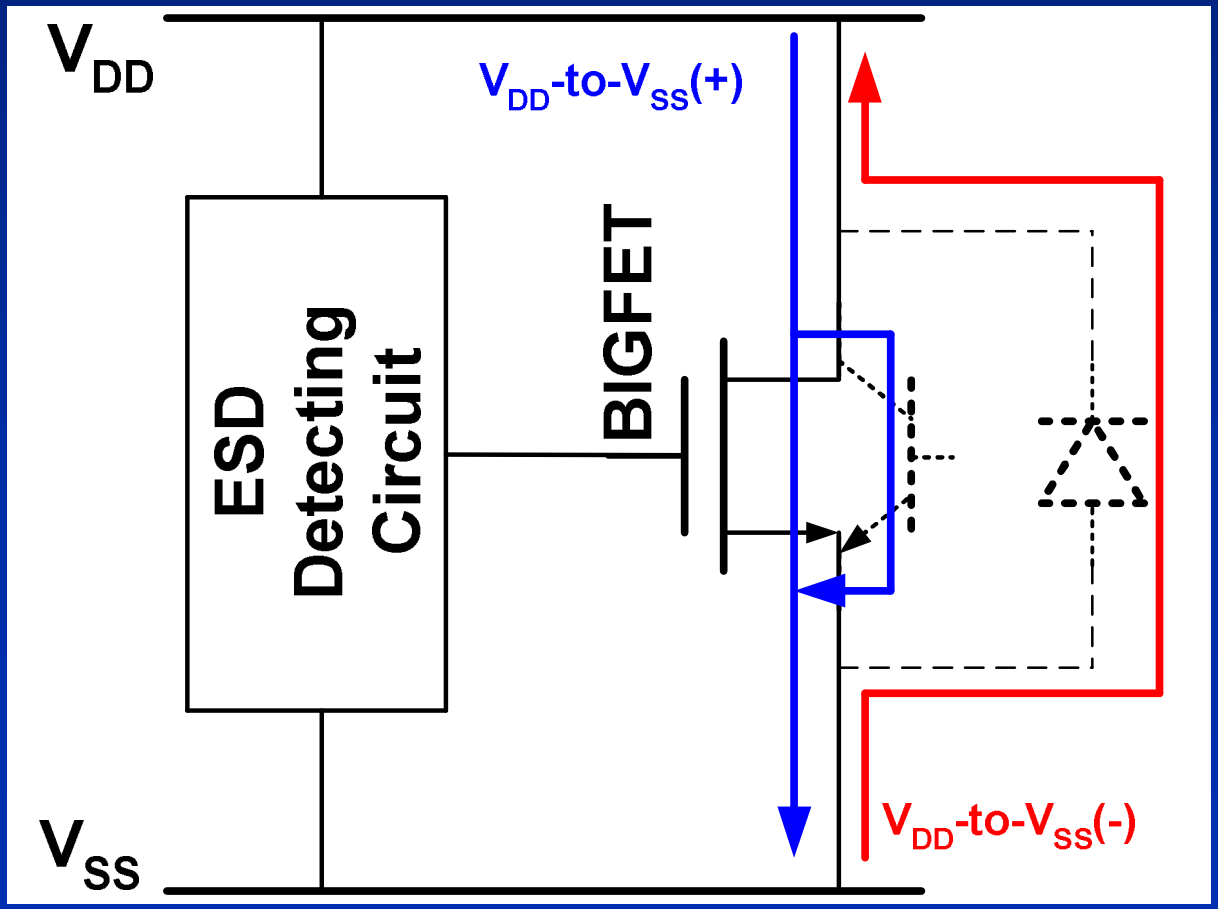


# HBM ESD Robustness

| RC Time Constant | $S_{dg}$=0.44 μm | | $S_{dg}$=0.33 μm | | $S_{dg}$=0.22 μm | |
|---|---|---|---|---|---|---|
| | (+) | (-) | (+) | (-) | (+) | (-) |
| 0.1 ms | 7.5 kV | 7.5 kV | 6.5 kV | 7.5 kV | 5.5 kV | 7.5 kV |
| 0.5 ms | >8.0 kV | >8.0 kV | 7.0 kV | >8.0 kV | 5.5 kV | 7.5 kV |
| 1.0 ms | 7.5 kV | >8.0 kV | 5.5 kV | >8.0 kV | 4.5 kV | 7.5 kV |

# Discharging Paths under ESD Stress

- $V_{DD}$-to-$V_{SS}$(+) : surface channel & npn BJT
- $V_{DD}$-to-$V_{SS}$(-) : parasitic diode



# Conclusions

- Although the layout area is increasing with larger $S_{dg}$, the effective improvement on ESD level is more beneficial to on-chip ESD protection design.
- From TLP measured results, the clamp device (BIGFET) drawn with larger $S_{dg}$ indeed performs lower turn-on resistance.
- There is an optimized value on RC time constant for using in the ESD detecting circuit.

# References


[1] S. Voldman, *ESD Physics and Devices*, John Wiley & Sons, Ltd., England, 2004.

[2] M.-D. Ker, "Whole-chip ESD protection design with efficient VDD-to-VSS ESD clamp circuits for submicron CMOS VLSI," *IEEE Trans. on Electron Devices*, vol. 46, pp. 173-183, 1999.

[3] R. Merrill and E. Issaq, "ESD design methodology," in *Proc. of EOS/ESD Symp.*, 1993, pp. 233-237.

[4] J. Li, R. Gauthier, and E. Rosenbaum, "A compact, timed-shutoff, MOSFET-based power clamp for on-chip ESD protection," in *Proc. of EOS/ESD Symp.*, 2004, pp. 273-279.

[5] M. Mergens, et al., "ESD protection circuit design for ultra-sensitive IO application in advanced sub-90nm CMOS technologies," in *Proc. of ISCAS*, 2005, pp. 1194-1197.