Design of 2xVDD-Tolerant I/O Buffer with 1xVDD CMOS Devices

Ming-Dou Ker[1,2] and Yan-Liang Lin[1]
[1]Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan
[2]Department of Electronic Engineering, I-Shou University, Kaohsiung, Taiwan

Abstract - **A new 2xVDD-tolerant I/O buffer realized with only 1xVDD devices has been proposed and verified in a 0.18-μm CMOS process. With the dynamic source output technique and the new gate-controlled circuit, the new proposed I/O buffer can transmit and receive the signals with the voltage swing twice as high as the normal power supply voltage (VDD) without suffering gate-oxide reliability problem. The proposed 2xVDD-tolerant I/O circuit solution can be implemented in different nanoscale CMOS processes to meet the mixed-voltage interface applications in microelectronic systems.**

I. Introduction

Recently, there are several essential topics on the I/O circuit design, such as PVT compensation techniques, simultaneous switching noise reduction, and gate-oxide overstress protection. The PVT compensation techniques detect process, voltage, and temperature variations in an integrated circuit chip and adjust the driving capability of the output buffer to reduce the rise/fall time variation with PVT, so the slew rate of the output voltage can be kept as constant as possible [1], [2]. The circuit techniques of simultaneous switching noise reduction were reported to reduce the ground bounce of I/O buffers [3], [4]. Besides, the gate-oxide reliability issue is another important topic to the I/O circuit design in the scaled-down CMOS technology.

With the rapid development of CMOS techniques, the power supply voltage (VDD) is reduced for low-power applications and the thickness of gate oxide has been scaled down to increase circuit operating speed. In the meanwhile, the maximum tolerable voltage across the transistor terminals should be decreased to ensure lifetime. However, the chips may receive the I/O signals with voltage levels higher than their normal supply voltage (VDD) from the old interface protocols of other CMOS ICs in a microelectronic system with multiple/different power supply voltages. Thus, it becomes more important to prevent the thin gate oxide of the I/O circuits in IC from voltage overstress in such mixed-voltage microelectronic systems. Recently, several mixed-voltage I/O buffers realized with thin oxide devices to receive input signals of higher voltage but only to transmit 1xVDD output signals were reported in [5]-[7].

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In this work, a 2xVDD-tolerant I/O buffer which can transmit and receive 2xVDD I/O signals without suffering gate-oxide reliability issue is proposed and verified in a 0.18-μm CMOS process.

II. New Proposed 2xVDD-Tolreant I/O Buffer

A. Design Concept

Fig. 1 and Fig. 2 show the design concept of the dynamic source output technique. MP and MN are the transistors of the output stage in an I/O circuit. As shown in Fig. 1(a), when transmitting signal high (2xVDD), the 2xVDD voltage at I/O PAD must come from the source of transistor MP. The gate voltage of MP should keep MP on and keep the voltage across gate to source and gate to drain within the normal power supply voltage (VDD), so the gate voltage must be VDD. At the same time, the gate voltage of MN must be also VDD to keep the voltage across gate to drain within VDD, and the source voltage of MN should be VDD to turn MN off. By the similar analysis, when transmitting signal low (0V), the voltages at each terminal can be derived as shown in Fig. 1(b). Comparing Fig. 1(a) and Fig. 1(b), it can be discovered that no matter transmitting high or low, the gate voltages of transistors MP and MN won't change but their source voltages would change. Therefore, it provides us a way to control the transistors MP and MN on or off by changing their source voltage in the transmit mode.

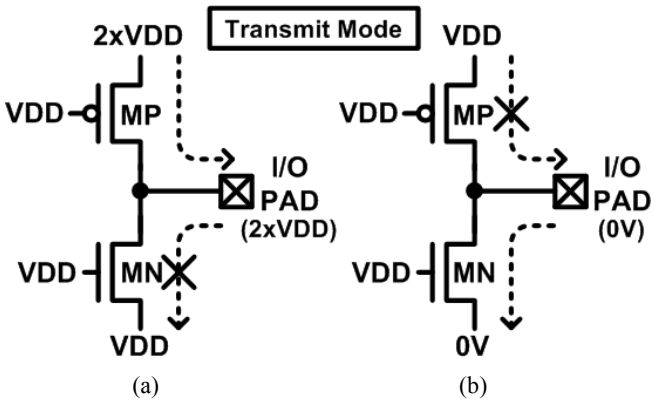

Fig. 1. The operations of the output stage in a 2xVDD-tolerant I/O buffer in transmit mode with (a) transmitting high and (b) transmitting low.

TABLE I
Operation Modes of the new proposed 2xVDD-tolerant I/O buffer.

Operating Modes	Dout	PUH	PD	Node A	Node B	TP	TN	I/O PAD
Transmit	0V	2xVDD	VDD	VDD	0V	VDD	VDD	0V
	VDD	VDD	0V	2xVDD	VDD	VDD	VDD	2xVDD
Receive	X	2xVDD	0V	VDD	VDD	VDD	0V	0V
	X	2xVDD	0V	VDD	VDD	2xVDD	VDD	2xVDD

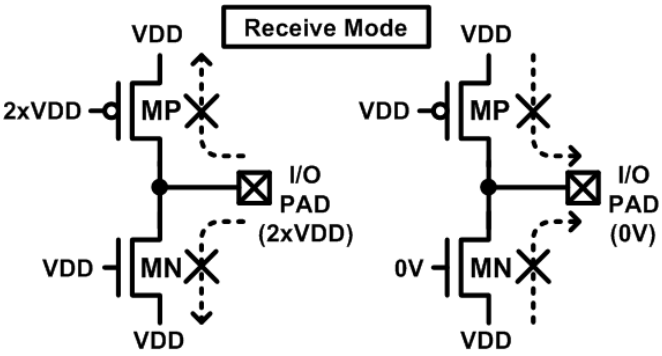

Fig. 2. The operations of the output stage in a 2xVDD-tolerant I/O buffer in receive mode with (a) receiving high and (b) receiving low.

Fig. 2 shows the operations of the output stage in the 2xVDD-tolerant I/O buffer during receive mode. In receive mode, the output stage should be kept completely off to avoid any unnecessary circuit leakage path. According to the operations in receive mode, the control signals from pre-driver will make the source voltages of MP and MN at VDD. As shown in Fig. 2(a), when I/O pad receiving 2xVDD input signal, the gate voltage of transistor MP should be biased at 2xVDD, and the gate of MN should be kept at VDD, to fully turn them off without suffering gate oxide reliability problem. With the same design consideration, the gate voltages of MP and MN can be arranged as that shown in Fig. 2(b) when I/O pad receiving signal low (0V).

B. Circuit Scheme and Operation Modes

Fig. 3 shows the whole circuit scheme of the proposed 2xVDD-tolerant I/O buffer with the dynamic source output technique and the new gate-controlled circuit to protect the I/O buffer realized with 1xVDD devices against gate oxide reliability during transmitting and receiving 2xVDD signals. In transmit mode, according to the above analysis, the gate-controlled circuit biases the gate voltages TP and TN of transistors MP and MN at VDD, and then the dynamic source output stage controls the transistors MP and MN to be on or off by changing their source voltages. When the I/O buffer transmits 2xVDD output signal, PUH is pulled down to VDD by the level converter which is implemented with all 1xVDD devices [8]. Then, the voltage at node A is 2xVDD due to the conduction of transistor MPP while MPN is off. At the same time, PD is pulled down to 0V, and the voltage at node B is VDD since transistor MNP is on while MNN is off. Consequently, the I/O PAD is pulled high to 2xVDD. The similar operation for the I/O buffer to transmit 0-V output signal can be derived. In receive mode, the signals from PU and PD will control the voltages at node A and node B to VDD, and then the gate-controlled circuit provides appropriate voltages to TP and TN to completely turn MP and MN off. When the I/O buffer receives 2xVDD input signal, TP is biased at 2xVDD and TN is biased at VDD. When the I/O buffer receives 0-V input signal, TP is biased at VDD and TN is biased at 0V. Accordingly, MP and MN can be completely turned off. The corresponding circuit operating voltages of the proposed 2xVDD-tolerant I/O buffer in two operating modes are summarized in Table I.

To avoid leakage current of the parasitic pn-junction diode in p-channel transistors, the bulks of transistors MP and MPP which are related to 2xVDD signals are connected to 2xVDD, and the bulks of transistors MNP and MI2 which are only related to VDD signals are connected to VDD for the concern of driving capacity. In general, the drain-to-bulk breakdown voltage is at least twice the normal operating voltage in the standard CMOS process [9], [10]. Hence, the drain-to-bulk breakdown issue would be ignored in the proposed 2xVDD-tolerant I/O buffer.

It has been verified by simulation in a 0.18-μm CMOS process that the maximum voltage across any two terminals of each transistor in the proposed 2xVDD-tolerant output buffer is kept within VDD. The simulated waveforms of the proposed I/O buffer to transmit or to receive 133-MHz 2xVDD signals with 10-pF loading and VDD of 1.5V are shown in Fig. 4.

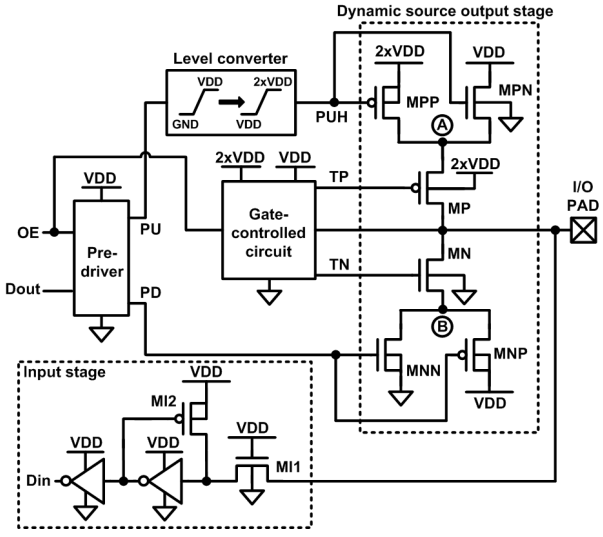

Fig. 3. The new proposed 2xVDD-tolerant I/O buffer.

As shown in Fig. 4(a), when the I/O buffer is operating in the transmit mode, the nodes TP and TN are 1.5V. If it transmits 3.3-V signals, node A will be 3.3V and node B will be 1.5V. If it transmits 0-V signals, node A will be 1.5V and node B will be 0V. On the other hand, as shown in Fig. 4(b), when the I/O buffer is operating in the receive mode, the nodes A and B are 1.5V. If it receives 3.3-V signals, node TP will be 3.3V and node TN will be 1.5V. If it receives 0-V signals, node TP will be 1.5V and node TN will be 0V.The simulated results are all consistent to this design expectation. The voltage across any two terminals of each transistor in the output stage would not exceed VDD.

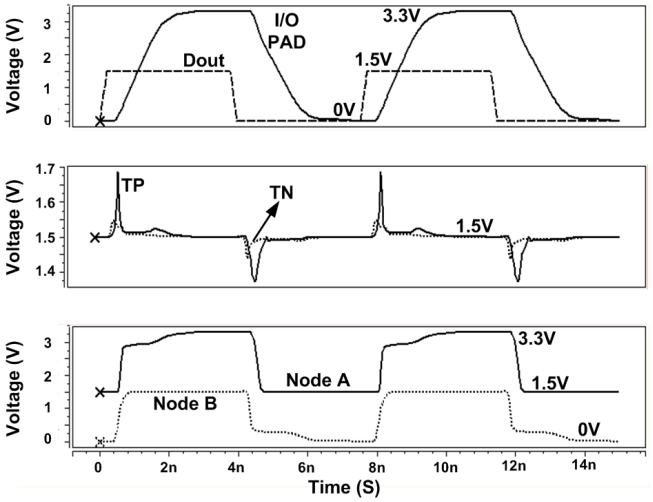

Fig. 4. Simulated waveforms of the proposed 2xVDD-tolerant I/O buffer with 133-MHz signals in (a) transmit mode, and (b) receive mode.

C. Gate-controlled Circuit

Fig. 5 shows the implementation of the gate-controlled circuit with 1xVDD devices which can provide appropriate voltages to the gates of MP and MN. The gate-controlled circuit can be divided into an upper part and an under part,

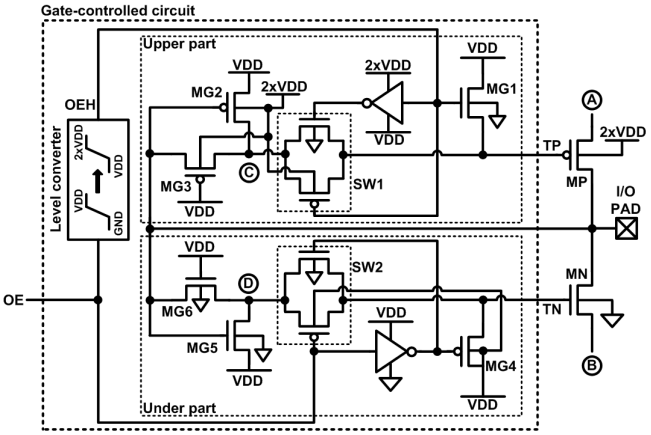

Fig. 5. The gate-controlled circuit for the proposed 2xVDD-tolerant I/O buffer.

which are with the complementary structures. All the signals in the upper part are VDD-to-2xVDD, and all the signals in the under part are 0V-to-VDD, so it can be guaranteed that there are no gate-oxide reliability problems in this gate-controlled circuit. To avoid the leakage current, the bulks of p-channel transistors in the upper part are all connected to 2xVDD, and the bulks of p-channel transistors in the under part are all connected to VDD. In transmit mode, the switches SW1 and SW2 are off to block the signals of node C and node D. Meanwhile, transistors MG1 and MG4 are on to bias TP and TN at VDD. In receive mode, the switches SW1 and SW2 are on. Transistors MG1 and MG4 are off, so the voltages of node C and node D can be transmitted to TP and TN. When the I/O buffer receives 2xVDD input signals, in the upper part, the signal from I/O PAD (2xVDD) transmits to TP through transistor MG3 and switch SW1 while MG2 is off. In the under part, transistor MG6 blocks the I/O PAD signal from transmitting to node D, and at this moment, MG5 is turned on to provide VDD to TN. As the I/O buffer receives 0-V input signal, the operation concept is similar to that receiving a 2xVDD input signal.

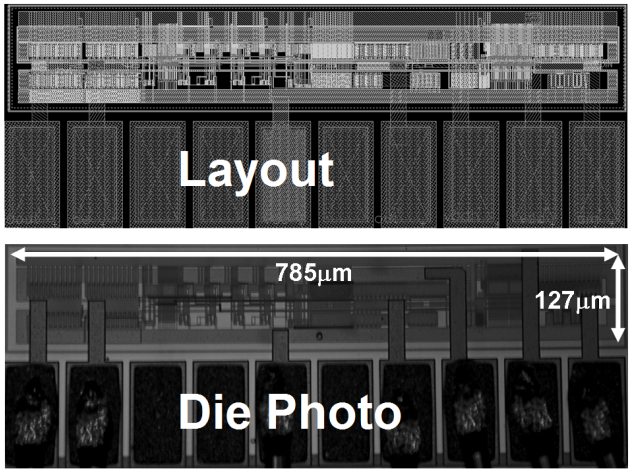

Fig. 6. The layout and die photo of the proposed 2xVDD-tolerant I/O buffer.

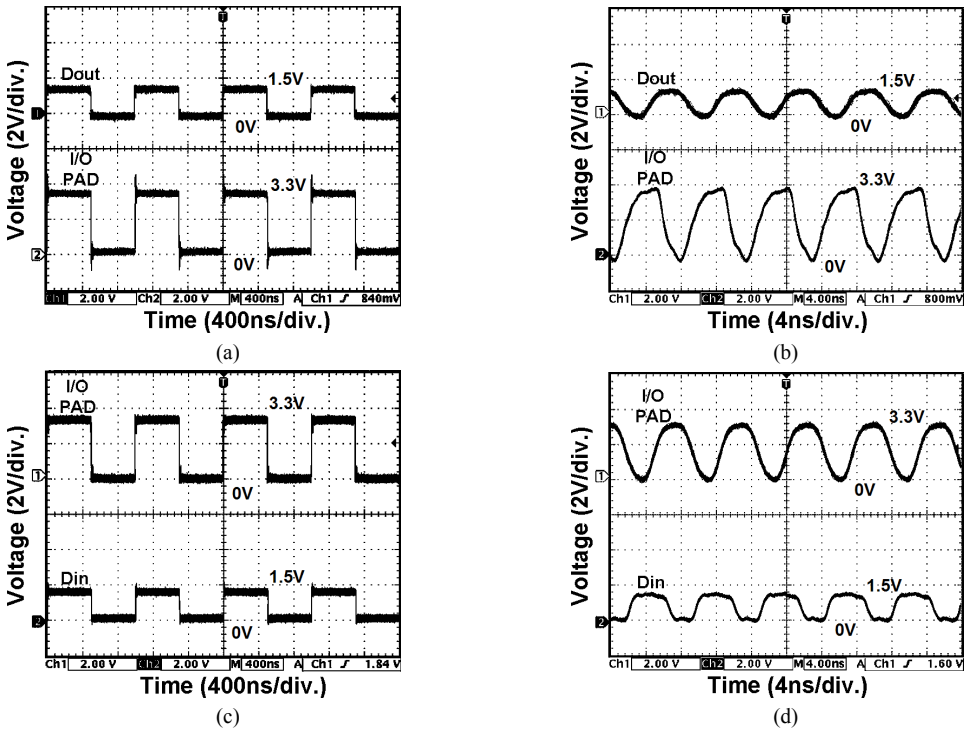

Fig. 7. The measurement results of the proposed 2xVDD-tolerant I/O buffer with (a) 1-MHz signals in transmit mode, (b) 133-MHz signals in transmit mode, (c) 1-MHz signals in receive mode, and (d) 133-MHz signals in receive mode.

III. Experimental Results

The layout and die photo of the proposed 2xVDD-tolerant I/O buffer fabricated in a 0.18-μm 1.8-V CMOS process is shown in Fig. 6. The active area of the proposed I/O buffer is around 127μm x 785μm. The measured waveforms of the proposed I/O buffer to transmit and receive 3.3-V signals are shown in Fig. 7 with VDD of 1.5V. Fig. 7(a) and Fig. 7(b) show the measured waveforms in transmit mode with respect to 1-MHz and 133-MHz signals. It is noticed that the input Dout is 1.5V and the output I/O PAD is 3.3V. Fig. 7(c) and Fig. 7(d) show the measured waveforms in receive mode with respect to 1-MHz and 133-MHz signals, where the input I/O PAD is 3.3V and the output Din is 1.5V. The experimental results have confirmed that the proposed 2xVDD-tolerant I/O buffer can successfully transmit and receive 2xVDD signals up to 133MHz.

IV. Conclusion

A 2xVDD-tolerant I/O buffer has been successfully designed with dynamic source output technique and realized with 1xVDD CMOS devices in this work, which has been fabricated in a 0.18-μm 1.8-V CMOS process to transmit and receive 3.3-V signals without suffering gate-oxide reliability issue. The new proposed 2xVDD-tolerant I/O circuit solution can be implemented in different nanoscale CMOS processes to meet the mixed-voltage applications in microelectronic systems.

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