Transient-to-Digital Converter for Protection Design in CMOS Integrated Circuits against Electrical Fast Transient

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***Abstract* - An on-chip transient-to-digital converter for protection design against electrical fast transient (EFT) is proposed. The proposed transient-to-digital converter is designed to detect fast electrical transients under EFT tests. The output digital codes can correspond to different EFT voltages during the EFT-induced transient disturbances. The experimental results in a 0.18-μm CMOS integrated circuit (IC) with 3.3-V devices have confirmed the detection function and digital output codes.**

***Keywords* – converter, electrical fast transient (EFT) test, transient detection circuit.**

I. Introduction

The reliability issue of electrical fast transient (EFT) events has attracted more attention than before in the microelectronic systems equipped with CMOS integrated circuits (ICs) [1]. This tendency results from not only the progress of more functions integrated into a single chip but also from the strict requirements of reliability test standards, such as the EFT test. The microelectronic product must sustain the EFT voltage level of ±2kV under EFT tests to achieve the immunity requirement of "level 4" in the IEC 61000-4-4 test standard [2]. During EFT tests, the power lines of the CMOS ICs in the microelectronic products no longer maintained normal voltage levels, but an exponential voltage pulse with the amplitude of several tens volts occurred. Such fast electrical transient disturbances often cause damage or malfunction to CMOS ICs inside the equipment under test (EUT) [3]-[5].

In order to solve such EFT issues, the traditional solution is to add some board-level noise filters into the microelectronic products to decouple, bypass, or absorb the electrical transients under EFT tests [6]. However, such additional discrete components substantially increase the total cost of microelectronic products. Therefore, the chip-level solutions without using additional discrete noise-bypassing components are highly requested by IC industry [7].

In this paper, a novel on-chip transient-to-digital converter is proposed to detect the fast electrical transients and convert to digital codes under EFT tests. The test chip fabricated in a 0.18-μm CMOS process has verified that the proposed on-chip transient-to-digital converter can successfully transfer different EFT voltage levels into digital thermometer codes.

II. Electrical Fast Transient (EFT) Tests

According to the IEC 61000-4-4 standard [3], the simplified circuit diagram of the EFT generator is shown in Fig. 1. In particular, only the impedance matching resistor R_m (50Ω) and the dc blocking capacitor C_d (10nF) are fixed. The charging capacitor C_c is used to store the charging energy and R_s is used to shape the pulse duration. The repetitive EFT test is a test with bursts consisting of a number of fast pulses. With the repetition frequency of 5kHz and 100kHz, the burst repeats every 300ms and the application time is not less than 1 minute. For EFT pulse with the repetition frequency of 5kHz, the general EFT voltage waveforms on a 50Ω load are measured in Fig. 2 with the pulse peak of 200V. In the inset figure of Fig. 2, the waveform of a single pulse has a rise time of about ~5ns and the pulse duration of ~50ns.

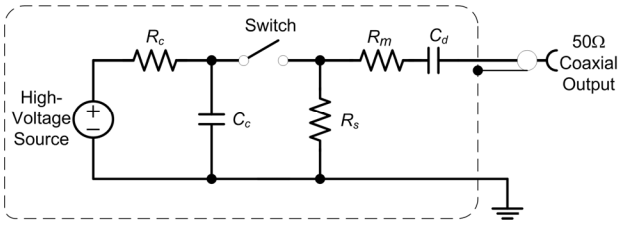

Fig. 1. Simplied circuit diagram of EFT generator.

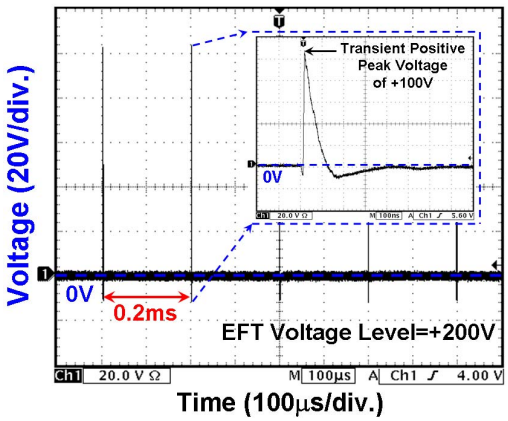

Fig. 2. EFT transient waveforms on a 50 Ω load with repetition rate of 5kHz.

III. Transient Detection Circuit

A. Circuit Implementation

Fig. 3 shows the on-chip transient detection circuit. The RC-based circuit structure is designed to realize the transient detection function. The NMOS (M_{nr}) is used to provide the initial reset function to set the initial output voltage (V_{OUT}) level to 0V. The node V_X is biased at V_{DD} and the node V_G is biased at V_{SS} during the normal operation condition. Under the EFT tests, the voltage waveform of V_X has much slower voltage response than the voltage waveform at V_{DD} because the RC circuit has a time constant in the order of microsecond (μs). Due to the longer time delay, the PMOS device in the inverter1 (INV_1) and NMOS (M_{n1}) can be turned on to pull down the voltage level at the node V_A. Therefore, the logic level stored in the two-inverter latch and output voltage (V_{OUT}) of the proposed on-chip transient detection circuit can be changed from 0V to 3.3V to memorize the occurrence of EFT events.

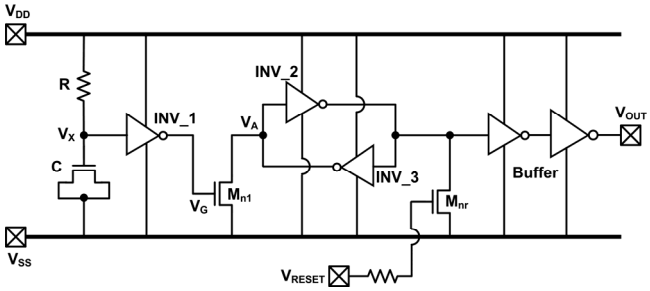

Fig. 3. The on-chip transient detection circuit.

B. Experimental Results

In order to simulate the EFT-induced transient disturbance on CMOS ICs inside the microelectronic products, the attenuation network with -40dB degradation is used in this work. The amplitude of EFT-induced transients can be adjusted through the attenuation network.

The measurement setup for EFT test combined with attenuation network is shown in Fig. 4. EFT generator is connected to the device under test (DUT) through the attenuation network with V_{DD} of 3.3V. The connected cable type is coaxial cable line. The V_{DD} and V_{OUT} transient responses of the on-chip transient detection circuit are monitored by the digital oscilloscope to verify the detection function.

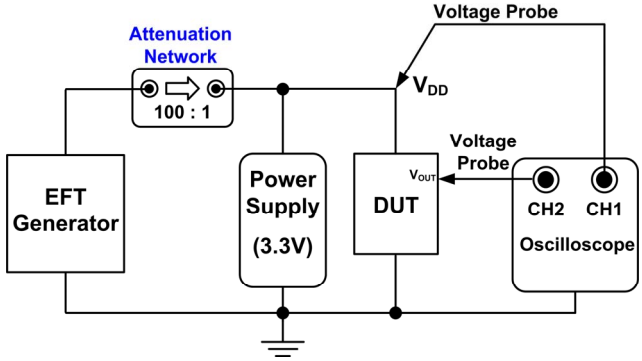

Fig. 4. Measurement setup for EFT test combined with attenuation network.

The measured V_{DD} and V_{OUT} waveforms of the on-chip transient detection circuit under EFT test with EFT voltage of +500V are shown in Fig. 5(a). As shown in Fig. 5(a), under the EFT test with positive EFT voltage, V_{DD} begins to increase rapidly from 3.3V. Meanwhile, V_{OUT} starts to greatly increase with positive exponential voltage pulse coupled on V_{DD} power line. Finally, after the EFT-induced transient disturbance, the output voltage (V_{OUT}) of the on-chip transient detection circuit is changed from 0V to 3.3V. Therefore, the on-chip transient detection circuit can memorize the occurrence of the EFT event with positive EFT voltage.

The measured V_{DD} and V_{OUT} transient waveforms of the on-chip transient detection circuit under EFT test with EFT voltage of -500V are shown in Fig. 5(b). As shown in Fig. 5(b), under the EFT test with negative EFT voltage, V_{DD} begins to decrease rapidly from 3.3V. V_{OUT} is disturbed simultaneously with negative exponential voltage pulse coupled on V_{DD} power line. Finally, after the negative EFT-induced transient disturbance, the output voltage (V_{OUT}) of the on-chip transient detection circuit transits from 0V to 3.3V.

From the EFT test results, the on-chip transient detection circuit can memorize the occurrence of the EFT events with positive or negative EFT voltages.

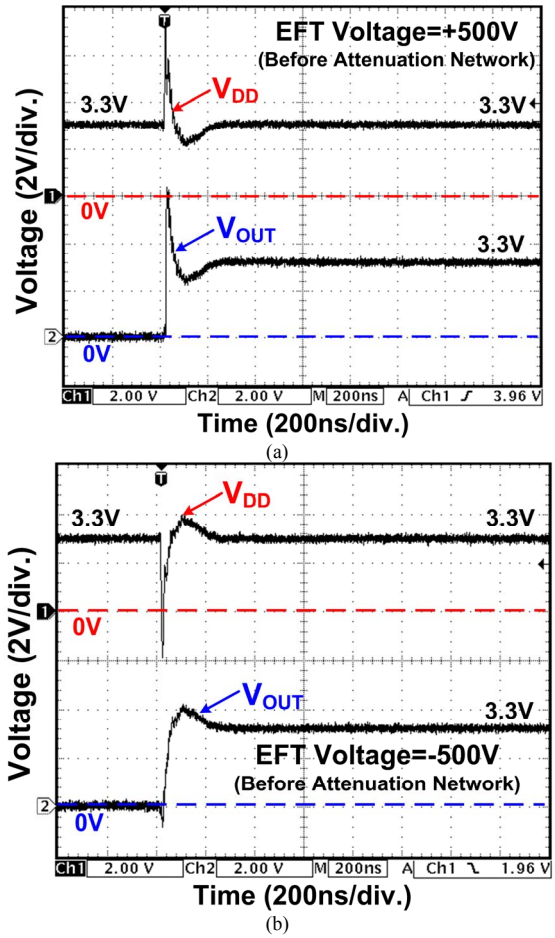

Fig. 5. Measured V_{DD} and V_{OUT} transient waveforms under EFT tests of (a) +500V, and (b) -500V.

IV. Transient-to-Digital Converter

A. Circuit Implementation

It has been investigated that noise filter networks can reduce the susceptibility of CMOS ICs against fast electrical transients by decoupling, bypassing, or absorbing electrical transient noise voltage (energy). It has been also reported that the noise filter networks have strong impacts to the parameters of the underdamped sinusoidal voltage such as transient peak voltage, damping frequency, and damping factor [6].

Fig. 6 shows the proposed on-chip transient-to-digital converter consisted of four transient detection circuits and four different RC filter networks. The RC filter network is realized with one decoupling capacitor and two resistors with equal value to provide the noise filter function during EFT stresses. The RC noise filter network can suppress the transient peak voltages on V_{DD} and V_{SS}, which has influence on EFT voltages to cause transition at the output (V_{OUT}) of the on-chip transient detection circuit. For the proposed on-chip transient-to-digital converter, with different R and C values in the filter networks, different EFT levels on V_{DD} and V_{SS} will reach to each transient detection circuit. Under the EFT zapping conditions, the four transient detection circuits will have different output voltage responses. Therefore, by combining with different RC noise filter networks, the proposed on-chip transient-to-digital converter can be designed to detect different EFT voltage levels and transfer output voltages into digital thermometer codes under EFT tests.

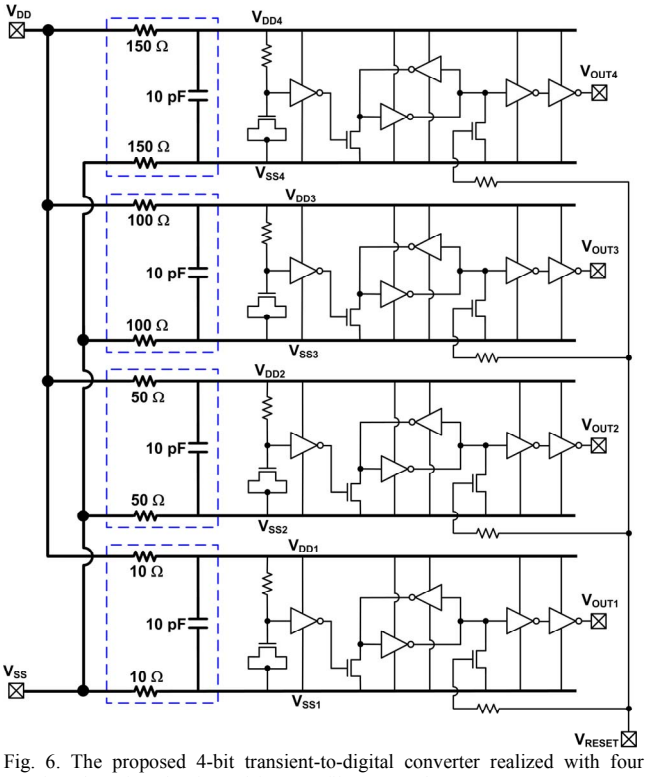

Fig. 6. The proposed 4-bit transient-to-digital converter realized with four transient detection circuits and four RC filter networks.

B. Experimental Results

The proposed on-chip 4-bit transient-to-digital converter has been designed and fabricated in a 0.18-μm 1P5M CMOS process with 3.3-V devices. The fabricated chip in a package for EFT test is shown in Fig. 7. The silicon area of the proposed on-chip transient-to-digital converter is 1030μm x 188.5μm.

The EFT generator combined with attenuation network shown in Fig. 4 is used to evaluate the digital thermometer codes of the proposed on-chip transient-to-digital converter under EFT tests. The V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} transient responses of the proposed on-chip transient-to-digital converter are monitored by the digital oscilloscope. Before EFT test zapping, the initial output voltages of the proposed on-chip transient-to-digital converter are reset to 0V. After each EFT zapping, the output voltage levels are measured to check the final voltage levels and to verify the transferred digital codes.

The measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} waveforms of the proposed transient-to-digital converter under EFT test with EFT voltage of -600V are shown in Fig. 8. During the EFT-induced disturbance, V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} are disturbed simultaneously. Finally, V_{OUT1} will be changed from 0V to 3.3V, while V_{OUT2}, V_{OUT3}, and V_{OUT4} are still kept at 0V. Therefore, under EFT test with EFT voltage of -600V zapping, the detection output voltages can be transferred into a digital thermometer code of "0001."

Under EFT test with EFT voltage of -650V, V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} are disturbed simultaneously. After EFT-induced transient disturbance coupled to V_{DD} line, V_{OUT1} and V_{OUT2} are pulled up from 0V to 3.3V, while V_{OUT3} and V_{OUT4} are still kept at 0V. Therefore, under EFT test with EFT voltage of -650V zapping condition, the output voltages can be transferred into a digital thermometer code of "0011.".

Under EFT test with EFT voltage of -700V, V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} are disturbed at the same time. After the fast transients, V_{OUT1}, V_{OUT2}, and V_{OUT3} will be changed from 0V to 3.3V, while V_{OUT4} is still kept at 0V. Therefore, with EFT voltage of -700V zapping, the detection results can be transferred into a digital thermometer code of "0111."

Under EFT test with EFT voltage of -800V, all transient detection circuits can detect the occurrence of transient disturbance on V_{DD}. Finally, V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} are all changed from 0V to 3.3V. Therefore, under EFT test with EFT voltage of -800V zapping, the detection results can be transferred into a digital thermometer code of "1111."

Similarly, under EFT test with EFT voltages of +700V, +1800V, +2400V, and +3400V, the transferred digital thermometer codes of proposed on-chip transient-to-digital converter are "0001," "0011," "0111," and "1111," respectively. Therefore, under EFT tests with positive or negative EFT voltages, the proposed on-chip transient-to-digital converter can successfully transfer different EFT voltage levels into digital thermometer codes.

Fig. 9 depicts the EFT voltage to digital code characteristic of the proposed transient-to-digital converter. With larger EFT voltage level under EFT tests, the transferred digital thermometer code goes higher.

C. Application in Microelectronic Systems Co-design

The proposed on-chip transient-to-digital converter can be co-designed with firmware to provide a system solution to solve the EFT event on microelectronic products equipped with CMOS ICs.

Under the normal power-on condition, the V_{DD} power-on voltage waveform has a rise time on the order of a millisecond (ms). The power on reset circuit should be designed with the longer rise time and send the system power-on firmware index to execute a normal reset procedure.

Under the EFT zapping with a low EFT voltage, the output digital code of the proposed on-chip transient-to-digital converter becomes "0001." Then, the firmware can execute the partial system recovery procedure to check and to recover partial electrical functions of microelectronic system. Under the EFT zapping with high enough EFT voltage, the output digital code of the proposed on-chip transient-to-digital converter becomes "1111." Then, the firmware can execute the recovery procedure to recover all the electrical functions to a desired stable state as soon as possible. The firmware can be designed to execute different recovery procedures with different digital codes. After the recovery procedures, the output digital code of the proposed on-chip transient-to-digital converter is again reset to "0000" for detecting the next EFT-induced transient disturbance.

With the system-level ESD test in IEC 61000-4-2 standard [8], the proposed on-chip transient-to-digital converter can also successfully detect and transfer the ESD-induced transient voltage into digital thermometer codes [9]. Such transient-to-digital converter can be co-designed with firmware/software to solve the system-level ESD protection issue in microelectronics systems.

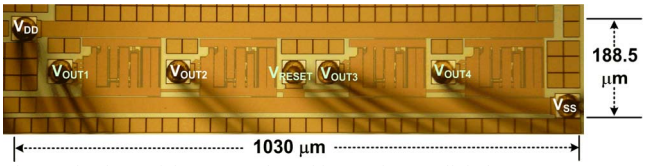

Fig. 7. Die photo of the proposed on-chip transient-to-digital converter.

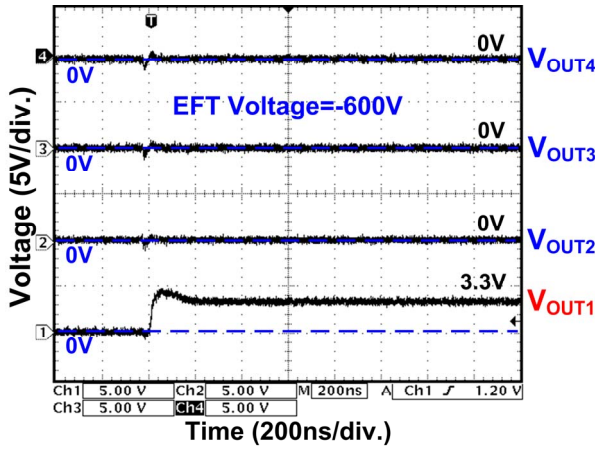

Fig. 8. Measured V_{OUT1}, V_{OUT2}, V_{OUT3}, and V_{OUT4} transient voltage waveforms under EFT test with EFT voltage of -600V.

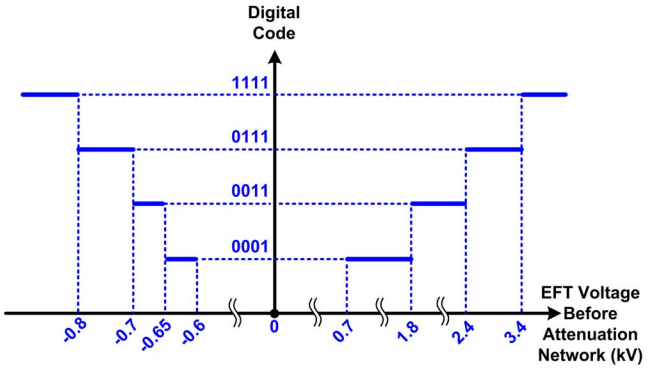

Fig. 9. EFT voltage to digital code characteristic.

V. Conclusions

A novel transient-to-digital converter composed of four transient detection circuits and four different RC filter networks has been successfully designed and verified in a 0.18-μm CMOS process with 3.3-V devices. The output digital thermometer codes of the proposed transient-to-digital converter correspond to different EFT voltages under EFT tests. These output digital thermometer codes can be used as the firmware index to execute different system recovery procedure of microelectronic products. Therefore, the proposed transient-to-digital converter can be further co-designed with firmware to provide an effective solution to solve the EFT-induced transient disturbance events in microelectronic systems equipped with CMOS ICs.

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