Low-Leakage Electrostatic Discharge Protection Circuit in 65-nm Fully-Silicided CMOS Technology

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Abstract — **A new low-leakage power-rail electrostatic discharge (ESD) clamp circuit, composed of the SCR device and new ESD detection circuit, has been designed with consideration of gate current to reduce the total standby leakage current under normal circuit operating conditions. After fabrication in a 1-V 65-nm fully-silicided CMOS process, the proposed power-rail ESD clamp circuit can sustain 7kV human-body-model (HBM) and 325V machine model (MM) ESD tests which occupying an silicon area of only 49μm×21μm and consuming a very low standby leakage current of 96nA at room temperature.**

Index Terms — **Electrostatic discharge (ESD), gate leakage, power-rail ESD clamp circuit, silicon controlled rectifier (SCR).**

I. Introduction

With the decrease of the power supply voltage for low power applications, the thickness of the gate oxide has been scaled down in the nanometer CMOS technologies. However, such a thin gate oxide of below ~2nm in advanced CMOS technology has been reported to result in a substantial fraction of the overall leakage current in the chip due to its gate leakage current [1]. In 45-nm generation and beyond, the metal gate cooperated with high-k gate oxide is therefore applied to reduce the gate leakage current [2]. Nevertheless, the gate leakage issue still exists in the 90-nm and 65-nm technologies which are widely used in production of most consumer ICs without metal gate structure. The gate current has been modeled in BSIM4 MOSFET model [3], and the foundries have also provided the corresponding SPICE models of nanometer CMOS processes to circuit designers.

From the perspective on electrostatic discharge (ESD) protection, the power-rail ESD clamp circuit to effectively protect the core circuits is traditionally implemented by RC-based ESD protection structure with a large-sized ESD clamping MOSFET [4]. However, the gate leakage current caused from the large-sized MOSFET and the MOS capacitor in the traditional power-rail ESD clamp circuit becomes serious in nanoscale CMOS processes. For example, the gate current flowing through a MOS capacitor with W/L of 5μm/5μm under 1-V bias is as large as 2μA in a 65-nm CMOS process. The ESD clamping MOSFET cannot be completely turned off under the power-on condition due to the malfunction of the ESD detection circuit caused from the leakage current in the MOS capacitor, and in turn to induce extra large leakage current through ESD clamping MOSFET.

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To solve the problem of malfunction in the traditional RC-based ESD detection circuit, the timer level restorer was ever reported [5]. However, even with the additional timer level restorer, the gate current of ESD clamping MOSFET and MOS capacitor still result in a total standby leakage current of several ten micro-amperes at 125°C in a 0.13μm CMOS process [5]. Such leaky ESD protection circuit is barely tolerable to portable product applications. New designs of the power-rail ESD clamp circuit should be developed to further reduce such standby leakage current in nanometer CMOS processes.

In this work, a new power-rail ESD clamp circuit with low standby leakage current is proposed. The new proposed ESD clamp circuit has an efficient ESD detection circuit to improve the turn-on efficiency of the ESD clamping device. By using the new proposed circuit solution realized with only thin gate-oxide devices, the standby leakage current of the proposed power-rail ESD clamp circuit can be successfully reduced in the normal circuit operating condition. The proposed power-rail ESD clamp circuit has been successfully verified in a 1-V 65-nm fully-silicided CMOS process.

II. New Proposed Low-Leakage Power-Rail ESD Clamp Circuit

The proposed low-leakage power-rail ESD clamp circuit is shown in Fig. 1. The p-type substrate-triggered silicon-controlled rectifier (SCR) device is used as the main ESD clamping device [6]. The SCR device, which is composed of cross-coupled n-p-n and p-n-p BJTs with regenerative feedback loop, with a low holding voltage can sustain a high ESD level within a smaller silicon area in CMOS process. Moreover, the SCR device without poly gate structure has good immunity against the gate leakage problem. The ESD detection circuit, which is designed with consideration of the gate current along the MOS capacitors, is used to enhance the turn-on speed of SCR device for effectively protecting the internal circuits. Utilizing the gate current to bias the ESD detection circuit and to reduce the voltage difference across the gate of MOS capacitors, the overall standby leakage current of the power-rail ESD clamp circuit can be further minimized by this new proposed design.

A. Normal Circuit Operating Condition

Under the power-on condition with VDD of 1V and grounded VSS, the node a in Fig. 1 is biased at around 1V

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through the resistor R with a low gate current of MOS capacitor Mc1, so that Mp1 is turned off and no trigger current at trigger node is generated from the ESD detection circuit. The node c in Fig. 1 is initially biased at some voltage level (~0.45V) to turn on Mn and then to keep the trigger node grounded. The diode-connected Mp2 and Mp3 are used as start-up circuit by conducting the gate current of Mc1 to bias the nodes c, d, and e. After that, the voltage level at the node d will be biased at some voltage level (~0.7V) to reduce the voltage drop across the gate of Mc1 and to minimize the gate leakage current through the MOS capacitors (Mc1 and Mc2). Fig. 2 shows the Hspice-simulated voltage waveforms on the nodes of the proposed ESD detection circuit and the gate current through Mc1 during the normal power-on transition with a rise time of 1ms and VDD of 1V (VSS of 0V). The gate current of Mc1 after VDD power-on transition is only around 23nA and the voltage level at the node a is almost kept at 1V (overlapped with VDD in Fig. 2), so that Mp1 is kept in off state.

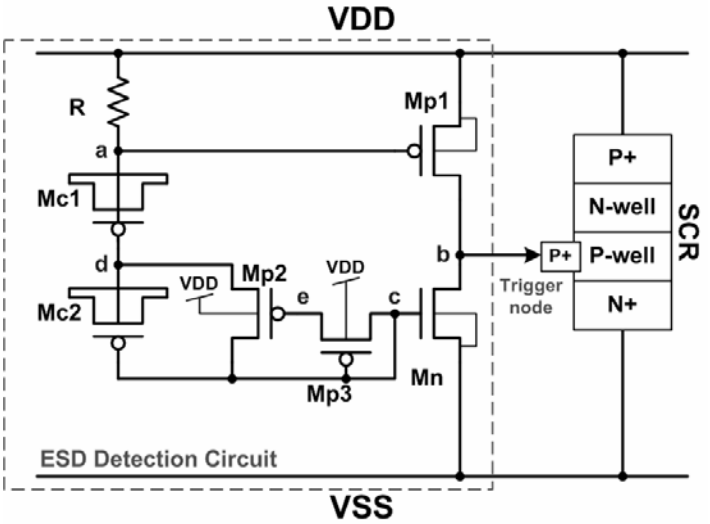

Fig. 1. The proposed low-leakage power-rail ESD clamp circuit with p-type substrate-triggered SCR device as ESD clamp device, where the ESD detection circuit is designed with consideration of gate leakage current.

B. ESD Transient Condition

When a positive fast-transient ESD voltage is applied to VDD with the VSS relatively grounded, the RC delay in the ESD detection circuit keeps the gate of Mp1 at a relatively low voltage level compared to the voltage level at VDD. Therefore, the Mp1 can be quickly turned on by the ESD energy to generate the substrate-triggered current into the trigger node (node b) of the SCR device. Finally, the SCR device can be turned on efficiently to discharge ESD current from VDD to VSS. Fig. 3 shows the simulated voltage and substrate-triggered current of the ESD detection circuit under the ESD transition, where a 0-to-5V voltage pulse with a rise time of 10ns is applied to VDD to simulate the ESD fast transient voltage of human body model (HBM) [7]. With a limited voltage height of 5V in the voltage pulse, the voltage transition on each node in the ESD detection circuit can be simulated to check the desired circuit function before device breakdown. With the correct circuit operation in the proposed ESD detection circuit, the SCR device should be triggered on before device breakdown.

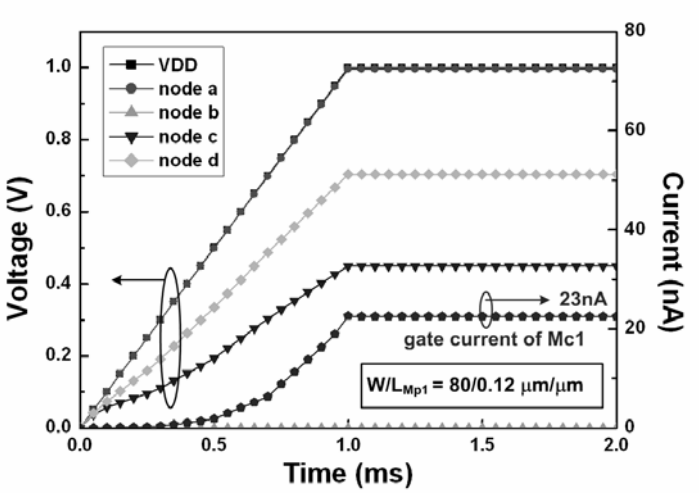

Fig. 2. Hspice-simulated voltage on the nodes of the ESD detection circuit and the gate current flow through the MOS capacitor Mc1 in the proposed low-leakage ESD clamp circuit in a 65-nm CMOS process under the normal power-on condition.

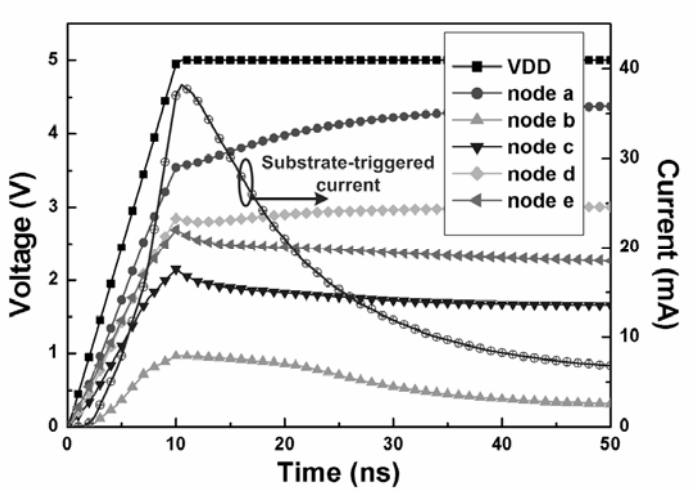

Fig. 3. Hspice-simulated voltages on the nodes of the ESD detection circuit and the substrate-triggered current which flows into the SCR device during 0-to-5V ESD-like transition on VDD.

III. Experimental Results

The new proposed power-rail ESD clamp circuit has been fabricated in a 65-nm CMOS process. All devices used in this design are 1-V fully-silicided devices, including the SCR device. The layout area of the whole ESD clamp circuit (including the SCR width of 45μm) is only 49μm×21μm, and the layout view is shown in Fig. 4. The widths of SCR device as ESD clamping device are varied in 45μm, 60μm, and 90μm in the test chip to verify the corresponding ESD robustness.

A. Turn-on Verificaion

The turn-on behavior of SCR devices is an important index for ESD protection, which had been evaluated in the literature [8], [9]. To verify the turn-on efficiency of the proposed low-leakage ESD clamp circuit, a square-type voltage pulse with a rise time of ~10ns and a pulse height of 5V is used to simulate the rising edge of a positive-to-VSS HBM ESD pulse. When the positive voltage pulse is applied to VDD of the proposed ESD clamp circuit with VSS grounded, the sharp-rising edge of

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the ESD-like voltage pulse will start the ESD detection circuit to generate the substrate-triggered current to trigger on the SCR device, and in turn to provide a low-impedance path between VDD and VSS. The voltage waveform clamped by the ESD clamp circuit on the VDD pad is shown in Fig. 5. The applied 5-V voltage pulse is clamped down quickly to a stable low voltage level (~2V) by the proposed ESD clamp circuit with a SCR device width of 45μm. From the measured voltage waveform, the excellent turn-on efficiency of the proposed ESD clamp circuit during the ESD stress has been successfully verified.

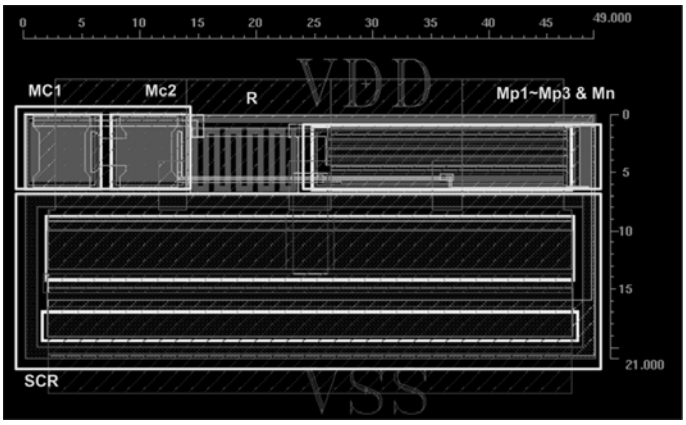

Fig. 4. Layout view of the proposed power-rail ESD clamp circuit. The chip has been fabricated in a 65-nm CMOS process with 1-V devices.

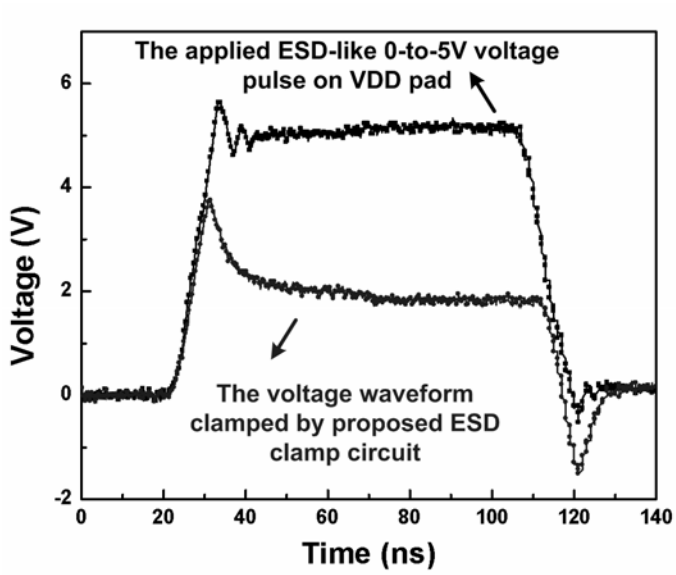

Fig. 5. The measured voltage waveforms clamped by the proposed ESD clamp circuit when a 0-to-5V voltage pulse is applied to VDD pad.

B. ESD Robustness

To investigate the turn-on behavior of the ESD clamping device with ESD detection circuit during ESD stress event, transmission line pulse (TLP) generator with a pulse width of 100ns and a rise time of ~10ns is widely used to measure the second breakdown current (It2) of ESD clamp circuit. The TLP-measured I-V characteristics of the ESD clamp circuit with different widths of SCR device are shown in Fig. 6. The ESD clamp circuit with SCR widths of 45μm, 60μm, and 90μm can achieve It2 of 4.54A, 6.03A, and 9.24A, respectively. Without any triggered current, the original trigger voltage of the SCR device is as high as 11.5V. However, with the proposed ESD detection circuit in this work, the trigger voltage of the SCR device is reduced to only around 3 to 4V. The low trigger voltage and high It2 value of the power-rail ESD clamp circuit can ensure the effective ESD protection capability. The HBM ESD levels and machine-model (MM) [10] ESD levels of the proposed ESD clamp circuit with SCR of different widths under positive-to-VSS ESD stress are listed in Table I. The failure criterion is defined as the I-V characteristic curve shifting over 20% from its original curve after three continuous ESD zaps at every ESD test level. The proposed power-rail ESD clamp circuit with SCR width of only 45μm can achieve 7kV in HBM and 325V in MM ESD tests, respectively. The corresponding second breakdown current (It2) measured by TLP is also listed in Table I.

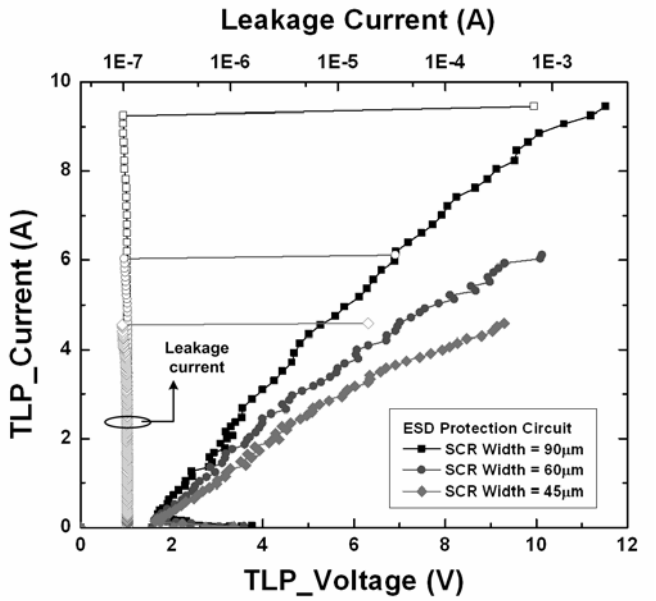

Fig. 6. The TLP-measured I-V characteristics of the proposed power-rail ESD clamp circuit with SCR device of different widths under positive-to-VSS ESD stress.

TABLE I

ESD ROBUSTNESS OF THE PROPOSED POWER-RAIL ESD CLAMP CIRCUIT WITH SCR DEVICE OF DIFFERENT WIDTHS

SCR Width (μm)	It2 (A)	HBM ESD Level (V)	MM ESD Level (V)
45	4.54	7000	325
60	6.03	> 8000	400
90	9.24	> 8000	525

C. Standby Leakage

The standby leakage current of the proposed power-rail ESD clamp circuit is dominated by Mp1 in the ESD detection circuit while the leakage current contributed by the MOS capacitor is only ~23nA from simulation result. Increasing the dimension of Mp1 can improve the turn-on speed of SCR device, but it results in a larger standby leakage current under the normal

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circuit operating condition. The measured results of the standby leakage current and the trigger voltage of the proposed power-rail ESD clamp circuit with different dimensions for Mp1 and SCR device are shown in Fig. 7. The leakage currents between the ESD clamp circuit realized with SCR of 45μm and 90μm are almost the same, because the leakage current generated from SCR device is quite small (less than 1nA at 25°C). While the device dimension of Mp1 is increased, the standby leakage current of the whole power-rail ESD clamp circuit also proportionally increases, but the corresponding trigger voltage of the SCR device can be reduced.

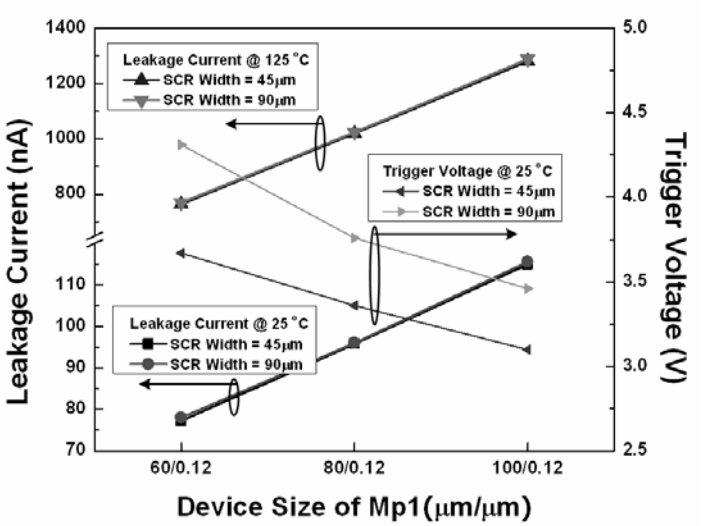

Fig. 7. The dependence of the standby leakage current under 1-V bias of the whole power-rail ESD clamp circuit with SCR device of different widths at different temperatures on the device size of Mp1.

TABLE II

COMPARISON AMONG THE PROPOSED POWER-RAIL ESD CLAMP CIRCUIT AND PRIOR WORKS

	Traditional RC-based ESD protection [4]		Modified ESD clamp circuit with timer level restorer [5]	This work (Fig. 1)
	ESD Detection Circuit Only	With M_{ESD} W = 400μm L = 0.12μm	ESD Detection Circuit Only	ESD Detection Circuit + SCR W_{Mp1} = 80μm W_{SCR} = 45μm
Standby leakage current under 1-V bias at 25°C	2.33 μA	3.74 μA	~1.5 μA (simulation)	96 nA
Standby leakage current under 1-V bias at 125°C	26.9 μA	44.8 μA	n/a	1.02 μA
HBM ESD level	n/a	3250 V	n/a	7000 V

Table II shows the performance comparison among the traditional RC-based power-rail ESD clamp circuit [4], the modified ESD clamp circuit with timer level restorer [5], and the new proposed design of this work. The traditional RC-based power-rail ESD clamp circuit was also fabricated in the same 65-nm CMOS process. The standby leakage currents under 1-V bias of the traditional RC-based ESD clamp circuit with the ESD clamping MOSFET (M_{ESD}) of W/L = 400μm/0.12μm at 25°C and 125°C are as large as 3.74μA and 44.8μA, respectively. Even if the leaky ESD clamping MOSFET is excluded, the standby leakage current of the stand-alone ESD detection circuit is still as large as 26.9μA at 125°C. The standby leakage current of the modified ESD detection circuit with timer level restorer is simulated as around 1.5μA with the appropriate device dimensions under the same bias condition (VDD of 1V with VSS grounded) at 25°C. With consideration of ESD robustness and standby leakage current, the new proposed power-rail ESD clamp circuit with SCR of 45μm and Mp1 of 80μm/0.12μm which achieves overall standby leakage current of only 96nA at 25°C and HBM ESD level of 7kV has performed the excellent ESD solution in a 65-nm fully-silicided CMOS technology.

IV. CONCLUSION

A new power-rail ESD clamp circuit with low standby leakage current and high robust ESD level has been successfully verified in a 65-nm CMOS process. With small active area and high robust ESD level, the proposed power-rail ESD clamp circuit has performed low standby leakage current during normal circuit operating condition, which is an excellent design solution for on-chip ESD protection in nanometer CMOS technologies.

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