Chip-Level and Board-Level CDM ESD Tests on IC Products

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Abstract **- The electrostatic discharge (ESD) transient currents and failure analysis (FA) between chip-level and board-level charged-device-model (CDM) ESD tests are investigated in this work. The discharging current waveforms of three different printed circuit boards (PCBs) are characterized first. Then, the chip-level and board-level CDM ESD tests are performed to an ESD-protected dummy NMOS and a high-speed receiver front-end circuit, respectively. Scanning electron microscope (SEM) failure pictures show that the board-level CDM ESD test causes much severer failure than that caused by the chip-level CDM ESD test.**

I. Introduction

Recently, it was informed from the IC industry that some IC products which already passed the component-level ESD specifications were still damaged by the CDM-like ESD events in the field applications. Besides, it had been reported that the customer-returned ESD damages can be duplicated by the board-level CDM ESD test [1], [2]. Some studies which evaluated the discharging current under different charged board dimensions in the board-level CDM ESD tests for different IC applications had been reported [3]-[5]. Board-level CDM ESD event often causes the ICs to be damaged after the ICs are installed to the circuit boards of electronic systems. For example, board-level CDM ESD events often occur during the module function test on the circuit board of electronic system. Even though the IC has been designed with good chip-level ESD robustness, it could have a reduced ESD level in board-level CDM ESD event. The reason is that the discharging current during the board-level CDM ESD event is significantly higher than that during the chip-level CDM ESD event. The board-level CDM ESD issue becomes more important in the real-world applications of IC products which are fabricated in nanoscale CMOS processes with the much thinner gate oxide.

In this work, three kinds of PCBs are used to compare the equivalent board capacitances, discharging current waveforms, and peak discharging currents under board-level CDM ESD tests. Moreover, a two-layer PCB with FR4 dielectric layer is employed to perform the board-level CDM ESD tests on the test circuits fabricated in a 130-nm CMOS process.

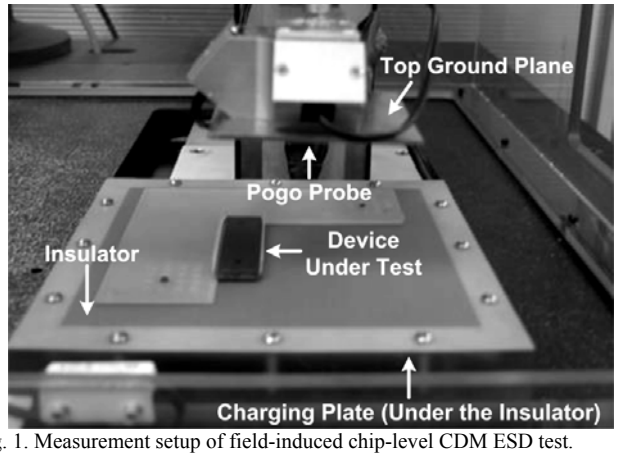


Fig. 1. Measurement setup of field-induced chip-level CDM ESD test.

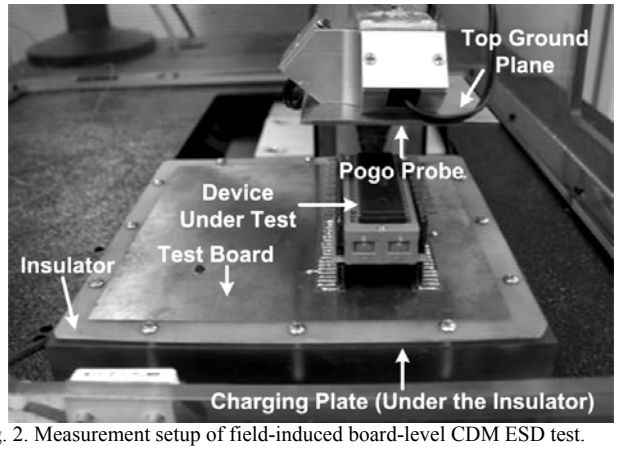


Fig. 2. Measurement setup of field-induced board-level CDM ESD test.

Table 1
Characteristics of Three Different PCBs

	PCB_1		PCB_2		PCB_3	
PCB Type						
PCB Size	12.5 cm x 12.5 cm		15 cm x 15 cm		15 cm x 15 cm	
Board Capacitance	274 pF		324 pF		390 pF	
Charged Voltage	+500 V	+1000 V	+500 V	+1000 V	+500 V	+1000 V
Peak Current	5.71 A	9.16 A	8.65 A	13.8 A	13.41 A	22.96 A

II. Measurement Setup

The experimental setups of chip-level and board-level CDM ESD tests are shown in Figs. 1 and 2, respectively. A CDM ESD test system was used for field-induced chip-level and board-level CDM ESD tests. In the traditional chip-level CDM ESD test, only the IC chip (DUT) is put on the charging plate of the field-induced CDM ESD tester. On the contrary, both the IC chip and the test board on which the IC chip is mounted are put on the charging plate of the field-induced CDM ESD tester in the board-level CDM ESD test. With a 40-pin dual-in-line-package (DIP) socket soldered on the PCB, the packaged test circuit can be mounted on the PCB to perform the board-level CDM ESD test. Three different two-layer PCBs were chosen to investigate their board capacitances, because the board capacitance is a key factor in board-level CDM ESD tests. The characteristics of these three PCBs are listed in Table 1. The board capacitances and discharging current waveforms were monitored by Agilent 4275A LCR meter at 1 MHz and Tektronix 680C oscilloscope, respectively.

III. Experimental Results and Discussion

A. *Board-Level CDM ESD Current Waveforms in Different PCBs*

Table 1 lists the measured board capacitance and peak discharging current among these three PCBs under +500-V and +1000-V charged voltages. Figs. 3, 4, and 5 shows their corresponding discharging current waveforms under +500-V charged voltage. Higher peak currents were observed in PCB_3 due to the largest board capacitance and lowest resistance along the discharging path on PCB. In the board-level CDM ESD tests with IC products, PCB_3 was chosen as the test board.

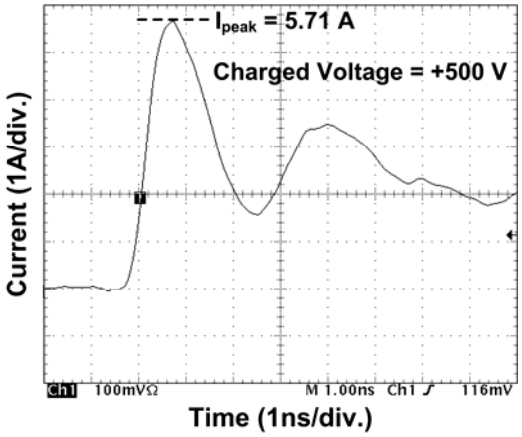


Fig. 3. Discharging current waveform of PCB_1 under +500-V charged voltage.

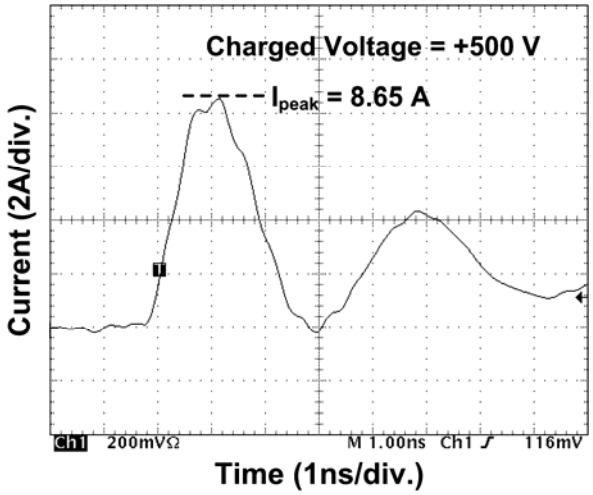


Fig. 4. Discharging current waveform of PCB_2 under +500-V charged voltage.

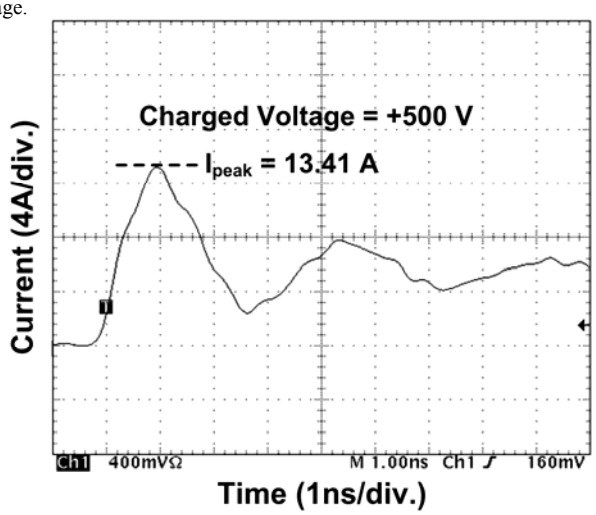


Fig. 5. Discharging current waveform of PCB_3 under +500-V charged voltage.

B. *Test With Dummy Receiver NMOS (RX_NMOS)*

As shown in Fig. 6, the dummy receiver NMOS (RX_NMOS) fabricated in a 130-nm CMOS process was used as the test circuit. The gate terminal of the RX_NMOS is connected to the input pad to emulate the connection of a typical input NMOS in a receiver. The drain, source, and bulk terminals of the RX_NMOS are connected to VSS. On-chip ESD protection circuits are applied in the chip with the RX_NMOS together. The typical double-diode ESD protection scheme is applied to the input pad. The power-rail ESD clamp circuit consists of an RC timer, an inverter, and an ESD clamp NMOS. The equivalent capacitance between the input pad and substrate of the RX_NMOS in the 40-pin DIP package is ~6.8 pF.

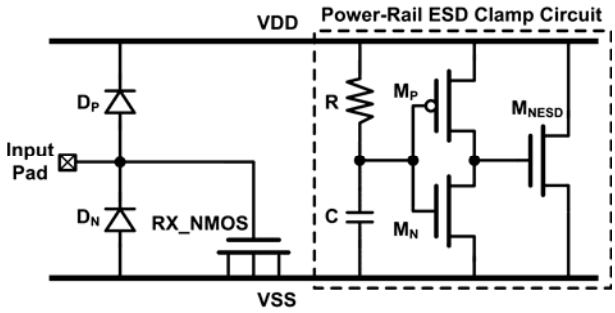
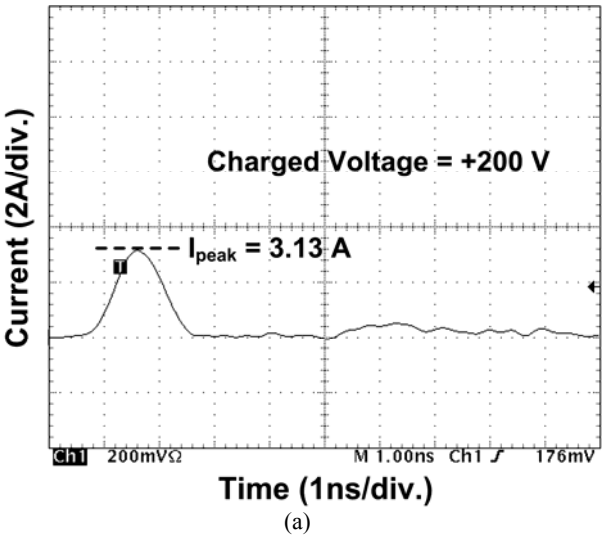
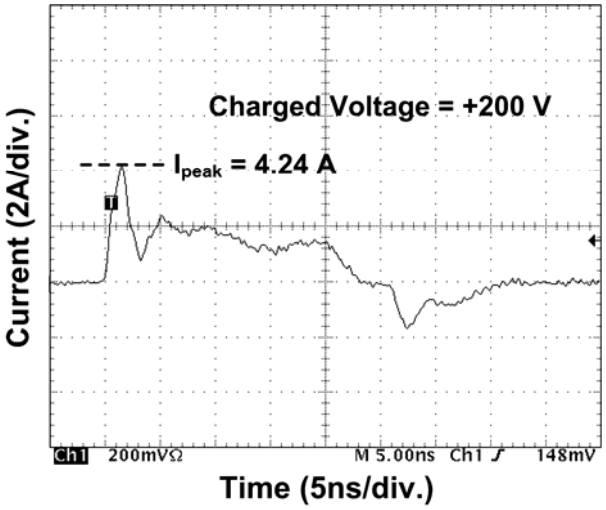


Fig. 6. Test circuit of RX_NMOS (dummy NMOS) for chip- level and board-level CDM ESD tests.

In the board-level CDM ESD test with PCB_3, the bottom layer of PCB_3 was connected to the test system as the charging plate, whereas the top layer was connected to the ground node of the test circuit. The tested pin under CDM ESD tests is the input pad. The discharging current waveforms under +200-V chip-level and +200-V board-level CDM ESD tests are shown in Figs. 7(a) and 7(b), respectively. As compared with the chip-level CDM ESD test, larger charging capacitance exists in the board-level CDM ESD test. Thus, the board-level CDM ESD test has higher peak discharging current, which results in lower ESD robustness of the IC. The peak discharging currents and measured results on the chip-level and board-level CDM ESD robustness of the RX_NMOS are listed in Table 2. The RX_NMOS passes +200-V chip-level CDM ESD test, but fails at +200-V board-level CDM ESD test. This result demonstrates that the board-level CDM ESD robustness is lower than the chip-level CDM ESD robustness, because the board-level CDM ESD event has much larger discharging current than that in the conventional chip-level CDM ESD event.



(a)



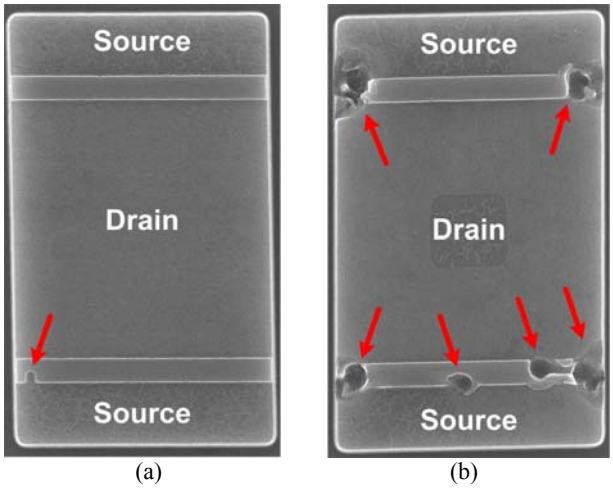
(b)

Fig. 7. Discharging current waveforms of RX_NMOS under (a) +200-V chip-level CDM, and (b) +200-V board-level CDM, ESD tests.

Table 2
Chip-Level CDM and Board-Level CDM ESD Robustness of RX_NMOS

	Charged Voltage	Chip-Level CDM	Board-Level CDM
Peak Current	+100 V	N/A	1.72 A (Pass)
	+150 V	N/A	2.71 A (Pass)
	+200 V	3.13 A (Pass)	4.24 A (Fail)
	+400 V	8.43 A (Fail)	N/A

By using the optical beam induced resistance (OBIRCH) detection, the failure sites caused by CDM ESD was detected and located at the gate of the RX_NMOS. Fig. 8 shows the SEM failure pictures. The test samples were de-layered to the substrate layer so the damages at the gate oxide can be clearly observed. Comparing to Figs. 8(a) and 8(b), the ESD damage caused by board-level CDM ESD event is much worse than that caused by the chip-level CDM ESD event, because the board-level CDM ESD event has much higher discharging energy than that of chip-level CDM ESD event under the same charged voltage.



(a) (b)

Fig. 8. SEM failure pictures of gate oxide damages at RX_NMOS after (a) chip-level CDM, and (b) board-level CDM, ESD tests.

C. *Test With 2.5-GHz High-Speed Receiver Interface Circuit*

A 2.5-GHz differential high-speed receiver interface circuit fabricated in a 0.13-μm CMOS process was also verified with the chip-level and board-level CDM ESD tests. Fig. 9 shows the circuit schematic of the 2.5-GHz differential high-speed receiver interface circuit with on-chip ESD protection design. The differential receiver interface circuit has the differential input stage realized by MOS transistors. The double-diode ESD protection scheme is applied to each differential input pad, and the P-type substrate-triggered silicon-controlled rectifier (P-STSCR) [6] is used in the power-rail ESD clamp circuit. Because of the high-speed application, the dimensions of ESD diodes under the input pads are limited to reduce the parasitic capacitance at the pads. The equivalent capacitance between the Vin_1 pad and the substrate of the ESD-protected 2.5-GHz differential high-speed receiver interface circuit in a 40-pin DIP package is ~5.4 pF. Besides, a reference high-speed receiver interface circuit without on-chip ESD protection circuit was also fabricated in the same process to compare their ESD robustness.

The tested pin under CDM ESD tests is the Vin_1 pad. The measured chip-level and board-level CDM ESD levels of the 2.5-GHz high-speed receiver circuits with and without on-chip ESD protection circuits are listed in Tables 3 and 4, respectively. The chip-level and board-level CDM ESD levels of the reference high-speed receiver interface circuit are quite poor, which fail at ±100 V and ±50 V, respectively. With the on-chip ESD protection circuits, the failure voltages of the high-speed receiver circuit during chip-level and board-level CDM ESD tests can be greatly improved to -1300 V and -900 V, respectively. Similarly, the board-level CDM ESD level is lower than the chip-level CDM ESD level. Failure analysis was performed on the ESD-protected high-speed receiver interface circuits after -1300-V chip-level CDM ESD test and -900-V board-level CDM ESD test.

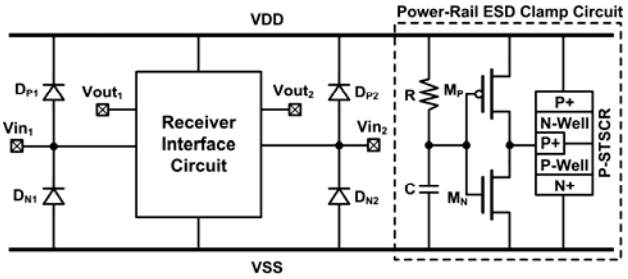


Fig. 9. Test circuit of 2.5-GHz high-speed receiver interface circuit for chip-level and board-level CDM ESD tests.

Table 3
Chip-Level CDM ESD Robustness of 2.5-GHz High-Speed Receiver Interface Circuit

	Without ESD Protection		With ESD Protection	
Polarity	+	-	+	-
Failure Voltage	100 V	100 V	2000 V	1300 V

Table 4
Board-Level CDM ESD Robustness of 2.5-GHz High-Speed Receiver Interface Circuit

	Without ESD Protection		With ESD Protection	
Polarity	+	-	+	-
Failure Voltage	50 V	50 V	1300 V	900 V

The SEM failure pictures after chip-level and board-level CDM ESD tests are shown in Figs. 10 and 11, respectively. The failure points are located at the P+/N-well ESD diode D_{P1}. Although the ESD protection devices are successfully turned on during CDM ESD tests, the huge current during CDM ESD tests still damages the ESD protection devices. According to the SEM failure pictures, the failure is much worse after board-level CDM ESD test than that after chip-level CDM ESD test. This result has confirmed again that board-level CDM ESD events are more critical than chip-level CDM ESD events.

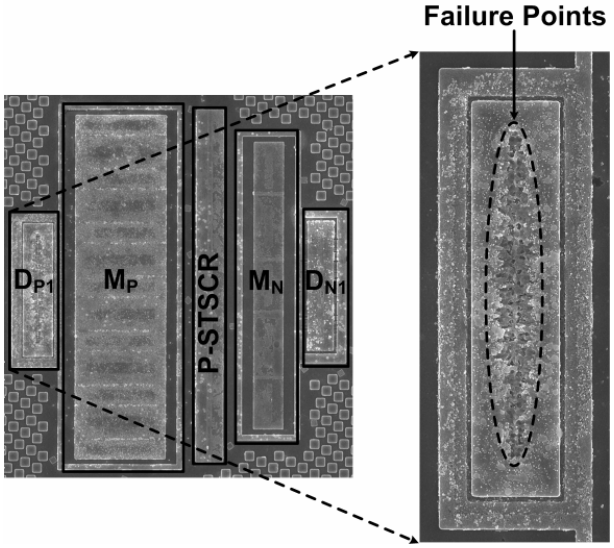


Fig. 10. SEM failure picture of the failure points on 2.5-GHz high-speed receiver front-end circuit after -1300-V chip-level CDM ESD test.

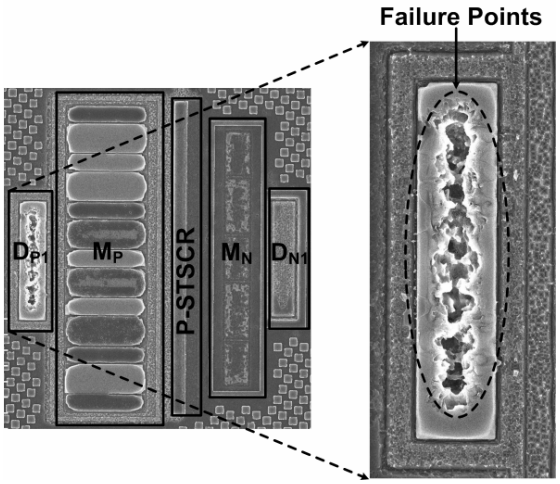


Fig. 11. SEM failure picture of the failure points on 2.5-GHz high-speed receiver front-end circuit after -900-V board-level CDM ESD test.

IV. CONCLUSION

Since the board capacitance is much larger than the IC chip

capacitance, the board-level CDM ESD event has higher discharging energy than that of chip-level CDM ESD event. Thus, the board-level CDM ESD robustness is lower than the chip-level CDM ESD robustness. Failure analysis on the IC samples shows that ESD damage caused by board-level CDM ESD is much worse than that caused by chip-level CDM ESD. This result indicates that the board-level CDM ESD event is more critical than the chip-level CDM ESD event to IC products in field applications. The test standard on board-level CDM ESD event should be established for IC industry to verify ESD robustness of their IC products in real-world applications.

ACKNOWLEDGEMENTS

This work was partially supported by Materials Analysis Technology Inc., Hsinchu, Taiwan, and partially supported by Ministry of Economic Affairs, Taiwan, under Grant 97-EC-17-A-01-S1-104.

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