Source-Side Engineering to Increase Holding Voltage of LDMOS in a 0.5-m 16-V BCD Technology to Avoid Latch-up Failure

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Abstract **- To avoid latch-up failure in high voltage integrated circuits, a source-side engineering technique for on-chip ESD protection nLDMOS is proposed in this work. Experimental results have been verified in a 0.5-μm 16-V bipolar CMOS DMOS technology. Measurement results from transmission-line-pulsing system show that the proposed source-side engineering method can effectively increase the holding voltage of the nLDMOS from 10.5V to 16.2V. Transient-induced latch-up tests show that the proposed source-side engineering technique significantly improves the latch-up immunity of nLDMOS in on-chip ESD protection circuit.**

I. INTRODUCTION

Electrostatic discharge (ESD) is an inevitable event during fabrication, packaging and testing processes of integrated circuits (ICs). ESD protection design is therefore necessary to protect ICs from being damaged by ESD stress energies. Since most of the ESD protection devices protect the internal circuits through the action of inherent bipolar junction transistors (BJTs), ESD devices are kept off until the voltage exceeds its BJT trigger voltage (V_{t1}). As long as the ESD device is triggered-on, the ESD voltage is clamped down to protect internal circuit from being damaged by the ESD energy. As a result, V_{t1} of the ESD protection device should be smaller than both junction and gate oxide breakdown voltages of internal circuits ($V_{BD,Internal}$). This ensures that the ESD protection device can protect the internal circuit effectively.

Although the ESD protection device can clamp down the ESD transient voltage and protect the internal circuits, the snapback holding voltage (V_h) smaller than power supply voltage (V_{DD}) can result in the latch-up issue [1]. The latch-up issue can arise from the mis-triggering of ESD protection devices under normal circuit operation [2]. As a result, to ensure the reliability and effectiveness of an ESD protection design, it is generally approved that the I-V characteristics of an ESD protection device should locate within the ESD protection window. As depicted in Fig. 1, V_{t1} of ESD protection devices should be smaller than $V_{BD,Internal}$ to ensure successful protection, and V_h of ESD protection devices should be higher than V_{DD} to accomplish a latch-up free design.

With the power supply voltage over ten volts or even higher, holding voltage of ESD protection devices in high-voltage (HV) ICs is usually lower than the V_{DD} voltage. Moreover, huge noise generated from large switching current, harsh operating environment, electromagnetic disturbance …and so on makes latch-up easily happen in HV ICs [3]. Accordingly, latch-up has become one of the main concerns in HV technologies. Because latch-up usually causes devastating results to ICs and electronic systems, it is important from the viewpoint of reliability to improve the latch-up immunity of on-chip devices. One of the most effective methods to prevent latch-up is to increase the holding voltage of devices that are directly connected between the power supply and ground lines, such as on-chip ESD protection devices [3], [4].

To increase the holding voltage of HV devices, the stacked configuration has been reported to be an effective method [3]. However, this technique consumes large silicon area in exchange of higher latch-up immunity. Moreover, the stacked configuration needs additional trigger circuit to reduce the bipolar trigger voltage (V_{t1}) of the stacked ESD protection devices. As a result, method to increase the latch-up immunity of HV devices without substantial increase on the occupied silicon area is a valuable technique in the aspect of reliability design.

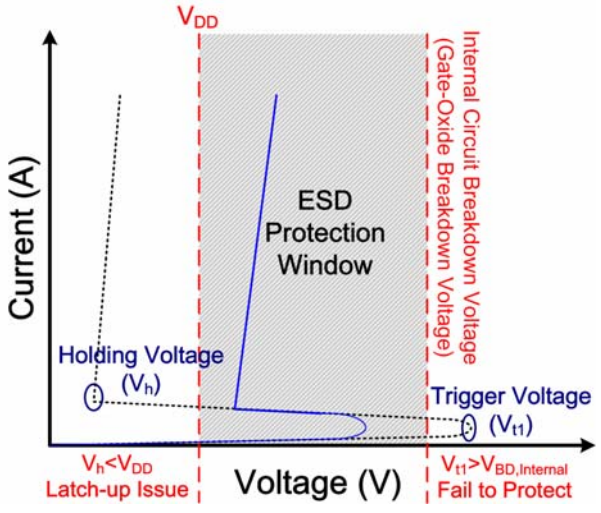

Fig. 1. Typical device I-V curve showing the ESD protection window of ESD protection devices.

II. Holding Voltage of Lateral DMOS in High-Voltage Technologies

In high-voltage technologies, in order to sustain the high V_{DD} voltage during normal circuit operating condition, the complexity of device structure is therefore increased and strongly influences the mechanism of ESD protection devices under high current injection [5], [6]. Fig. 2 shows the device cross-sectional view of the 16-V n-channel lateral DMOS (nLDMOS) in this work. The PBI layer under the source side is an optional P-type boron implant layer, and the n-p-n bipolar junction transistor is formed through (N+/NDD/HV N-Well)—(P-Body/PBI)—(N+). Under high current injection, the kirk effect is known to induce impact ionization at the drain side [7]. Due to the large extended depletion region toward drain region under high current injection, nearly all the electrons ejected from N+ implant at source side can be swept to the drain side without being recombined. These ejected electrons from source side can enter the avalanche region at drain side, and help the multiplication process of electron-hole pair generation [6]. As a result, the electron density ejected from source side is one import factor that affects the snapback holding voltage of nLDMOS.

To modulate the electron density ejected from source side under high current injection, and to increase the holding voltage of nLDMOS, a source-side engineering method is proposed in this work. Three different structures of nLDMOS to the influence of holding voltage were studied. Devices were fabricated in a 0.5- m 16-V bipolar CMOS DMOS (BCD) process.

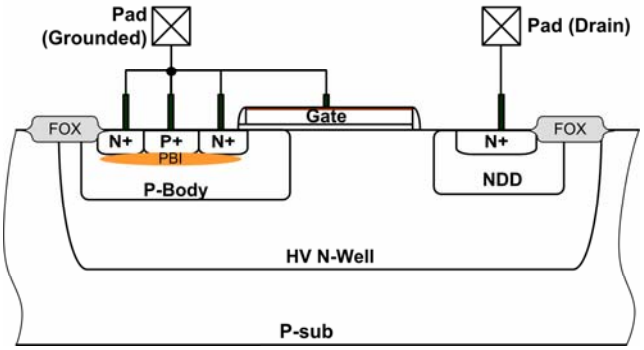

Fig. 2. Device cross-sectional view of nLDMOS in a 0.5- m 16-V BCD process.

III. Device Structures

To sustain the high V_{DD} voltage without inducing device breakdown, the nLDMOS is surrounded by the HV N-Well, as shown in Fig. 2. As a result, P+ pick-up is needed for every source finger of the nLDMOS to control the body bias. Layout top view of a traditional nLDMOS in the 0.5-μm 16-V BCD process is shown in Fig. 3(a). The traditional nLDMOS shown in Fig. 3(a) does not have PBI layer and is labeled as type A in this work. To reduce the ejected electrons from source side and increase the holding voltage of nLDMOS, nLDMOS with type-B structure has interleaved N+ source implant, as shown in

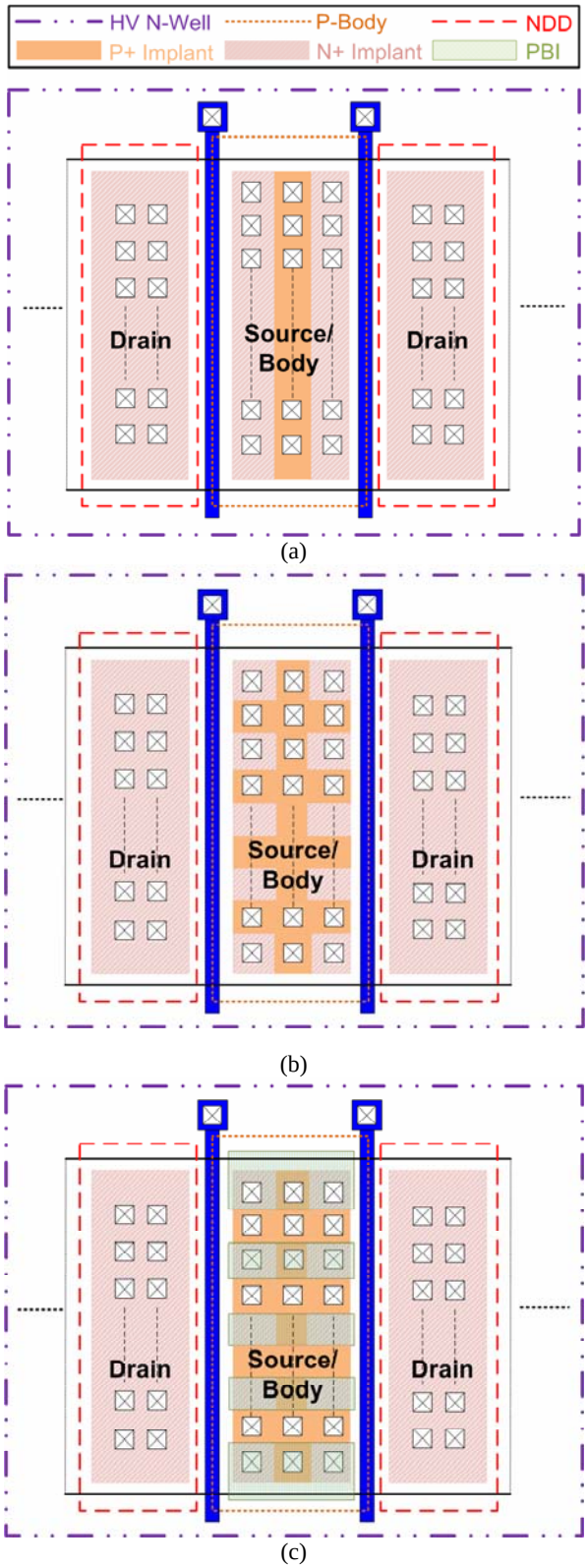

Fig. 3. Layout top view of nLDMOS with (a) type-A, (b) type-B, and (c) type-C, device structure in this work.

Fig. 3(b), where half the N+ implant on every two source-side contacts is replaced by P+ implant. No PBI layer was drawn in the type-B nLDMOS device structure. The nLDMOS with type-C device structure have interleaved N+ source implant and interleaved PBI, which is drawn to cover all N+ implant at source side, as shown in Fig. 3(c).

IV. Experimental Results

A. Measurement on Transmission-Line-Pulsing System

Device characteristics of the three types of nLDMOS under ESD stress conditions were measured by transmission-line-pulsing (TLP) system [8]. Gate of the nLDMOS devices were grounded during TLP measurements. As shown in Fig. 4, traditional nLDMOS with type-A structure has TLP-measured holding voltage of 10.5V. With the reduced overall source-side N+ area, nLDMOS with type-B structure exhibits higher TLP-measured holding voltage than that of nLDMOS with type-A structure (12.7V versus 10.5V). With the PBI layer underneath the N+ source to recombine the ejected electrons, TLP-measured holding voltage of nLDMOS with type-C structure is further increased to 16.2V. From the measurement results, source-side engineering method can effectively increase the TLP-measured holding voltage of nLDMOS.

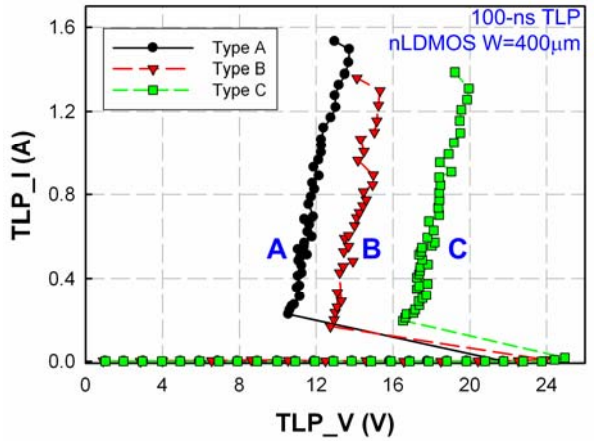

Fig. 4. TLP measured I-V curves of the type-A, type-B, and type-C nLDMOS structures.

B. Transient-Induced Latch-Up Test

Though the higher holding voltage of nLDMOS measured from TLP system infers that the higher transient energy across the nLDMOS is required to trigger on the inherent bipolar junction transistor, self-heating of HV devices has been reported to result in the lower DC-measured holding voltage compared to the TLP-measured holding voltage [9], [10]. As a result, to evaluate the latch-up susceptibility of nLDMOS with the source-side engineering technique, the three types of nLDMOS were evaluated by using the transient-induced latch-up (TLU) test [2]. TLU measurement setup in this work is depicted in Fig. 5. The nLDMOS was biased under the circuit operating voltage with power supply voltage of 16V. A 200-pF capacitor was used to store charges as the TLU-triggering source with the voltage of V_{charge}. After switching the relay, the stored charges were discharged to the device under test (DUT), resulting in the sinusoidal damping voltage across the nLDMOS to simulate the power-supply voltage with external noise disturbance during normal circuit operating conditions [11]. By monitoring the change on voltage and current waveforms after transient trigger, TLU measurement can effectively judge the latch-up immunity of the DUT.

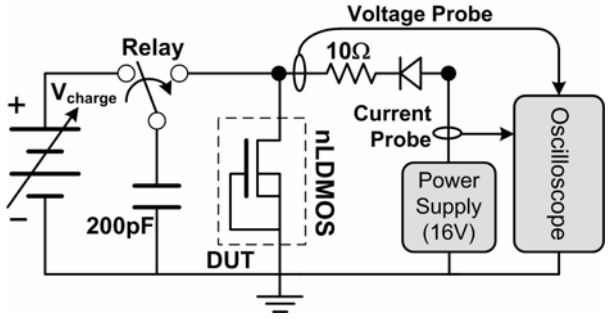

Fig. 5. Measurement setup for transient-induced latch-up (TLU) test.

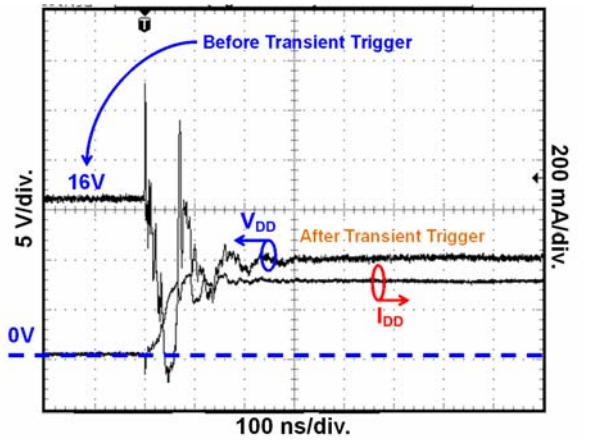

Fig. 6. Transient-induced latch-up test for the nLDMOS with type-A structure and V_{charge} of +25V.

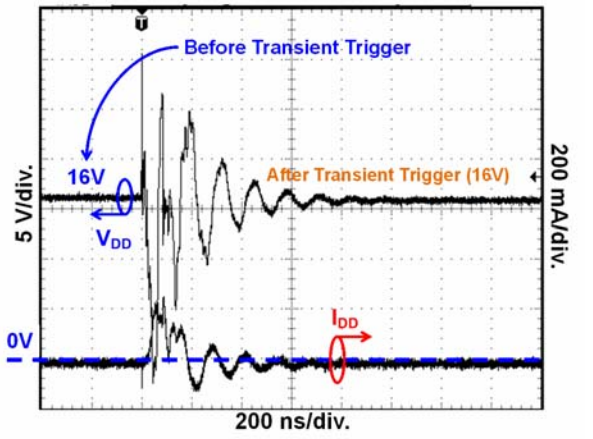

Fig. 7. Transient-induced latch-up test for the nLDMOS with type-C structure and V_{charge} of +50V.

TLU measurement result of the nLDMOS with type-A structure is shown in Fig. 6. With the V_{charge} of +25V, type-A nLDMOS enters latch-up state after transient trigger. In Fig. 6, an increase in power supply current (I_{DD}) and the clamp down of V_{DD} voltage were observed. For the nLDMOS with type-C structure, neither drop on V_{DD} voltage nor increase on power supply current is observed even when the V_{charge} voltage is increased from +25V to +50V, as the measured voltage and current waveforms shown in Fig. 7. The measured minimum positive V_{charge} voltages to induce TLU on nLDMOS of type A, B, and C are summarized in Fig. 8. With the interleaved N+ implant on source side, the measured V_{charge} to induce TLU on the nLDMOS of type B is increased from +25V to +38V. With the help of PBI layer, the measured V_{charge} to induce TLU on the nLDMOS of type C is +56V, which is more than two times compared to the minimum V_{charge} to induce TLU on nLDMOS of type A. As a result, measurement results indicate that source-side engineering technique can effectively improve the latch-up immunity of nLDMOS without increasing the layout area.

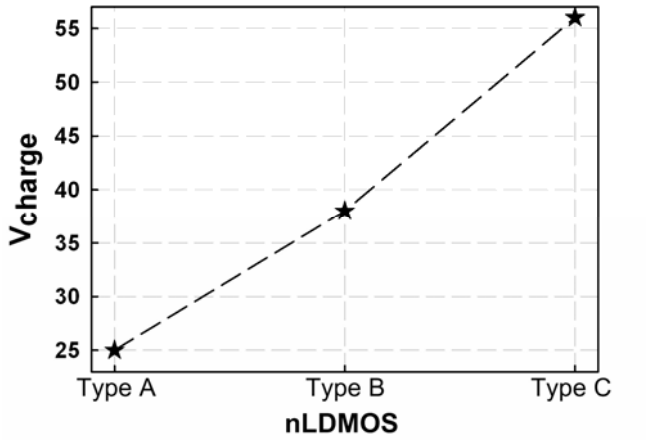

Fig. 8. The measured minimum V_{charge} voltages to induce TLU on nLDMOS of different types.

V. Conclusion

nLDMOS devices with source-side engineering have been studied in this work to increase the holding voltage and to improve the latch-up immunity of nLDMOS. Through reducing the overall source-side N+ area and introducing an additional PBI layer underneath the source-side N+ region, the TLP-measured holding voltage of 16-V nLDMOS is substantially increased from 10.5V to 16.2V. TLU measurement results verify that the source-side engineering method can effectively increase the latch-up immunity of 16-V nLDMOS. Therefore, nLDMOS with the proposed source-side engineering technique is a useful structure for HV integrated circuits to improve latch-up immunity among the nLDMOS in the on-chip ESD protection circuits.

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