Ultra-Low-Leakage Power-Rail ESD Clamp Circuit in Nanoscale Low-Voltage CMOS Process

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***Abstract*—A new power-rail ESD clamp circuit with ultra-low-leakage design is presented and verified in a 65-nm CMOS process with a leakage current of only 116nA at 25°C, which is much smaller than that (613μA) of traditional design. Moreover, it can achieve ESD robustness of over 8kV in HBM and 800V in MM ESD tests, respectively.**

Keywords — electrostatic discharge (ESD); ESD clamp circuit; gate leakage; silicon-controlled rectifier (SCR).

I. INTRODUCTION

The power-rail ESD clamp circuit plays an important role in on-chip electrostatic discharge (ESD) protection design. Traditional power-rail ESD clamp circuit was often realized with the RC-based ESD detection circuit and the ESD clamp device [1], which was designed to provide discharging current path between VDD and VSS during ESD stresses and to be kept off under normal power-on conditions. With the consideration of area efficiency, the capacitor in the ESD-detection circuit was often realized by the MOS capacitor, because the MOS capacitor has the largest capacitance per unit area in baseline CMOS processes. In nanoscale CMOS technology, the gate oxide thickness becomes thinner, which makes gate-tunneling issue more serious. The gate leakage current in MOS transistor had been investigated and modeled for HSPICE simulation [2], [3]. With such a large gate leakage current, the power-rail ESD clamp circuit with a large MOS capacitor in the ESD detection circuit will cause huge leakage under power-on condition [4].

In this work, a new power-rail ESD clamp circuit designed with the consideration of gate leakage issue has been proposed and successfully verified in a 65-nm CMOS process with a ultra-low-leakage standby current under power-on condition.

II. IMPACTS OF GATE LEAKAGE IN POWER-RAIL ESD CLAMP CIRCUIT

The gate leakage in the nanoscale CMOS process causes the leakage current through the MOS capacitor, which in turn introduces more circuit leakage paths in the power-rail ESD clamp circuit. The power-rail ESD clamp circuit with the traditional RC-based ESD detection circuit and the silicon-controlled rectifier (SCR) as main ESD clamp device for 1-V application in a 65-nm CMOS process is shown in Fig. 1(a). Due to the gate leakage of the MOS capacitor, the PMOS (M_{P1}) in the ESD detection circuit cannot be fully turned off, which causes another circuit leakage path under normal circuit operating conditions. If the ESD clamp device is realized with an NMOS, the ESD clamp NMOS will leak more current, because its gate voltage cannot be fully biased to VSS under normal circuit operating conditions. Some previous works had addressed this leakage issue, and the modified design to reduce the leakage current by adding the PMOS restorer (M_{PR}) in the ESD detection circuit is shown in Fig. 1(b) [4], [5]. However, the MOS capacitor in the ESD detection circuit always conducts some leakage current in the nanoscale CMOS process, because there is a voltage drop across it under the normal circuit operating conditions.

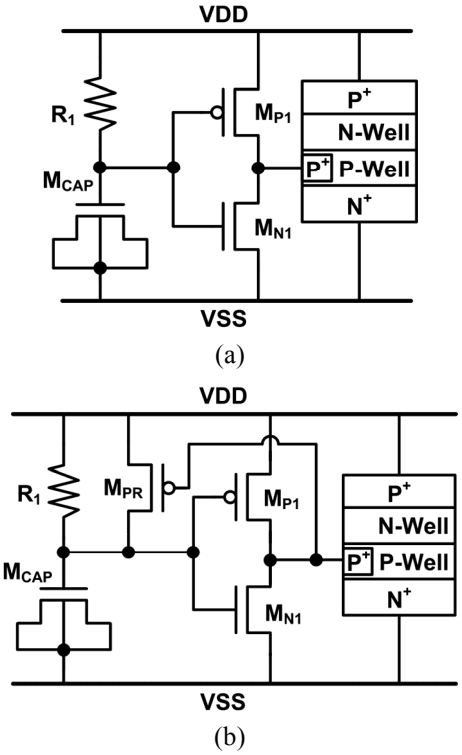


Figure 1. (a) Power-rail ESD clamp circuit with the traditional RC-based ESD detection circuit, and (b) modified power-rail ESD clamp circuit with an additional restorer.

III. NEW PROPOSED POWER-RAIL ESD CLAMP CIRCUIT

Fig. 2 shows the new proposed power-rail ESD clamp circuit with ultra-low-leakage design, which consists of the new ESD detection circuit and the substrate-triggered silicon-controlled rectifier (STSCR) as the ESD clamp device. In the new proposed power-rail ESD clamp circuit, the RC-based ESD detection circuit and the feedback control inverter are combined, where the MOS capacitor (M_{CAP}) is connected between the V_A and V_B nodes. Because M_{CAP} is not directly connected to VSS, no direct leakage path is formed through the large-sized MOS capacitor to ground under normal circuit

operating conditions. To avoid another gate leakage current path through the large ESD clamp NMOS, the ESD clamp device is replaced by the STSCR. Without the thin gate-oxide structure, SCR has very low leakage current under normal circuit operating conditions. Besides, SCR had been proven to have the highest ESD robustness under the smallest device size [6].

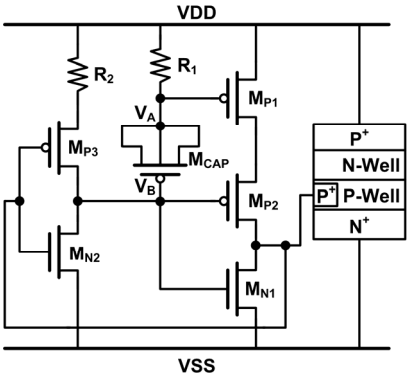


Figure 2. New proposed power-rail ESD clamp circuit with ultra-low-leakage design.

A. Operation Under Normal Circuit Operating Conditions

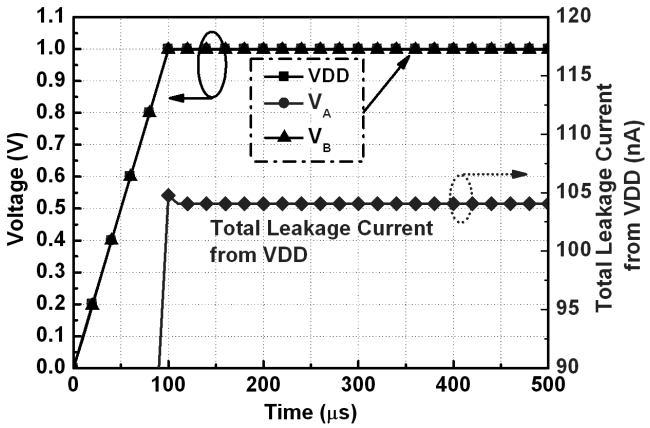
During VDD power-on transition, the rise time of power-on transient voltage is in the order of millisecond (ms). In the new proposed power-rail ESD clamp circuit shown in Fig. 2, the RC time constant is designed in the order of microsecond (μs). With such a slow rise time of the normal power-on transition, the voltage levels at V_A and V_B can follow up the VDD voltage in time to keep M_{P1} and M_{P2} off. Moreover, M_{N1} is turned on because its gate terminal is connected to V_B. Through the feedback path, M_{N2} can be turned off, and M_{P3} can be turned on to fully charge the voltage at V_A and V_B to VDD. So, there is no voltage drop across M_{CAP} and no circuit leakage path exists in the ESD detection circuit.

Without voltage drop across the M_{CAP} under normal circuit operating conditions, M_{CAP} can be realized with large device size without causing leakage current. Since V_A and V_B are charged to VDD, M_{P1} and M_{P2} can be fully turned off. No trigger current is injected into STSCR. Therefore, STSCR can be kept off under normal circuit operating conditions. Fig. 3(a) shows the simulated transient waveforms of the new ESD detection circuit under normal power-on transition with a rise time of 0.1ms. With the power-supply voltage of 1 V, the simulated overall leakage current of the power-rail ESD clamp circuit is only about 104 nA at 25 °C.

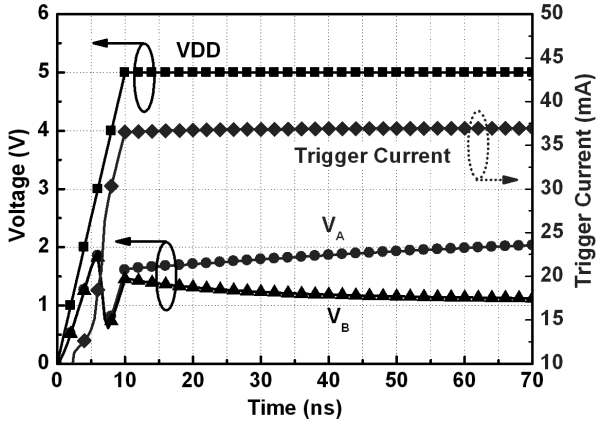
B. Operation Under ESD-Stress Conditions

When ESD is zapping to VDD with VSS grounded, due to its fast rise time (in the order of nanosecond), the voltage levels at node V_A and V_B are initially kept at VSS. Therefore, M_{P1} and M_{P2} are initially turned on to conduct trigger current to turn on the STSCR. Moreover, M_{N2} is turned on by the feedback path, which further keeps the node V_B voltage near to VSS. Due to the leaky M_{CAP}, the voltage at V_A can be continually kept in low voltage level, which in turn keeps M_{P1} and M_{P2} on to conduct trigger current into STSCR. Consequently, the turned-on STSCR provides a low-impedance path to discharge ESD current from VDD to VSS.

With the leaky MOS capacitor in the ESD detection circuit, the new proposed circuit can continually provide the trigger current into the STSCR. By such circuit arrangement, the leakage current of the leaky MOS capacitor becomes the advantage of the ESD detection circuit. Fig. 3(b) shows the simulated voltage transient waveforms and the trigger current generated from the new proposed ESD detection circuit, when a 0-to-5V voltage ramp with a rise time of 10ns is applied to VDD, which is used to simulate the fast rising edge of a HBM ESD pulse before MOS junction breakdown in the circuit. The new proposed ESD detection circuit successfully injects the trigger current into the STSCR. With a 100-Ω resister connected between the trigger node and VSS to model the substrate resistance of the STSCR, the simulated trigger current is about 37 mA, which is large enough to turn on the STSCR.



(a)



(b)

Figure 3. Simulated transient waveforms of the new proposed ESD detection circuit under (a) normal power-on transition with a rise time of 0.1ms, and (b) ESD-stress condition with a rise time of 10ns.

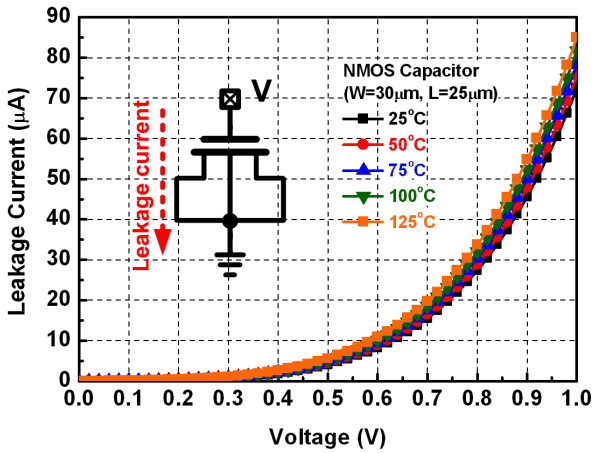
IV. EXPERIMENTAL RESULTS

The new proposed power-rail ESD clamp circuit and two prior designs have been fabricated in a 65-nm CMOS process.

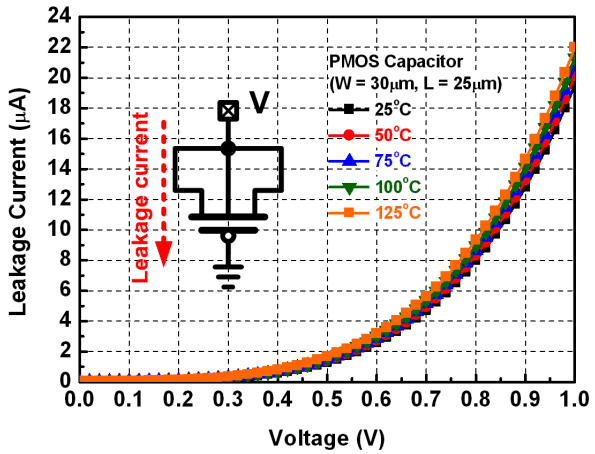
Since the MOS capacitor is connected to VSS in Figs. 1(a) and 1(b), the NMOS capacitor is used in the traditional power-rail ESD clamp circuit and the modified design with the PMOS restorer. However, the PMOS capacitor is used in the new proposed power-rail ESD clamp circuit because the PMOS capacitor is not connected to VSS. The device dimensions used in the prior designs and the new proposed power-rail ESD clamp circuits are listed in Table I. All of the power-rail ESD clamp circuits implemented in this work use the same STSCR with identical device layout and dimension.

TABLE I. DEVICE DIMENSIONS IN POWER-RAIL ESD CLAMP CIRCUITS

Device Dimensions	R1 (Ω)	M_{CAP} (W/L)	M_{P1} (W/L)	M_{N1} (W/L)	M_{P2} (W/L)	SCR (WxLxM)
Traditional Design	20kΩ	30μm / 25μm	100μm / 0.15μm	5μm / 0.15μm		60μmx3.9μmx2
Modified Design With Restorer	20kΩ	30μm / 25μm	100μm / 0.15μm	5μm / 0.15μm		60μmx3.9μmx2
New Proposed Design (This Work)	20kΩ	30μm / 25μm	100μm / 0.15μm	5μm / 0.15μm	100μm / 0.15μm	60μmx3.9μmx2



(a)

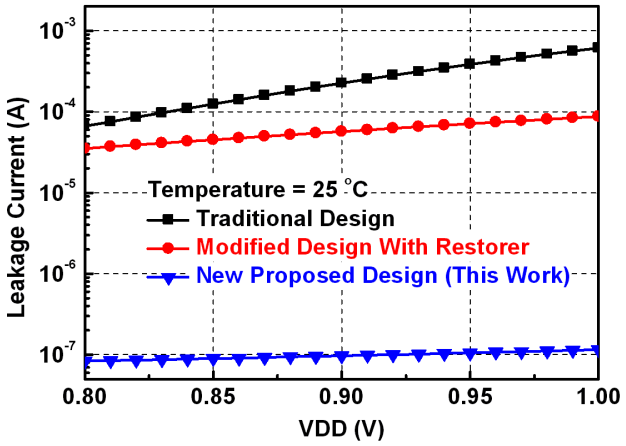


(b)

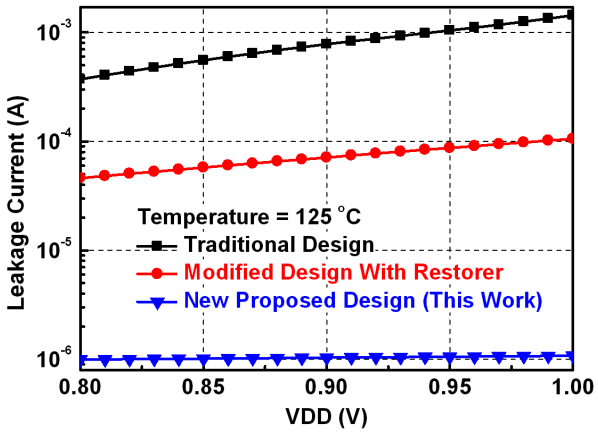
Figure 4. Measured leakage currents of stand-alone (a) NMOS capacitor, and (b) PMOS capacitor, at different temperatures.

Figs. 4(a) and 4(b) show the measured leakage currents of the stand-alone NMOS and PMOS capacitors (W=30μm, L=25μm) with gate-oxide thickness of ~16Å in a 65-nm CMOS process, respectively. Under 1-V bias, the gate leakage current of PMOS capacitor (NMOS capacitor) at 125°C is as high as 22μA (85μA).

The leakage currents among three fabricated power-rail ESD clamp circuits under different VDD voltages at 25°C and 125°C are compared in Figs. 5(a) and 5(b), respectively. The leakage currents under 1-V VDD voltage are listed in Table II. Compared with the leakage current of the stand-alone MOS capacitor, much larger leakage current is observed in the traditional design, which implies that the leaky MOS capacitor causes other circuit leakage path in the ESD detection circuit. Although the leakage current is reduced by adding the restorer into the modified design in Fig. 1(b), it still has a leakage current of as high as 88μA under 1-V VDD bias at 25°C. On the contrary, the new proposed design (this work) has the lowest leakage current of only 116nA (1.08μA) under 1-V VDD bias at 25°C (125°C).



(a)



(b)

Figure 5. Comparison of measured leakage currents at different VDD biases among the prior designs and the new proposed power-rail ESD clamp circuits at (a) 25°C and (b) 125°C.

The leakage currents among these three power-rail ESD clamp circuits under VDD of 1 V at different temperatures are compared in Fig. 6. From 25 °C to 125 °C, the leakage current of the new proposed design is two-order smaller than that of the traditional design or the modified design with restorer.

TABLE II. MEASURED LEAKAGE CURRENTS OF POWER-RAIL ESD CLAMP CIRCUITS UNDER 1-V VDD BAIS

Leakage Current at VDD = 1V	25 °C	125 °C
Traditional Design	613 μA	1.43 mA
Modified Design With Restorer	88 μA	106 μA
New Proposed Design (This Work)	116 nA	1.08 μA

TABLE III. HBM AND MM ESD ROBUSTNESS OF POWER-RAIL ESD CLAMP CIRCUITS

ESD Robustness	HBM	MM
Traditional Design	6 kV	600 V
Modified Design With Restorer	> 8 kV	750 V
New Proposed Design (This Work)	> 8 kV	800 V

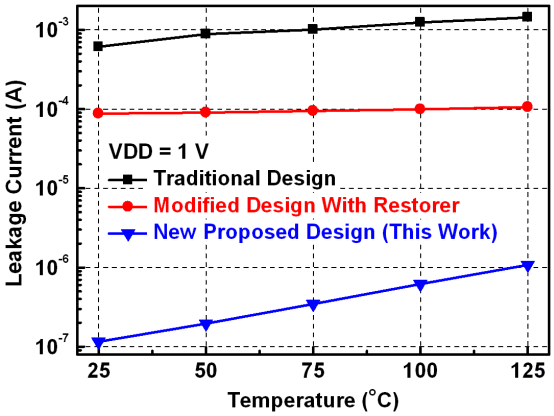


Figure 6. Comparison of measured leakage currents at VDD of 1V among the prior designs and the new proposed power-rail ESD clamp circuits at different temperatures.

To verify the turn-on speed of these three fabricated power-rail ESD clamp circuits, a voltage pulse with fast rise time is applied to the VDD node to emulate the ESD-like stress. When a 5-V ESD-like voltage pulse with 2-ns rise time and 100-ns pulse width is applied to VDD with VSS grounded, the ESD detection circuit starts to inject the trigger current to turn on the STSCR. The turned-on STSCR provides a low-impedance path between VDD and VSS to clamp the voltage level at VDD. The new proposed power-rail ESD clamp circuit can rapidly clamp the voltage level to around 2 V within 5 ns, as shown in Fig. 7. With low enough clamped voltage level, the internal circuits can be well protected by the new proposed power-rail ESD clamp circuit under ESD-stress conditions. In addition, with the holding voltage of ~2 V, the STSCR does not suffer latch-up trouble in 1-V IC applications.

The human-body-model (HBM) and machine-model (MM) ESD robustness among these three designs are listed in Table III. The new proposed design has the best ESD level of over 8kV in HBM and 800V in MM ESD tests, respectively.

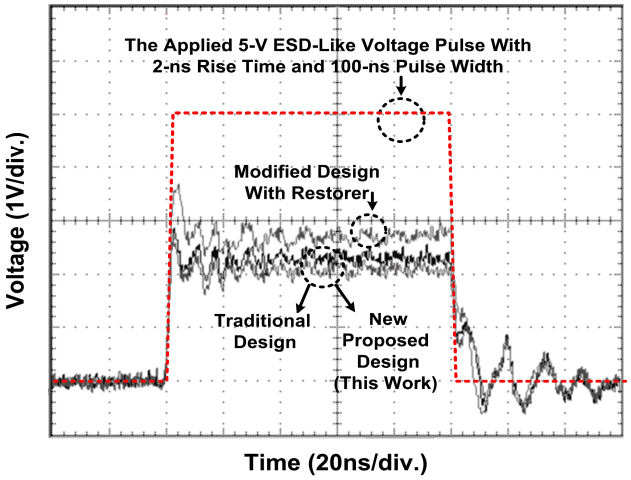


Figure 7. Comparison of the turn-on efficiency among the fabricated power-rail ESD clamp circuits when a 0-to-5V ESD-like voltage pulse with a rise time of 2ns and a pulse width of 100ns is applied to VDD.

V. CONCLUSION

A new power-rail ESD clamp circuit designed with the consideration of gate leakage issue has been proposed and successfully verified in a 65-nm CMOS process with only thin-oxide devices. The leakage currents of the new proposed power-rail ESD clamp circuit are only 116 nA and 1.08 μA at 25 °C and 125 °C, respectively. In addition, the new proposed power-rail ESD clamp circuit achieves the ESD robustness of over 8 kV in HBM and 800 V in MM ESD tests, respectively. With very low leakage current and high ESD robustness, the proposed power-rail ESD clamp circuit is very suitable for whole-chip ESD protection design in IC chips fabricated by the advanced nanoscale CMOS processes.

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