# Improvement on ESD Robustness of Lateral DMOS in High-Voltage CMOS ICs by Body Current Injection

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***Abstract* — With the waffle layout style, body-injected technique implemented by body current injection on n-channel lateral DMOS (nLDMOS) has been successfully verified in a 0.5-μm 16-V BCD process. The TLP measured results confirmed that the secondary breakdown current ($I_{t2}$) of waffle nLDMOS can be significantly increased by the body current injection with the corresponding trigger circuit design. The latchup immunity of power-rail ESD protection circuit can be further improved by the stacked configuration with multiple nLDMOS devices in HV ICs.**

## I. Introduction

Electrostatic discharge (ESD) is an inevitable event of integrated circuits (ICs) during fabrication, packaging, conveyance, and assembly processes. ESD events can arise from the contact of a statically charged human body with an IC pin, or the contact of a statically charged machine with an IC pin. Typically, IC products were requested to have ESD robustness of at least 2kV in human-body model (HBM) [1] and 200V in machine-model (MM) [2] ESD tests.

With the thriving applications such as automotive electronics, liquid-crystal display, and light-emitting-diode driver ICs, the demands of high-voltage (HV) ICs are increasing rapidly. In high-voltage ICs, the power supply voltage ($V_{DD}$) can be over ten volts or even higher. To fabricate devices to sustain such a high operating voltage, not only the process complexity is increased but also the difficulty to guarantee the reliability of HV devices. ESD protection for HV ICs hence suffers a complex engineering issue. Due to the high trigger voltage ($V_{t1}$) and the strong snapback characteristic of HV n-channel lateral DMOS (nLDMOS), serious non-uniform turn-on issue has been found. The non-uniform turn-on behavior has constrained ESD level of nLDMOS used in the on-chip ESD protection circuits [3]. Therefore, how to effectively achieve high ESD robustness is one of the main challenges in HV CMOS ICs.

## II. Device Structure and Layout of nLDMOS

To sustain the high operating voltage, device structures of LDMOS are often more complex than those of advanced logic CMOS devices. Fig. 1 shows the device cross-sectional view of a 16-V nLDMOS. To fulfill the RESURF technique [4], the nLDMOS is surrounded by a HV N-well. As a result, the p-body is separated from the common p-type substrate (P-sub), and the channel length is decided by the overlapped distance of P-Body with the poly gate. The nLDMOS in this work is fabricated in a 0.5-μm 16-V bipolar CMOS DMOS (BCD) technology.

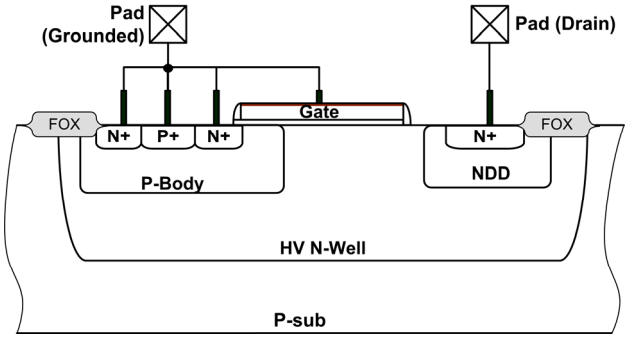


Fig. 1 Device cross-sectional view of the 16-V nLDMOS in a 0.5-μm bipolar CMOS DMOS (BCD) technology.

Because the body of the nLDMOS is separated from the p-type substrate (P-sub), additional P+ body pick up at every source region is required. Fig. 2 shows the regular layout of nLDMOS in stripe style.

In low-voltage (LV) CMOS technologies, one of the most effective methods to increase ESD robustness of ESD protection devices is the substrate-triggered technique [5]. To inject the substrate-triggered current into the base of parasitic n-p-n bipolar junction transistor (BJT) inherent in LV NMOS, a P+ trigger node was placed at drain and connected to the trigger circuit [6]. However, in HV nLDMOS, the base of its parasitic n-p-n BJT is the P-Body region. As a result, due to the reverse biased HV N-Well and P-Body, the layout method in LV technologies to inject the substrate-triggered current from the P+ trigger node at drain side cannot be implemented in such a HV BCD process.

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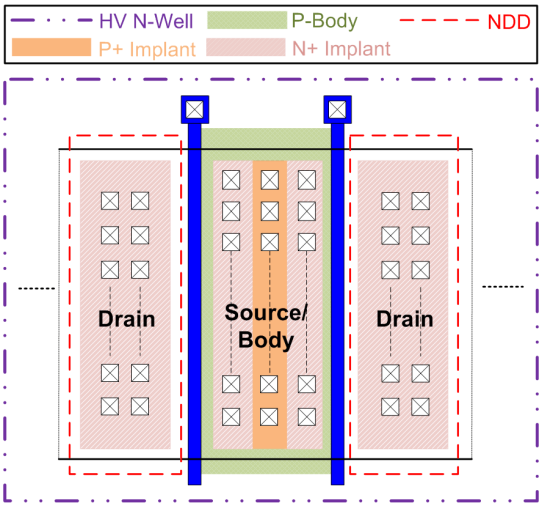


Fig. 2 Layout top view of the 16-V nLDMOS in stripe style.

## III. nLDMOS in Waffle Layout Style with Trigger Node

In order to effectively inject the trigger current into the P-Body of nLDMOS, nLDMOS realized in waffle layout style is proposed in this work. As shown in Fig. 3, the drain of nLDMOS in waffle style is drawn in a square. Source and body of the waffle nLDMOS is laid out at four sides of the drain square. Such a waffle layout style leads to four squares (Trigger Nodes) at the diagonal of drain region. In the 0.5-μm 16-V BCD process, because the P-Body in Fig. 1 is implanted before the formation of gate oxide, the four squares at the diagonal of drain are shorted to the body pick up at source/body region. The body current can therefore be injected from these trigger nodes, and be collected by the grounded P+ pick up at the source/body. The injected body current at the trigger node therefore acts as the base current, which helps turn on of the parasitic n-p-n BJT inherent in nLDMOS.

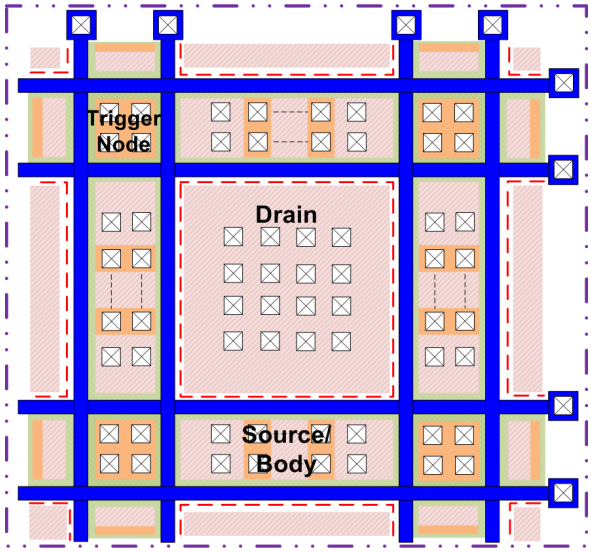


Fig. 3 Layout top view of the 16-V nLDMOS in waffle style with trigger node.

## IV. Turn-on Verification

To verify the design of body current injection in this work, a stand-alone trigger circuit and a stand-alone waffle style nLDMOS were fabricated in the same silicon chip. Corresponding measurement setup to verify the stand-alone trigger current during ESD transition is shown in the inset of Fig. 4. To effectively distinguish between ESD transition and normal power-on transition, RC distinguisher is a well-known technique in ESD protection designs, especially in the power-rail ESD clamp circuit [7]. During ESD transition, R1 and C1 result in a RC time delay, so that the trigger current (body injection current) can be provided by the HV PMOS ($M_{P1}$). During the verification measurement, an external 55-Ω discrete resistor was connected between the trigger node and the ground pad. Measured result shows that the trigger circuit can provide a peak trigger current ($I_{Trigger}$) of 30mA to the 55-Ω resistor when a 20-V voltage pulse with 10-ns rise time ($t_r$) and 1-μs pulse width ($t_{pw}$) is applied, as shown in Fig. 4. After 200ns, $I_{Trigger}$ fades to 0mA because the gate voltage of $M_{P1}$ has followed up the source voltage of $M_{P1}$ through the RC distinguisher.

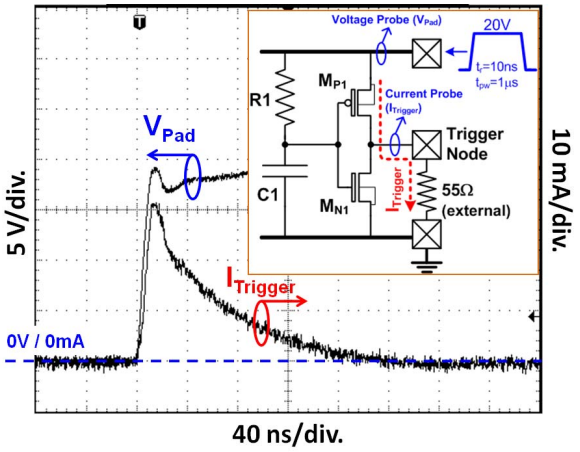


Fig. 4 Turn-on verification of the stand-alone trigger circuit. The measurement setup is shown in the inset of this figure.

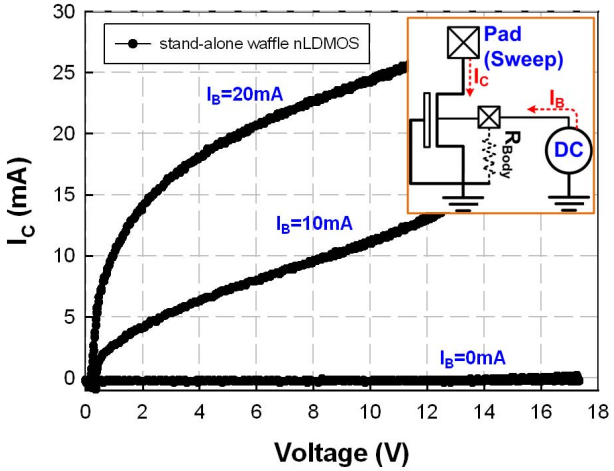


Fig. 5 Turn-on verification of the stand-alone nLDMOS drawn in waffle style with the additional body current ($I_B$) injection.

To verify the ability to trigger the parasitic n-p-n BJT of nLDMOS through the body current injection, different levels of body current ($I_B$) were injected into the stand-alone waffle nLDMOS through the trigger node. Measurement setup is shown in the inset of Fig. 5, where the $R_{Body}$ denotes the equivalent resistance of P-Body from the trigger node to the P+ body pick up. With the larger injected $I_B$ current, the nLDMOS exhibits higher collector current $I_C$. This result has verified that the parasitic n-p-n BJT inherent in waffle nLDMOS can be successfully triggered through the body current injection.

## V. Experimental Results

The 100-ns TLP measured I-V curves of three 16-V nLDMOS devices are shown in Fig. 6. The stripe nLDMOS in Fig. 6 has layout style as shown in Fig. 2. The waffle nLDMOS in Fig. 6 has layout style as shown in Fig. 3, and the trigger nodes of the waffle nLDMOS are grounded internally. The body-injected waffle nLDMOS in Fig. 6 has layout style as shown in Fig. 3, and the trigger nodes in the body-injected waffle nLDMOS are connected internally to the trigger circuit through metal directly wiring in the chip. The trigger circuit has the same design parameters as that verified in Fig. 4. These three nLDMOS have the same effective channel width and the same channel length in layout. Failure criteria (1-μA leakage current under 16-V drain bias voltage) of all devices are kept the same to judge their ESD robustness. The measured results show that the stripe nLDMOS and waffle nLDMOS have roughly the same secondary breakdown current ($I_{t2}$) of 0.39A and 0.41A, respectively, if the body current injection was not applied. By applying the body current injection, $I_{t2}$ of the waffle nLDMOS can be significantly increased from 0.41A to 0.95A. From the 100-ns TLP measurement, a more than 2X increase on $I_{t2}$ has been achieved through the waffle layout style and the technique of body current injection.

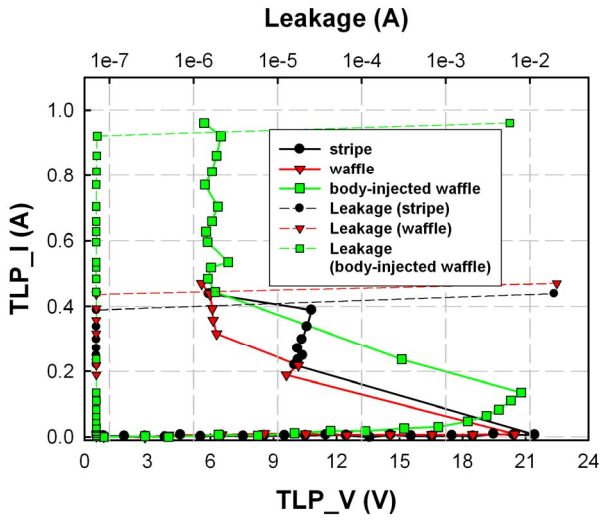


Fig. 6 The 100-ns TLP-measured I-V curves of stripe, waffle, and body-injected waffle nLDMOS.

Scanning electron microscope (SEM) image of the body-injected waffle nLDMOS after 100-ns TLP measurement is shown in Fig. 7. The failure location of the body-injected waffle nLDMOS is found on the drain of nLDMOS. This result shows that the ESD current is mainly discharged by the nLDMOS instead of the trigger circuit, which in turn confirmed the usefulness of body current injection to improve the ESD robustness of waffle nLDMOS.

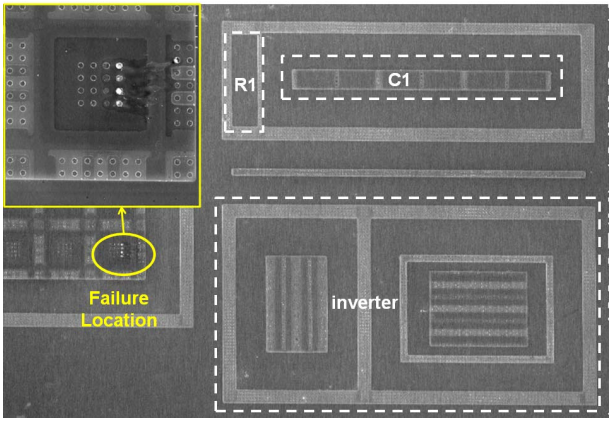


Fig. 7 Scanning electron microscope (SEM) image of the body-injected waffle nLDMOS after 100-ns TLP measurement.

## VI. Latch-Up in High-Voltage nLDMOS

In high-voltage ICs, due to the high operating voltage and the low holding voltage of ESD protection devices, latch-up has become a serious reliability concern. As the 100-ns TLP measured I-V curves in Fig. 6, the 16-V nLDMOS has a holding voltage ($V_h$) of ~6.2V only. Even if ICs have passed the quasi-static latch-up test [8], transient-induced latch-up (TLU) can still result in a devastating outcome in the field applications [9].

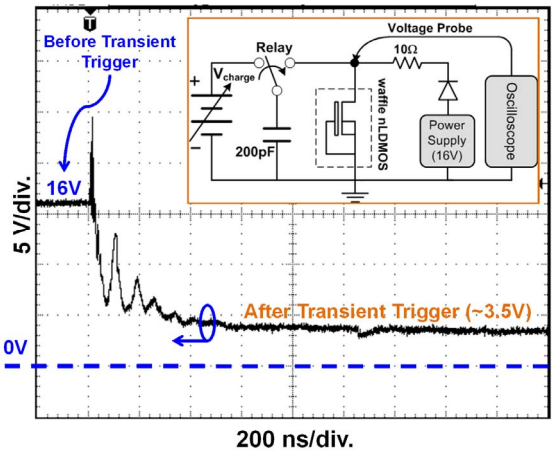


Fig. 8 Measured voltage waveform of a waffle nLDMOS under transient-induced latch-up (TLU) test.

Fig. 8 shows the TLU measured result on the 16-V waffle nLDMOS. Measurement setup is shown in the inset of Fig. 8. After the noise injection (transient trigger), the power supply voltage is pulled down from 16V to ~3.5V due to the turn-on operation of the parasitic n-p-n BJT inherent in the nLDMOS. Holding voltage difference between the TLU and 100-ns TLP measurement results can come from the device self-heating effect in the HV nLDMOS [10]. In HV ICs, if the output power of the $V_{DD}$ (power supply) is not controlled or limited,

latch-up results in huge power consumption over the latched device, which can cause huge temperature increase and eventually burn out the IC itself.

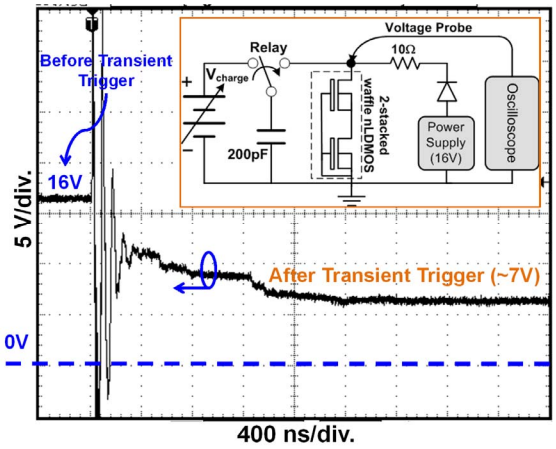


Fig. 9 Measured voltage waveform of the two-stacked waffle nLDMOS under transient-induced latch-up test.

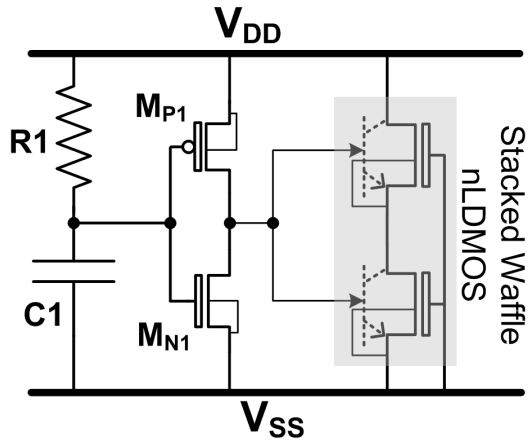


Fig. 10 Configuration of body-injected waffle nLDMOS with stacked configuration to achieve higher holding voltage and better latch-up immunity.

To increase the holding voltage of HV ESD protection devices, techniques such as the stacked configuration have been used [11]. Experimental results in [11] showed that both holding voltage and latch-up immunity can be effectively increased through the stacked configuration. Fig. 9 shows the voltage waveform of the two-stacked waffle nLDMOS under TLU measurement. By stacking two waffle nLDMOS, the holding voltage can be successfully doubled (~7V). Although the required level of holding voltage is dependent on applications, such a stacked configuration provides an effective method to increase the overall holding voltage of on-chip ESD protection circuit without additional process modifications.

However, in exchange for higher holding voltage and higher latch-up immunity, such a stacked configuration has to sacrifice large silicon area. From the 100-ns TLP measured results, the ESD robustness of nLDMOS can be increased more than 2X by the body-injected technique. As a result, under the same required ESD protection level, only half the effective channel width of the original ESD protection nLDMOS is needed by using the body-injected technique with waffle layout style. Silicon area of the stacked configuration can therefore be substantially saved without decreasing ESD robustness. Fig. 10 shows the power-rail ESD protection circuit with the body-injected waffle nLDMOS in two-stacked configuration. More number of waffle nLDMOS can be further stacked to achieve higher holding voltage and better latch-up immunity.

## VII. Conclusion

With the waffle layout style, body-injected technique implemented by body current injection on high-voltage nLDMOS has been successfully verified in a 0.5-μm 16-V BCD process. The 100-ns TLP measurement shows that with the body current injection, $I_{t2}$ of the waffle nLDMOS can be increased from 0.41A to 0.95A. With the ability to substantially increase ESD robustness of nLDMOS, effective channel width of the ESD protection nLDMOS can be reduced under the same requirement of a specified ESD level. Two or more nLDMOS devices can be stacked for higher holding voltage and latch-up immunity. In HV ICs, technique of body current injection has been shown to be an effective method for increasing the ESD robustness of high-voltage nLDMOS.

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