P-51: Design and Realization of Delta-Sigma Analog-to-Digital Converter in LTPS Technology

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Abstract

A delta-sigma analog-to-digital (A/D) converter designed and implemented with the thin-film transistors (TFTs) on glass substrate is proposed, which has been successfully verified in a 3-μm low-temperature polycrystalline silicon (LTPS) process. The experimental results have shown that the probability in the bit stream of the digital output from the delta-sigma modulator is correctly fit in the analog input voltage ratio. Such a bit stream can be converted into 8-bit digital code successfully under the operation voltage of 10V with thin-film transistors (TFTs) on the glass substrate. The proposed delta-sigma A/D converter can be further used to achieve the precise analog circuits for System-on-Panel (SOP) or System-on-Glass (SOG) applications, which enables the analog circuits to be integrated in the active matrix LCD (AMLCD) panels.

1. Introduction

Recently, the thin-film transistors (TFTs) in low-temperature polycrystalline silicon (LTPS) technology have been used to fabricate the compact and high-resolution displays [1]. The active-matrix liquid crystal displays (AMLCDs) integrated with driver and control circuits on glass substrate in LTPS technology have been used to product the portable microelectronic systems, such as mobile phone, digital camera, and notebook, etc. The CPU, memory, timing controller, digital-to-analog converter (DAC), and driving buffer had been demonstrated on glass substrate with LTPS technology [2], [3]. Moreover, integrating the driver and control circuits on glass substrate can practically made the display device thin and compact in total. Thus, the integration of more analog and digital circuits on display panel together is important for System-on-Panel (SOP) or System-on-Glass (SOG) applications.

Analog-to-digital converters (ADCs) are widely used in interface of the analog sensing circuits and digital processing circuits. For example, sensor is widely used in many applications, such as temperature sensor and image sensor [4-6]. Besides, sensing circuit can be applied to color image scanner, temperature compensation circuit, and touch panel that are indispensable in LTPS technology. Particularly, the touch panel attached on display has been widely used as an input device for mobile system such as Car Navigation System (CNS), Personal Digital Assistant (PDA), digital camera (DC), and hand-held phone.

In silicon CMOS technology, delta-sigma A/D converter has been widely used in VLSI industry. With the small amount of analog circuitry, the delta-sigma A/D converter is very economically competitive with other types of data converters, such as pipeline A/D converter or flash A/D converter, for high resolution applications in the frequency range from kilohertz scale to hundred kilohertz scale [7-9].

A delta-sigma A/D converter consists of two basic blocks, a delta-sigma modulator and a decimation filter, as shown in Fig. 1. One analog input x[n] enters the modulator, where it is sampled at a high rate. The delta-sigma modulator in the delta-sigma A/D converter is running continuously to produce a bit stream b[n]. The probability in the bit stream over a given period is approximately equal to the mean value of the analog input over the same period. The bit stream generated from the delta-sigma modulator will be filtered by the decimation filter to remove the out-of-band quantization noise which is produced from the delta-sigma modulator.

Although the delta-sigma A/D converters to convert analog input signals into digital outputs have been reported and realized in silicon CMOS technology, the delta-sigma A/D converter on glass substrate with LTPS technology was never reported in the literature.

In this work, the circuit of delta-sigma A/D converter designed and realized in a 3-μm LTPS process is proposed. The new proposed delta-sigma A/D converter has been verified on the glass substrate with the probability in the output of bit stream from the modulator fitting in the analog input voltage ratio. Furthermore, the bit stream is converted into 8-bit digital output code successfully under the power supply of 10 V.

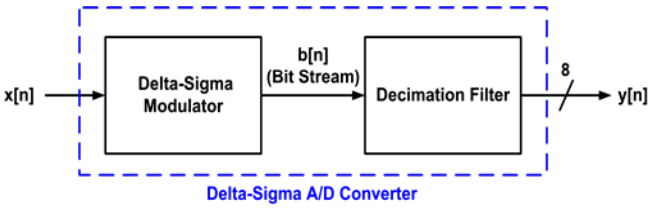

Figure 1. Basic circuit diagram of Delta-sigma A/D converter which consists of delta-sigma modulator and decimation filter.

2. Delta-Sigma Modulator

Fig. 2 shows the block diagram of delta-sigma modulator. The delta-sigma modulator consists of mainly an integrator, a comparator, and a D/A converter (DAC). The resulting single bit digital output b[n] is converted into one of two analog levels by the single-bit feedback DAC. The output of the DAC is subtracted from the analog input signal in the summing amplifier. The resultant error signal from the summing amplifier output is low-pass filtered by the integrator and the integrated error signal polarity is detected by the comparator.

With such arrangement, the transfer function of the discrete time integrator can be derived as

$$H(z)=\frac{z^{-1}}{1-z^{-1}}, \quad (1)$$

and the input-output relation of the modulator is derived and given by

$$B(z)=\frac{H(z)}{1+H(z)}X(z)+\frac{1}{1+H(z)}E(z) \quad (2)$$
$$=z^{-1}X(z)+\left(1-z^{-1}\right)E(z)$$

Thus, the input signal simply goes straight through the delta-sigma modulator with only one delay. Nevertheless, the high level quantization noise e[n] generated by the comparator, which is approximated as a white-noise source, is shaped by the high-pass function ($1-z^{-1}$), called noise transfer function (NTF). Any nonlinearity of the comparator is simply combined with the quantization error e[n], and is thus suppressed in-band along with e[n]. However, nonlinear distortion in the DAC affects the output signal without any shaping. Hence, it represents a major limitation on the attainable performance, which can be solved by using single-bit quantization. In this case, the input/output characteristic of the DAC consists of only two levels to ensure the inherent linear operation of DAC.

Moreover, the integrator design is another important part of the delta-sigma modulator. The circuit implementation of the operational amplifier is shown in Fig. 3. A folded cascode amplifier is chosen except for its high gain and its easier frequency compensation, it doesn't suffer from frequency degradation due to the power supply rejection ratio.

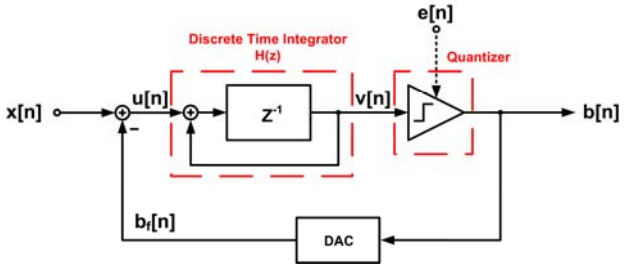

Figure 2. Block diagram of delta-sigma modulator.

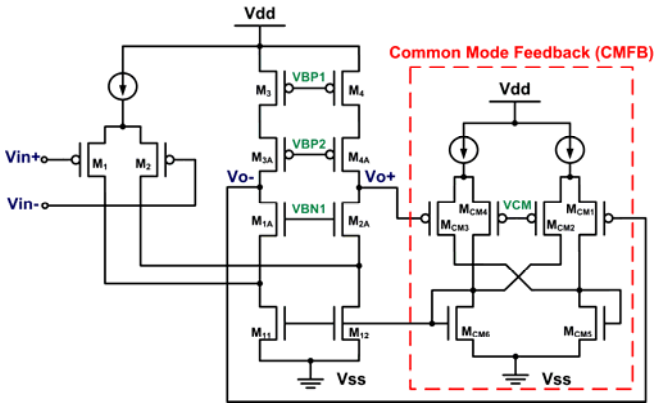

Figure 3. Circuit implementation of the fully differential operational amplifier on glass substrate in a 3-μm LTPS technology.

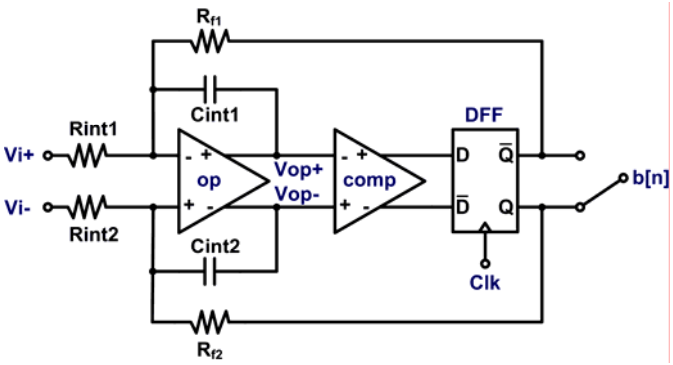

Figure 4. Circuit implementation of the delta-sigma modulator on glass substrate in a 3-μm LTPS technology.

Fig. 4 shows a continuous-time realization of delta-sigma modulator using fully-differential architecture to overcome the common-mode noise generating by process variation. In this application, there exists a comparator followed by a D flip-flop while the DAC function performed by the R_{f1} and R_{f2} resistors connected the D flip-flop outputs to the op-amp inputs. When the positive input Vi+ is equal to x[n] in Fig. 2, Vi- is equal to ten minus Vi+, under the operation voltage (Vdd) of 10 V.

As the output voltage of the D flip-flop b[n] is high ('Logic-1'), it feeds back a positive charge through R_{f2} and negative charge through R_{f1}. Then, driving the output of the integrator Vop- down and driving Vop+ up. It causes b[n] to become low ('Logic-0'), forming a negative feedback loop. Besides, when the positive input voltage Vi+ is larger than half of the supply voltage (10V), the charge increment in capacitance Cint2 during high b[n] level in one clock cycle is less than charge decrement in capacitance Cint1 during low b[n] level. Thus, the large input signal will produce high probability of 'Logic-1' in the bit steam b[n]. The typical converting example, sequential operations of delta-sigma modulator with an input signal x[n] of 6V, is listed in Table 1.

By considering the delta-sigma modulator with an input x[n], the relation between x[n], output bit stream b[n], and the output of the integrator v[n] in discrete time from the block diagram in Fig. 2 can be expressed as

$$v[n+1]=x[n]-b[n]+v[n] \quad (3)$$

Equation (3) can then be used to generate the sequences v[n] and b[n] from a given input x[n] with the initial condition of v[0]. For example, as x[n] is equal to 6V and v[0] is 1V, the probability of 'Logic-1' in the bit stream is 0.6 (6/10), which is correctly equal to the input voltage ratio (Vi+ over 10V).

n	0	1	2	3	4	5	6
x[n]	6	6	6	6	6	6	6
v[n]	1	-3	3	-1	5	1	-5
b[n]	10	0	10	0	10	10	0

Table 1. The operation of delta-sigma modulator with an input signal x[n] of 6V.

3. Decimation Filter

For a delta-sigma A/D converter, the delta-sigma modulator is operated with oversampling to produce 1-bit output stream in high data rate. However, the results can not represent the converting

results of input analog signal directly. Decimation filter acts as a low-pass function to filter the signal outer the frequency band and to decimate the output bit stream down to the Nyquist rate. This process changes the high sampling rate and low resolution digital signals into the high resolution digital signals. Then, the bit stream will be converted into 8-bit determined digital signals. In this case, a counter which is a finite-impulse-response (FIR) filter is used as a decimation filter to compute a running average of the output bit stream b[n] from the delta-sigma modulator and to produce the 8-bit digital output. By such a design, the output y[n] of the decimation filter expressed as a function of output bit stream b[n] of the delta-sigma modulator can be written as

$$y[n] = \frac{1}{N}\sum_{i=0}^{N-1} b[n-i]. \quad (4)$$

Then, equation (4) can be translated into its z-domain transfer function, which is derived as

$$H_1(z) = \frac{1}{N}\frac{1-z^{-N}}{1-z^{-1}}. \quad (5)$$

By equation (5), the amplitude of the transfer function is close to 1 near zero frequency and it decays as frequency increases. Moreover, the harmonic tones of the transfer function in equation (5) in high frequency also contribute noise to the delta-sigma A/D converter. It represents as a non-ideal low-pass filter because noise in the bit stream b[n] can be attenuated at only the certain frequency. Thus, a counter which is used as a decimation filter can be taken as a low-pass filter. However, more calculating number would lead to the error decrease gradually, even if the counter also results in some error. Moreover, an important advantage of this decimation filter is the economically realization for single-bit modulator.

Fig. 5 shows the implementation of the decimation filter and its timing chart. A counter is incremented for each 'Logic-1' of b[n] from the modulator. Once in every N clock cycle, the output of the counter is clocked into a register, then the counter is reset. Thus, the output y[n] is a down-sampled count. The counter produces k-bit output if $N=2^k$, which may be interpreted as a binary fraction between 0 and 1. In this case, N is chosen as 256 for 8-bit digital output.

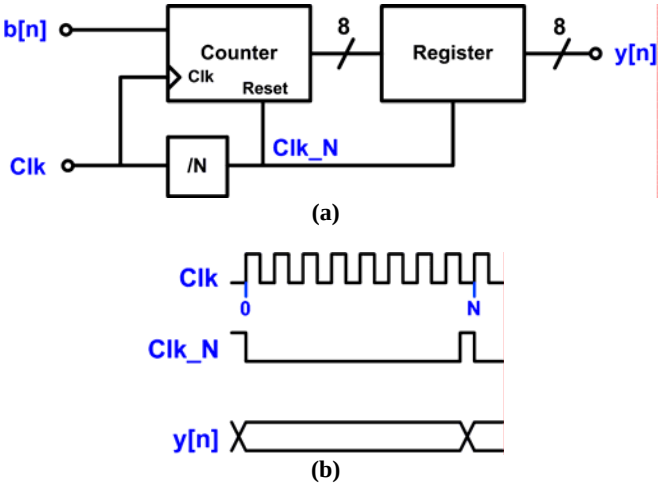

Figure 5. (a) Block diagram of decimation filter and (b) its timing chart.

4. Experimental Results

The proposed delta-sigma A/D converter on glass substrate has been fabricated in a 3-μm LTPS technology. Fig. 6 shows the die photo of fabricated delta-sigma A/D converter on glass substrate, where the test chip size is 1415μm x 1781μm. The measured results of the delta-sigma modulator, shown in Fig. 7, represent the relation between Clk and the output bit stream b[n]. As the input voltage Vi+ is equal to 1V and Vi- is equal to 9V at the clock period of 0.5 second, 16 cycles of 'Logic-0' accompany 2 cycles of 'Logic-1' can be found in the bit stream b[n]. With such an input signal, the probability of b[n] is 0.11, which is close to the input voltage ratio (1/10).

Fig. 8 shows that the input voltage Vi+ and Vi- are both changed into 5V. Then, 4 cycles of 'Logic-0' accompany 4 cycles of 'Logic-1' can be found in the bit stream b[n], which producing the probability of b[n] is 0.5 to fit in the input voltage ratio (5/10).

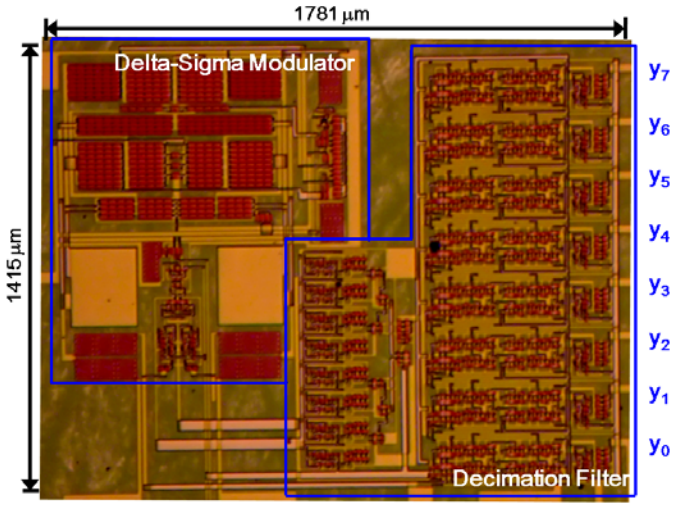

Figure 6. Die photo of the fabricated delta-sigma A/D converter in a 3-μm LTPS technology.

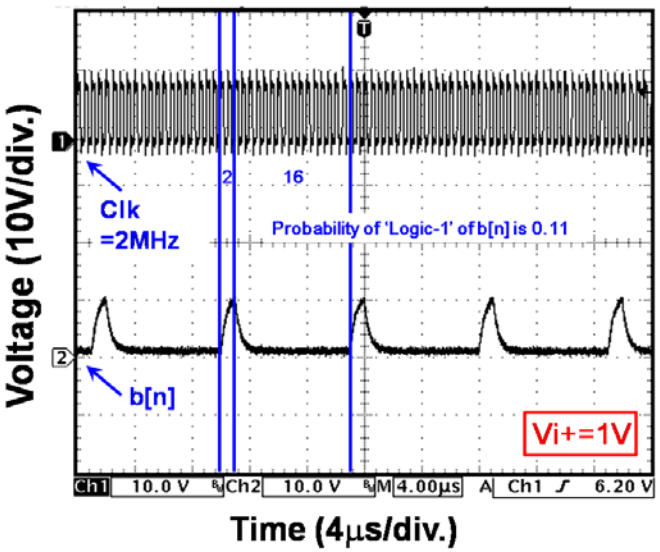

Figure 7. Measured result of b[n] when the input Vi+ is 1V and Vi- is 9V.

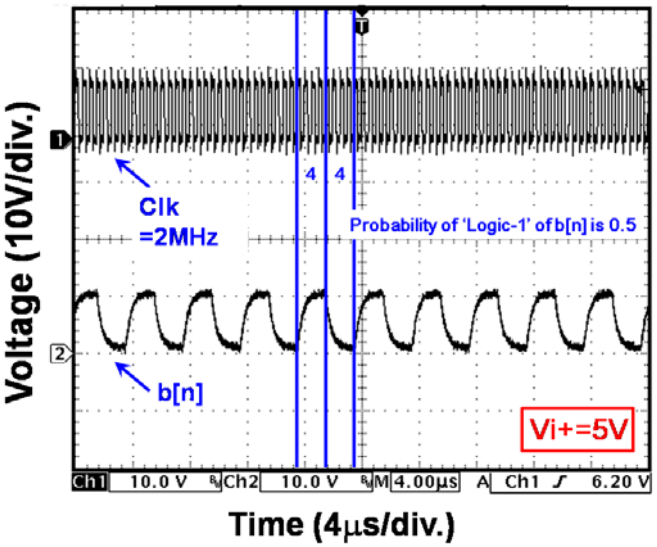

Figure 8. Measured result of b[n] when Vi+ and Vi- are both equal to 5V.

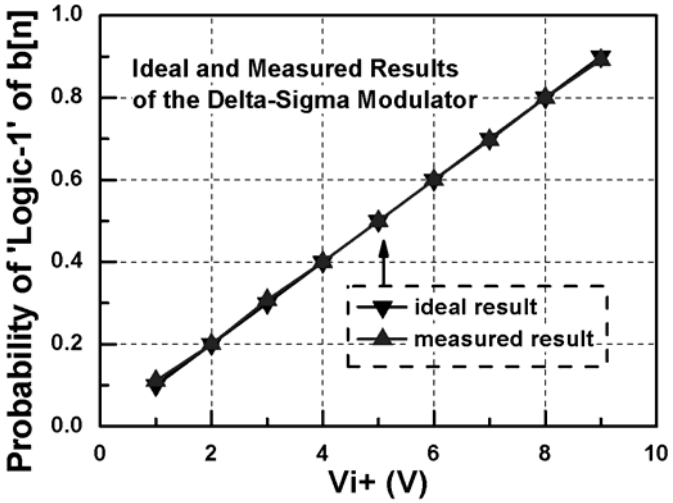

Figure 9. Measured results of the fabricated delta-sigma modulator, comparing with the ideal calculation.

Then, Vi+ is changed from 1V to 9V to observe the circuit performance of the delta-sigma modulator by such measurement procedure. To verify the proposed circuit, Fig. 9 shows the comparison between ideal and measurement results of probability of 'Logic-1' in the bit stream b[n]. Good agreement between ideal calculation and measurement results can be obtained from the fabricated delta-sigma modulator.

A counter is incremented for each 'Logic-1' of b[n] from the delta-sigma modulator. Once in every 256 clock cycles, the output of the counter is clocked into a register, then the counter is reset. The single-bit signal b[n] in bit stream form can be converted into 8-bit digital output code by the decimation filter. The proposed delta-sigma A/D converter has been successfully implemented in a 3-µm LTPS technology, which is suitable to be further integrated with display panel for system-on-panel (SOP) or system-on-glass (SOG) applications.

5. Conclusion

A delta-sigma A/D converter on glass substrate for panel integration has been successfully designed and fabricated in a 3-µm LTPS technology. A delta-sigma modulator is formed with an integrator, comparator, D flip-flop, and negative feedback loop by R_f resistors operating at frequency equal to 2MHz to produce a serial bit stream b[n] output. The input signal can be reconstructed by calculating the running probability of b[n]. The decimation filter is used to change the high sampling rate and low resolution results into the low sampling rate and high resolution results. Good agreement between ideal calculation and experimentally measured results has been obtained from the fabricated delta-sigma modulator. The delta-sigma A/D converter studied in this work, which is realized on glass substrate and successfully verified in a 3-µm LTPS technology, is firstly reported in the literature. The proposed delta-sigma A/D converter can be further used to achieve the precise analog circuits for System-on-Panel (SOP) or System-on-Glass (SOG) applications, which enables the analog circuits to be integrated in the active matrix LCD (AMLCD) panels.

6. Acknowledgment

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