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Bi-Directional SCR Device with Dual-Triggered Mechanism for ESD Protection in Extended-Voltage-Swing I/O Application

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1. Introduction

With the evolution of CMOS technology, the gate oxide thickness has been scaled down to improve circuit operating speed and performance. In order to follow the constant-field scaling requirement and reduce power consumption, the power-supply voltages in CMOS ICs have been also scaled downwards. However, some ICs still have higher voltage levels such as driver IC because of the requirement of driving capability. When a system includes different chips with different power-supply voltages, the interface I/O circuits between different chips are often subjected to undesirable leakage current problems. One of the mixed-voltage circuit applications, such as the interface in asymmetric digital subscriber line (ADSL), has input signals with voltage levels higher than VDD and lower than VSS. Under such extended-voltage-swing I/O condition, the traditional input ESD protection circuits are not suitable because the Dp (Dn) diode will be forward biased to cause leakage issue when input signals with voltage levels higher than VDD (lower than VSS) as shown in Fig. 1. Therefore, the ESD diodes or parasitic ESD diodes (Dp and Dn) in traditional input ESD protection circuits must be removed and a bi-directional ESD device could be placed between input PAD and VSS to solve leakage problems. Some previous papers were proposed to implement such bi-directional ESD devices including bi-directional SCR [1] and low-triggering bi-directional SCR with p+ diffusion [2].

The substrate-triggered technique has obvious improvement on reducing trigger voltage of general SCR device [3]. In this paper, a bi-directional SCR (BISCR) with substrate-triggered technique (called as ST-BISCR) is implemented and has lower trigger voltage (Vt1) and higher secondary breakdown current (It2) to protect thin internal gate oxide in extended-voltage-swing I/O application.

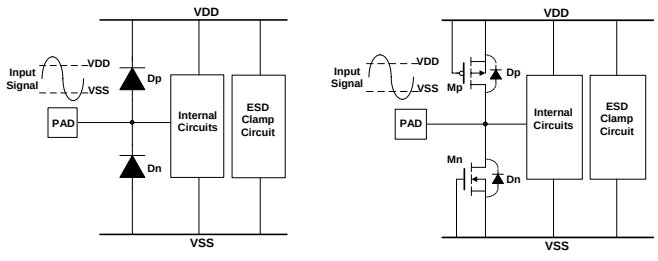

Fig. 1 Leakage problems will be induced in traditional input ESD protection circuits under extended-voltage-swing I/O condition.

2. Device Structure of ST-BISCR

The cross-sectional view of ST-BISCR is shown in Fig. 2 and the gray dash lines indicate ESD current directions under positive and negative ESD stresses applied on I/O pad with grounded VSS. In addition, in order to decrease the Vt1 of the bi-directional SCR, two p-trigger nodes (P-trig 1 and P-trig 2) were inserted into the bi-directional SCR as shown in Fig. 2. The trigger current would respectively inject into P-trig 1 and P-trig 2 nodes under positive and negative ESD stresses by adding suitable ESD detection circuit described in next paragraph.

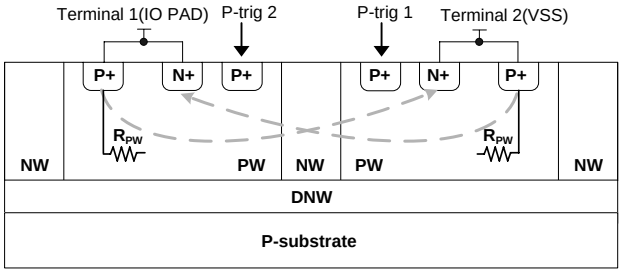

Fig. 2 The cross-sectional view of ST-BISCR device structure.

3. Experimental Results and ESD Protection Circuit

DC I-V Characteristics

The ST-BISCR has been fabricated in 0.18-μm mixed-signal CMOS technology without any specific process modification. The dependence of Vt1 of ST-BISCR on the substrate-triggered current are compared in Fig. 3 and the inset of Fig. 3 is the measured DC I-V curves of ST-BISCR under different substrate-triggered currents. When the substrate-triggered currents at two p-trigger nodes are increased from 0mA to 7mA, the Vt1 of ST-BISCR is reduced from 16.5V/-16.5V to 1.36V/-1.36V. The DC I-V results have proven that increasing the substrate-triggered current can significantly reduce the Vt1 of ST-BISCR.

TLP I-V Characteristics

Fig. 4 is the measured TLP I-V curves of BISCR in ref. [1], low-triggering BISCR in ref. [2], and ST-BISCR. The device width is 50μm and the spacing from anode to cathode of these three structures is identical in the layout. The Vt1 of ST-BISCR is only 4.31V/-4.30V and is the lowest value among three structures as seen in Fig. 4. Because the gate oxide breakdown voltage in 0.18-μm CMOS process is about 9.7V, the Vt1 of ST-BISCR (4.31V/-4.30V) is applicable in 0.18-μm mixed-signal

CMOS process. On the other hand, the It2 of ST-BISCR slightly increases to 3.83A/-3.82A and is the highest value compared with other two structures. In general, the HBM ESD level increases as It2 increases. The TLP results of Vt1 and It2 can prove that ST-BISCR has lower Vt1 and higher ESD level for the extended-voltage-swing I/O application in 0.18-μm mixed-signal CMOS process.

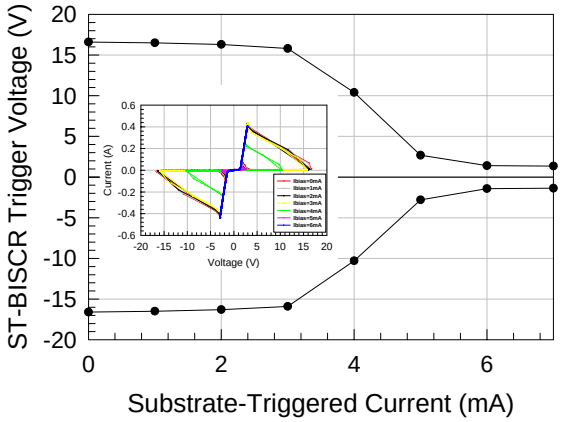

Fig. 3 The dependence of Vt1 of ST-BISCR on the substrate-triggered current and the inset is the measured DC I-V curves of ST-BISCR under different substrate-triggered currents.

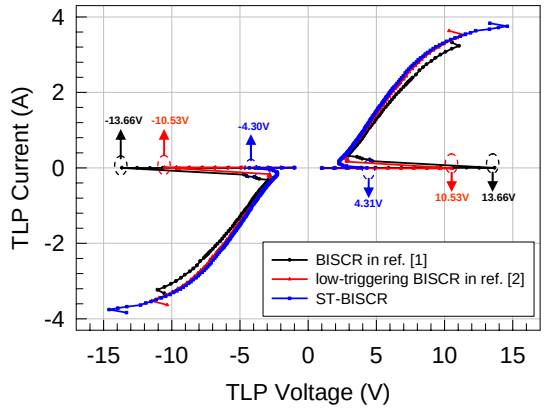

Fig. 4 The measured TLP I-V curves of BISCR in ref. [1], low-triggering BISCR in ref. [2], and ST-BISCR.

Discussion on ESD-Transient Detection Circuit

To generate trigger current under ESD condition, suitable ESD detection circuit must be added in ESD protection circuit. Fig. 5 is the ESD protection design including positive-ESD detection circuit, negative-ESD detection circuit and ST-BISCR. The resistor R1 is applied to avoid sudden damage occurred at the gate of Mp1 under ESD condition. The PMOS (Mp1) is turned on to conduct positive trigger current into P-trig 1 node through n-diode-string to trigger ST-BISCR on under positive ESD stress, while negative trigger current is also generated and conducted into P-trig 2 node through m-diode-string to trigger ST-BISCR on under negative ESD stress. In the normal circuit operating condition, the ESD protection circuit must remain in a non-conductive state in order that it does not interfere with the voltage levels on the I/O pad. Therefore, the equation to avoid positive-ESD detection circuit being turned on can be expressed as

$$V_{PAD} < (n \times V_{diode}) + |Vtp|_{Mp1} + VDD$$

Moreover, the equation to avoid negative-ESD detection circuit being turned on can be also expressed as

$$V_{PAD} > VSS - (m \times V_{diode})$$

where V_{PAD} is the voltage level on the I/O pad, V_{diode} is the cut-in voltage of diode, and $|Vtp|_{Mp1}$ is the threshold voltage of the PMOS (Mp1). For example, in order to satisfy the requirements of extended voltage swing (V_{PAD} is -2V~3.8V) and VDD/VSS (1.8V/0V), the number of the diodes in the n-diode-string and m-diode-string should be adjusted to be 3 and 4 respectively to avoid positive-ESD detection circuit and negative-ESD detection circuit being turned on under normal operation condition as V_{diode} and $|Vtp|_{Mp1}$ are 0.57V and 0.45V respectively in 0.18-μm mixed-signal CMOS process. The n-diode-string and m-diode-string are composed of individual diodes formed by using p+ diffusion in the separated n-well structure. Since n-diode-string and m-diode-string are not in the main ESD current discharging path, their perimeters can be adjusted to be smaller than those of ESD diodes.

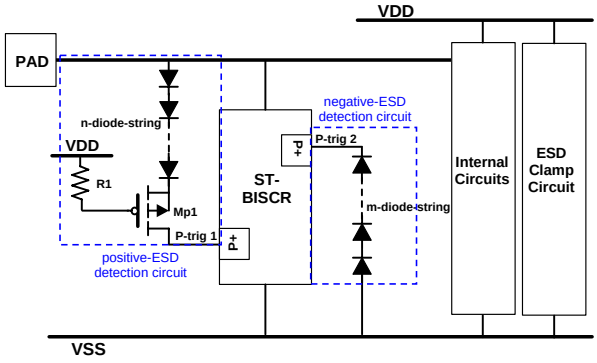

Fig. 5 ESD protection design including ESD detection circuit and ST-BISCR.

4. Conclusions

The ST-BISCR device has been implemented successfully in 0.18-μm mixed-signal CMOS process. It has lower Vt1 and higher It2 for input signals with voltage levels higher than VDD and lower than VSS. Such ESD protection circuit can effectively protect the thin gate oxide against ESD damage in deep submicron CMOS integrated circuits and extended-voltage-swing I/O application.

References

[1] Z.-H. Wang and C.-H. Tsay, "On a dual-polarity on-chip electrostatic discharge protection structure," *IEEE T-ED*, vol. 48, pp. 978-984, 2001.

[2] Z.-W. Liu, J. Vinson, L.-F. Lou, and J.-J. Liou, "An improved bidirectional SCR structure for low-triggering ESD protection ," *IEEE EDL*, vol. 29, pp. 360-362, 2008.

[3] M.-D. Ker and K.-C. Hsu, "Substrate-triggered SCR device for on-chip ESD protection in fully silicided subquarter-micrometer CMOS process," *IEEE T-ED*, vol. 50, pp. 397-405, 2003.