Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials, Sendai, 2009, pp372-373

P-2-13

Low-Capacitance and Low-Loss Bond Pad Design Using LC-Resonator Structure in CMOS Technology for RF and High-Speed Applications

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1. Introduction

As nanoscale CMOS technology wildly be used to implement RF and high-speed integrated circuits (ICs) [1], the semiconductor nature of silicon substrate introduces the undesired parasitic capacitance between the substrate and input pad, which will disturb the high frequency signals, induce RC delay in the signal path, and cause other degradation on the circuit performances [2]. The parasitic capacitance at the input pad must be minimized. For a 5-GHz low-noise amplifier in an RF receiver, the typical specification on the total input loading capacitance is in the order of 100 fF, including the bond pad and input electrostatic discharge (ESD) protection devices [3]. The specification is even stricter for the circuits applied to higher frequency band. However, the dimensions of ESD protection devices and bond pad can not be shrunk in advanced CMOS process due to the considerations of reliability and bondability; namely, the parasitic effects of ESD protection devices and bond pad can not be reduced with the shrinking process. Therefore, the implementations of low-capacitance bond pad and ESD protection device are strongly requested by RF and high-speed ICs.

2. Low-Capacitance and Low-Loss Bond Pad Design

The low-capacitance bond pad with embedded inductor has been presented [4]. In some bond-pad patterns with embedded inductors, the insertion loss may increase significantly. Therefore, the low-capacitance bond pad with embedded inductor must be optimized to lower the insertion loss.

The device structure and circuit model of the low-capacitance bond pad with embedded inductor are shown in Figs. 1 and 2, respectively. The circuit model for the bond pad consists of three parts, which are the parasitic capacitance between the support metal and the overlapped substrate, the coupling effect between the support metal and stacked inductor, and the stacked inductor model. In order to lower the insertion loss of the low-capacitance bond pad, a simple approach is to shift the embedded inductor in the bond pad to the lower metal layers, which can reduce the loss through the parasitics between the support metal and stacked inductor. The bond pad with the lower-metal-layer inductor is implemented to improve the insertion loss from that with the higher-metal-layer inductor.

In this work, a 65-nm one-poly ten-metal (1P10M) CMOS process is used. The reference pad 1 without embedded inductor is implemented with the top three metal layers (metal 8~10) and the lower metal layers (metal 1~7) are removed to reduce the bond-pad capacitance. Other bond pads with two kinds of inductors, which are the reference pad 2 with embedded inductor using metal 5~7, and the optimized pad with embedded inductor using metal 1~5, have also been implemented in the same test chip for comparison. The effective thickness of the inductors in these bond pads are about 0.7 μm and 0.9 μm, respectively. Both inductors are drawn with 4-μm track width, 2-μm track spacing, and three turns. The polysilicon layer as the patterned ground shield is used to reduce the energy dissipation in substrate and increase quality factor of the inductor [5]. All the inductors are implemented within the region of bond pad, and each bond pad occupies silicon area of 52 μm × 64 μm. One-port ground-signal-ground (G-S-G) pads are adopted to facilitate on-wafer RF measurement. The layout top view of one test pattern used to measure the s-parameter is shown in Fig. 3.

3. Experimental Results

Figs. 4 and 5 show the extracted capacitance and insertion loss of the fabricated bond pads under different frequencies. The bond pads with embedded inductors have very small capacitance around the specific frequency band. The optimized pad with lower-metal-layer inductor has the lower loss, and the lower loss is more tolerable for RF and high-speed ICs. Therefore, the optimized low-capacitance bond pad is much suitable for RF and high-speed applications. The frequency at which the capacitance of the bond pad is minimum can be shifted by adjusting the resonant frequency of inductance and capacitance, which can be achieved by changing the track width, spacing, turn numbers, or other dimensions of the embedded inductor.

4. Conclusions

With carefully design on the embedded inductor under the bond pad, the optimized bond pad can perform both low parasitic capacitance and insertion loss. The optimized bond pad can be realized in any bulk CMOS technology, and widely used for RF and high-speed ICs.

Acknowledgements

This work was supported by Faraday Technology Corporation, Taiwan, and National Science Council, Taiwan, under Contract of NSC 97-2221-E-009-170.

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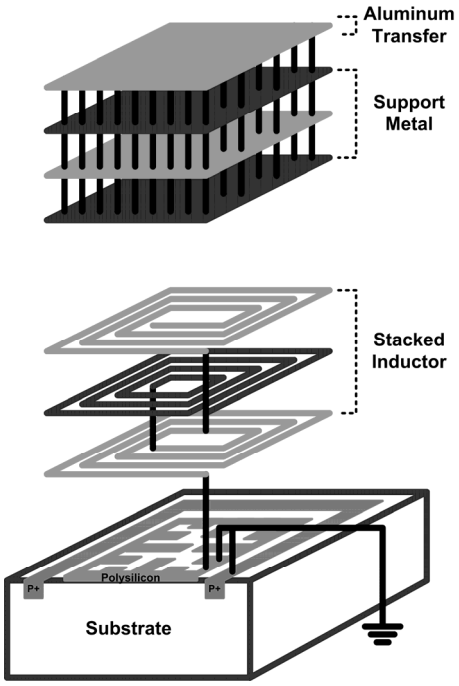

Fig. 1 Low-capacitance bond pad with stacked inductor.

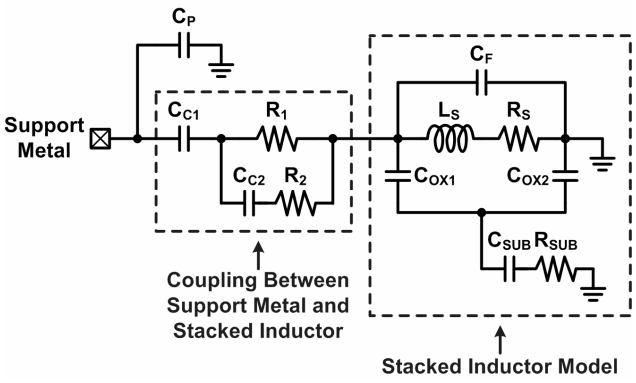

Fig. 2 Circuit model of bond pad with embedded inductor.

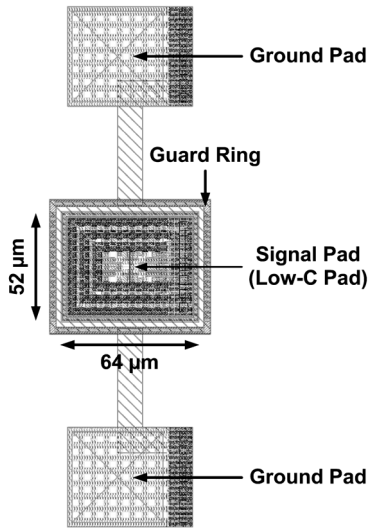

Fig. 3 Layout top view of one test pattern with one-port G-S-G pads.

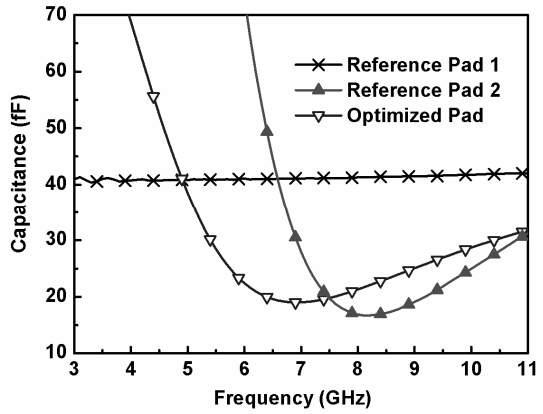

Fig. 4 Extracted bond pad capacitance of each fabricated bond pad under different frequencies.

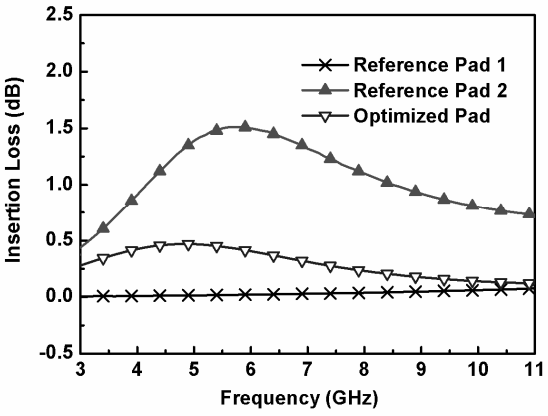

Fig. 5 Extracted insertion loss of each fabricated bond pad under different frequencies.