DESIGN OF ON-CHIP POWER-RAIL ESD CLAMP CIRCUIT WITH ULTRA-SMALL CAPACITANCE TO DETECT ESD TRANSITION

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***Abstract*—A power-rail ESD clamp circuit with a new proposed ESD-transient detection circuit which adopts a ultra small capacitor to achieve the required functions has been presented and substantiated to own a long turn-on duration and high turn-on efficiency. In addition, the power-rail ESD clamp circuits with the new proposed ESD-transient detection circuit also presented an excellent immunity against the mis-trigger and the latch-on event under the fast power-on condition.**

INTRODUCTION

ElectroStatic Discharge (ESD) protection has become a tough task on the product reliability of CMOS integrated circuits fabricated in the advanced nanoscale technology. The scaled down device dimension with thinner gate oxide and shallower junction depth in nanoscale CMOS technology is easily damaged by ESD stress. The power-rail ESD clamp circuit is an efficient design to achieve whole-chip ESD protection in IC products [1], [2]. It not only can enhance ESD robustness of VDD-to-VSS ESD stress, but also can significantly improve ESD robustness of the ESD stresses between input/output and VDD/VSS [2]. To efficiently protect the core circuits realized with much thinner gate oxide in nanoscale CMOS technology, some studies had reported the efficient NMOS-based power-rail ESD clamp circuits without snapback operation [3]-[9]. All of them adopted the gate-driven mechanism [1]-[9], which was basically implemented by an ESD-transient detection circuit and a controlling circuit, to respectively command the main ESD clamp NMOS transistor into the on state or the off state under the ESD-stress conditions and normal circuit operation conditions, as illustrated in Fig. 1.

Two major different circuit schemes, which are RC-time delay technique [1]-[7] and capacitance coupling mechanism [8], [9], were usually used as the ESD-transient detection circuit in the power-rail ESD clamp circuit. Then, the controlling circuit was always implemented by single- or multi-stage inverters. In such power-rail ESD clamp circuit, main ESD clamp NMOS transistor can thoroughly discharge huge ESD current by its channel current to exhibit excellent turn-on efficiency, such as lower trigger voltage (Vt1) and lower clamped voltage (Vclamp). The main ESD clamp NMOS transistor without snapback operation has to be kept at the on state under the whole duration of ESD events in order to ensure that the ESD current can be discharged by its channel current. Based on the traditional RC-based ESD-transient detection circuit [1], [2], the RC-time constant which is the product of the resistance (R) and capacitance (C) essentially dominated the turn-on duration of the main ESD clamp NMOS transistor. Therefore, the RC-time constant of the RC-based ESD-transient detection circuit should be designed to sufficiently achieve a desirable turned-on duration of the main ESD clamp NMOS transistor. In general, the turn-on duration was adjusted to meet the period of human-body-model (HBM) ESD event, which is about several hundred nano-seconds (ns) [10]. The extended RC-time constant not only accompanies with the larger layout sizes of the resistance and capacitance, but also is subject to mis-trigger the main ESD clamp NMOS transistor under fast power-on applications [5]. Several previous works proposed special circuit schemes with feedback circuit techniques to extend the turn-on duration under a small RC-time constant [3]-[5], [8]-[9]. However, those feedback circuit designs always suffered from the latch-on threats under the fast power-on events or the electrical fast transient noise [11]. Besides, other circuit schemes without feedback circuit techniques, such as on-time control circuit [4] and multi-RC-triggered [6], also had been presented to achieve the desirable turn-on duration and to avoid the latch-on threat. However, extra resistances and capacitances have to be implanted into these designs, which occupying a quite silicon area.

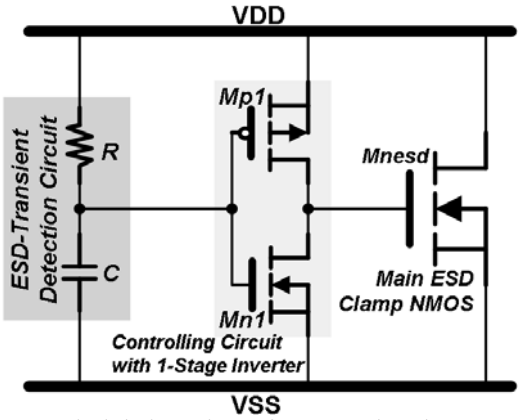


FIGURE 1. Typical design scheme for NMOS-based power-rail ESD clamp circuit with an ESD-transient detection stage and controlling stage.

In this work, an efficient ESD-transient detection circuit has been proposed and verified in 130-nm 1.2-V CMOS technology. This design abandons the feedback circuit techniques and adopts capacitance coupling mechanism to accomplish the desirable function on commanding the main ESD clamp NMOS transistor. Through experimental measurements, such as turn-on verification, ESD stress, and fast power-on test, this power-rail ESD clamp circuit with the new proposed ESD-transient detection circuit presents an excellent performance to meet the specific requirements. According to the measured results, the new proposed ESD-transient detection circuit possesses the sufficient turn-on duration under the ESD-stress conditions and high mis-trigger and latch-on immunities under the fast power-on conditions.

REALIZATION OF POWER-RAIL ESD CLAMP CIRCUIT

Area-efficient ESD-transient detection circuit with ultra small capacitor has been presented in Fig. 2, which adopts capacitance coupling mechanism to achieve the required functions on the power-

rail ESD clamp circuit. This area-efficient ESD-transient detection circuit consists of an ultra small capacitor (C1), cascode NMOS transistors (Mnc1 and Mnc2), a resistor (R1), and a switch NMOS transistor (Mns), commanding the main ESD clamp NMOS transistor through a controlling circuit with single-stage inverter. The ultra small capacitor is implemented by metal-oxide-metal (MOM) parasitic capacitance. The cascode NMOS transistors are used as a large resistor and cooperated with the ultra small capacitor to construct a capacitance coupling network [12]. The node A between the ultra small capacitor and the cascode NMOS transistors is connected to gate terminal of the switch NMOS transistor. Then, its drain terminal is tied to the VDD through the resistor and also connected to the input of the controlling circuit. Through the controlling circuit, the switch NMOS transistor can rule the main ESD clamp NMOS transistor to keep at "on" or "off" state. Finally, the main ESD clamp NMOS transistor has been drawn with the BigFET layout style, which has the minimum drain-contact-to-poly - gate spacing of 0.25 µm and without silicide blocking on its diffusion. This testchip is fabricated in a 130-nm 1.2-V CMOS process. Compared with the layout area of the power-rail ESD clamp circuit with traditional RC-based ESD-transient detection circuit, this work with the new proposed ESD-transient detection circuit is far smaller in the power-rail ESD clamp circuit, as shown in Figs. 3(a) and 3(b). The cell height of the novel power-rail ESD clamp circuit is reduced about 15 % and the layout area of the ESD-transient detection circuit is more reduced about 50 %.

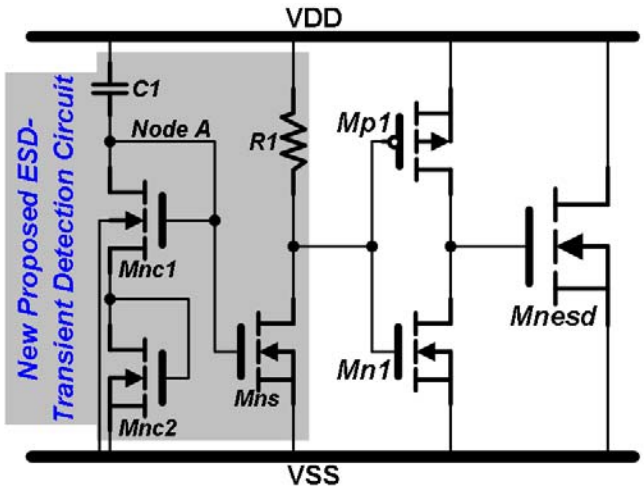


FIGURE 2. Novel power-rail ESD clamp circuit with a new proposed ESD-transient detection circuit.

During the positive VDD-to-VSS ESD stress condition, the potential of the node A will be synchronously evaluated toward a positive voltage potential by the capacitance coupling of the ultra small capacitor to trigger on the switch NMOS transistor. Then, through the switch NMOS transistor and the controlling circuit, the gate terminal of the main ESD clamp NMOS transistor will be promptly charged toward the positive voltage potential. The main ESD clamp NMOS transistor is turned on to clamp and discharge the huge ESD voltage and ESD current. The turn-on duration of the main ESD clamp NMOS transistor is dominated by the potential of node A. This potential is synchronously kept at the positive voltage potential by the capacitance coupling; however, it will be slowly pulled down due to the turned-on cascode NMOS transistors. Because the gate terminals of these two cascode NMOS transistors with small device dimensions have been connected to their drain terminals, they are operated at saturation region to provide a huge resistance under the positive VDD-to-VSS ESD event. Finally, when the potential of node A is lower than the threshold voltage of NMOS transistor, the switch NMOS transistor will be turned off to force the main ESD clamp NMOS transistor off. Based on the simulation result, the turn-on duration of the main ESD clamp NMOS transistor can achieve over 600 ns in the power-rail ESD clamp circuit with the ultra small capacitor of only ~10 femto-Farad (fF), as presented in Fig. 4.

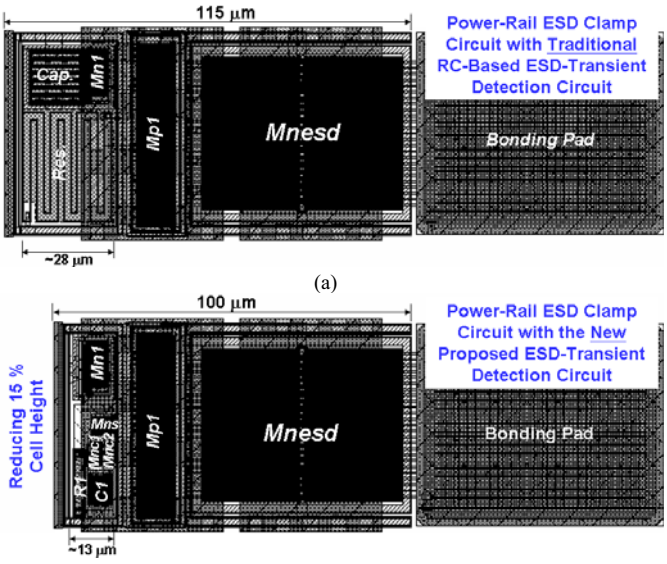


FIGURE 3. The comparison of the layout areas between the power-rail ESD clamp circuits with (a) the traditional, and (b) the new proposed, ESD-transient detection circuits.

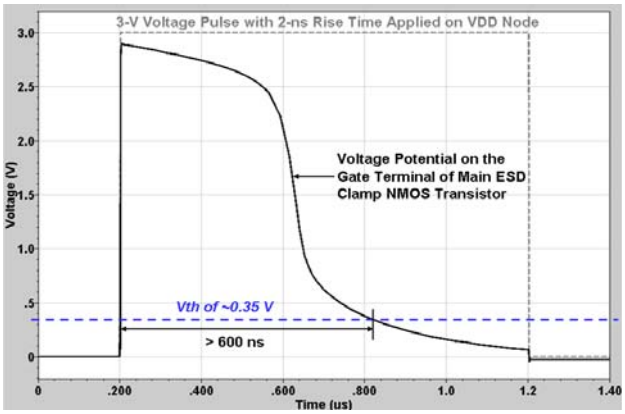


Figure 4. The simulation result of the voltage potential on the gate terminal of main ESD clamp NMOS transistor in power-rail ESD clamp circuit.

The 3-V voltage pulse with rise time of 2 ns was applied on VDD node with VSS node grounded. The voltage potential on the gate terminal of main ESD clamp NMOS transistor is higher than the threshold voltage of ~0.35 V during the period of ~620 ns. The detailed design parameters, such as device sizes of cascode NMOS transistors and switch NMOS transistor, have been listed in Table I. On the other hand, the parasitic drain-bulk diode of the main ESD clamp NMOS transistor can provide low impedance path under negative VDD-to-VSS ESD stress. Under the normal power-on condition, the normal VDD power-on voltage waveform has a rise time in the order of milli-second (ms). Such power-on voltage waveform will not produce enough coupling potential on the node A to trigger on the switch NMOS transistor. The potential of node A

will be actually kept at ground through the high resistance path of the cascode NMOS transistors. Therefore, the main ESD clamp NMOS transistor will be kept at "off" state under the normal circuit operation condition. Besides, the power-rail ESD clamp circuit with the new proposed ESD-transient detection circuit also presents a high immunity against mis-trigger and latch-on event.

TABLE I. Design parameters in the power-rail ESD clamp circuit with the new proposed ESD-transient detection circuit

Design Parameters	
Ultra Small Capacitor	10 fF
Device Size of Cascode NMOS	4 μm/2 μm (W/L)
Resistor	1.5 kΩ
Device Size of Switch NMOS	60 μm
Device Size of Main ESD Clamp NMOS	2600 μm

EXPERIMENTAL RESULTS

A. Turn-On Verification under ESD-Like Stress Condition

In order to observe the turn-on efficiency of the power-rail ESD clamp circuit with the new proposed ESD-transient detection circuit, 2.4-V and 5-V ESD-like voltage pulses with 2-nano-seconds (ns) rise time are applied on the VDD terminal with VSS terminal grounded. The voltage pulses with a rise time of 2 ns and duration of 1 μs generated from a pulse generator are used to simulate the fast rising edge of HBM ESD event [10]. The sharp-rising edge of the ESD-like voltage pulse will be detected by the ESD-transient detection circuit and then to turn on the switch NMOS transistor. The main ESD clamp NMOS transistor is therefore triggered on by the controlling circuit. When the main ESD clamp NMOS transistor is turned on, the voltage waveform on VDD terminal will be clamped as the measured results shown in Fig. 5.

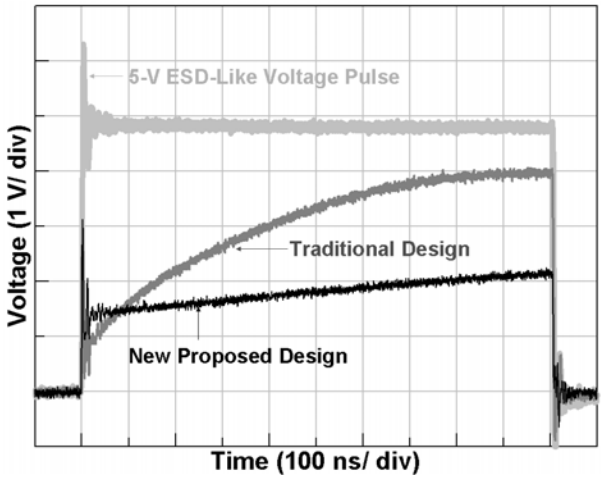


FIGURE 5. The measured voltage waveforms of the power-rail ESD clamp circuits with the traditional and the new proposed ESD-transient detection circuits under 5-V ESD-like voltage pulses with 2-ns rise time.

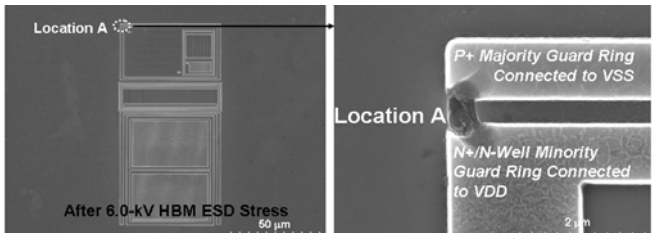
According to the measured results in Fig. 5, the new proposed design exhibits an excellent turn-on efficiency to clamp the overshooting voltage to a much lower voltage level. The voltage waveform of the new proposed design can be constantly clamped by the turned-on main ESD clamp NMOS transistor during the whole 1-μs pulse width. On the contrary, the voltage waveform of the traditional design will quickly raise and its clamped voltage is much higher than that of the new proposed design after the duration of 200 ns. The new proposed ESD-transient detection circuit can efficiently extend the turn-on duration of the main ESD clamp NMOS transistor in the power-rail ESD clamp circuit. The longer turn-on duration of the main ESD clamp NMOS transistor would assure that the low impedance path was entirely provided from VDD to VSS under the whole HBM ESD event, and would also enhance the ESD robustness of the power-rail ESD clamp circuit.

B. ESD Robustness and Failure Analysis

Table II shows the HBM and machine model (MM) [13] ESD robustness of these two power-rail ESD clamp circuits. The HBM and MM ESD robustness of the power-rail ESD clamp circuit with the new proposed ESD-transient detection circuit are 8.0 kV and 400 V, respectively, which are obviously higher than those of the power-rail ESD clamp circuit with the traditional ESD-transient detection circuit. According to the failure analysis by SEM observation, the failure spot of the traditional design is located on the unexpected junction melting damages between the n+/n-well minority guard ring and the p+ majority guard ring after 6.0-kV HBM ESD stress, as shown in Figs. 6(a) and 6(b). Because the power-rail ESD clamp circuit with traditional ESD-transient detection circuit has insufficient turn-on duration, the huge ESD current could not efficiently discharge during the whole HBM ESD event to induce the unexpected failure spot after 6.0-kV HBM ESD stress.

TABLE II. HBM and MM ESD robustness of the power-rail ESD clamp circuits with the traditional and the new proposed ESD-transient detection circuits.

Design	HBM	MM
Traditional	5.5 kV	200 V
New Proposed	8.0 kV	400 V



(a) (b)

FIGURE 6. The failure spot of the power-rail ESD clamp circuit with traditional ESD-transient detection circuit after 6.0-kV HBM ESD stresses.

C. Fast Power-On Condition and Discussion

In general, the normal VDD power-on voltage waveform has a rise time in the order of milli-second (ms) and amplitude of VDD operation voltage. Due to such a slow rise time and small amplitude in normal power-on conditions, the coupling potential on the node A is too weak to turn on the switch NMOS transistor. Therefore, the main ESD clamp NMOS transistor will be well kept at off state. In this work, both power-rail ESD clamp circuits with the traditional and the new proposed ESD-transient detection circuits can successfully achieve this desirable task under normal power-on conditions. However, some previous studies [5], [11] have illustrated that several power-rail ESD clamp circuits with RC-based ESD-transient detection circuits and feedback circuit schemes were easily mis-triggered and into the latch-on state under the fast power-on

conditions with the rise time in the order of nano-second (ns). The design with the new proposed ESD-transient detection circuit has been applied with 1.2-V voltage pulses with 100-ns or 2-ns rise time, both of which are used to simulate the fast power-on condition, to investigate its immunities against the mis-trigger and latch-on event. The measured results are respectively shown in Figs. 7(a) and 7(b). Its measured voltage waveforms do not show any obvious degradation under the fast power-on condition with voltage pulse of 1.2 V and rise time of 100 ns or 2 ns. On the contrary, the power-rail ESD clamp circuit with the traditional ESD-transient detection circuit suffered from the mis-trigger under the fast power-on conditions. Its voltage waveforms will be slightly degraded under the 1.2-V fast power-on pulse with 100-ns rise time, and dramatically degraded under that with 2-ns rise time. Compared with the results in the previous studies [4]-[6], [8], [9], the power-rail ESD clamp circuit with new proposed ESD-transient detection circuit possesses an excellent immunity against mis-trigger and latch-on event. Because the new proposed ESD-transient detection circuit adopts the capacitance coupling mechanism, this new proposed design not only distinguishes the abnormal overshooting voltage pulse by its rise time, but also discriminates this voltage pulse by its voltage amplitude. The new proposed ESD-transient detection circuit can easily distinguish the ESD event from the fast power-on condition with the voltage amplitude of 1.2 V and the rise time of 2 ns.

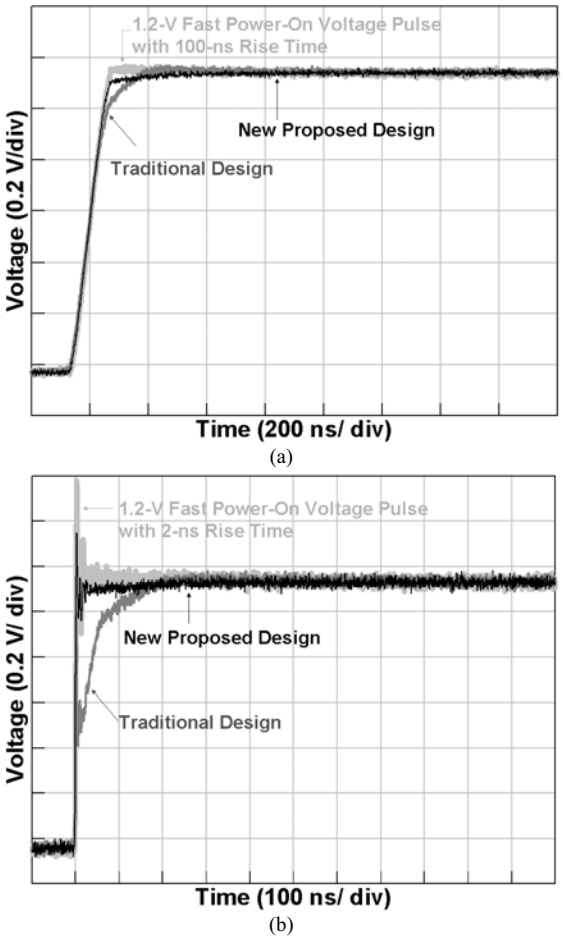


FIGURE 7. The measured voltage waveforms of the power-rail ESD clamp circuits with the traditional and the new proposed ESD-transient detection circuits under the 1.2-V fast power-on conditions with (a) 100-ns rise time and (b) 2-ns rise time.

CONCLUSION

A new proposed ESD-transient detection circuit cooperated with NMOS-based power-rail ESD clamp circuit has been presented and successfully verified in a 130-nm CMOS technology. The new proposed ESD-transient detection circuit adopts the capacitance coupling mechanism and a switch NMOS transistor to command the main ESD clamp NMOS transistor by the general controlling circuit with single-stage inverter. According to the measured results, the power-rail ESD clamp circuit with the new proposed ESD-transient detection circuit exhibits the superior ESD robustness of 8.0 kV and 400 V in HBM and MM ESD stresses, respectively. Moreover, it also possesses an excellent immunity against the mis-trigger and latch-on event under the 1.2-V fast power-on condition with the rise time of 2 ns.

REFERENCES

[1] R. Merrill and E. Issaq, "ESD design methodology," in *Proc. EOS/ESD Symp*., 1993, pp. 233-237.

[2] M.-D. Ker, "Whole-chip ESD protection design with efficient VDD-to-VSS ESD clamp circuits for submicron CMOS VLSI," *IEEE Trans. Electron Devices*, vol. 46, pp. 173-183, 1999.

[3] S. Poon and T. Maloney, "New considerations for MOSFET power clamps," in *Proc. EOS/ESD Symp*., 2002, pp. 1-5.

[4] M. Stockinger, J. Miller, M. Khazhinsky, C. Torres, J. Weldon, B. Preble, M. Bayer, M. Akers, and V. Kamat, "Boosted and distributed rail clamp networks for ESD protection in advanced CMOS technologies," in *Proc. EOS/ESD Symp*., 2003, pp. 17-26.

[5] J.-J. Li, R. Gauthier, and E. Rosenbaum, "A compact, timed-shutoff, MOSFET-based power clamp for on-chip ESD protection," in *Proc. EOS/ESD Symp*., 2004, pp. 273-279.

[6] J.-J. Li, R. Gauthier, S. Mitra, C.Putnam, K. Chatty, R. Halbach, and C. Sequin, "Design and characterization of a multi-RC-triggered MOSFET-based power clamp for on-chip ESD protection," in *Proc. EOS/ESD Symp*., 2006, pp. 179-185.

[7] O. Quittard, Z. Mrcarica, F. Blanc, G. Notermans, T. Smedes, and H. Zwol, " ESD protection for high-voltage CMOS technologies," in *Proc. EOS/ESD Symp*., 2006, pp. 77-86.

[8] J. Smith and G. Boselli, "A MOSFET power supply clamp with feedback enhanced triggering for ESD protection in advanced CMOS technologies," in *Proc. EOS/ESD Symp*., 2003, pp. 8-16.

[9] J. Smith, R. Cline, and G. Boselli, "A low leakage low cost-PMOS based power supply clamp with active feedback for ESD protection in 65 nm CMOS technologies," in *Proc. EOS/ESD Symp*., 2005, pp. 298-306.

[10] *ESD Association Standard Test Method ESD STM5.1-2001, for Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level,* 2001.

[11] M.-D. Ker and C.-C. Yen, "Unexpected failure in power-rail ESD clamp circuits of CMOS integrated circuits in microelectronics systems during electrical fast transient (EFT) test and the re-design solution," in *Proc. IEEE Int. Zurich Symp. on Electromagn. Compat.*, 2007, pp. 69-72.

[12] M.-D. Ker, C.-Y. Wu, T. Cheng, and H.-H. Chang, "Capacitor-couple ESD protection circuit for deep-submicron low-voltage CMOS ASIC," IEEE Trans. VLSI Syst., vol. 4, pp. 307-321, 1996.

[13] *ESD Association Standard Test Method ESD STM5.2-1999, for Electrostatic Discharge Sensitivity Testing – Machine Model (MM) – Component Level,* 1999.