On-Panel Readout Circuit for Capacitive Sensor with LTPS Technology

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New configuration of on-panel readout circuit for capacitive sensor suitable for low temperature polysilicon (LTPS) thin-film transistor (TFT) process has been proposed. In this work, switch capacitor (SC) technique is applied to compensate the impact of threshold voltage (V_{th}) variation owing to LTPS process variation on readout circuit. To further identify the different touch position by conductive object, a 2-bit analog-to-digital converter is used to convert the output of readout circuit into 2-bit digital codes.

1. Introduction

Low temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) have been widely investigated as a material for portable systems, such as digital camera, mobile phone, personal digital assistants (PDAs), notebook, and so on. Furthermore, LTPS technology can achieve slim, compact, and high-resolution display by integrating driving circuits, analog digital converters (ADC), timing controller etc. on the peripheral area of display. Some poly-Si TFT characteristics, such as high carrier mobility, low threshold voltage, high stability, and high reliability, are required to fulfill the SOP application [1], [2].

In last few years, integrating touch panel into glass substrate has attracted much attention because the aforesaid advantages. Touch panels used in mobile applications are mainly resistive or capacitive. Although resistive touch panel can achieve low cost and rarely malfunction, it has some drawbacks including serious glare, low transmittance and single touch only. On the other hand, capacitive touch panel can realize multi-touch functionality easily which allows user to operate information instruments more intuitively [3].

However, because most LTPS TFTs are based on excimer laser crystallized poly-Si, random orientation of poly-Si grains, grain size variation, and incomplete termination of grain boundaries lead to a quite large threshold voltage variation of TFT device which contributes to serious impact on the accuracy of analog circuits [4]-[5].

In this work, a new readout circuit for capacitive sensor on glass in LTPS fabrication process has been proposed. The switch capacitance (SC) technique is used to compensate the threshold voltage variation effect. Different value of sensed capacitance can be judged by ADC. In this way, the overall resolution for touch panel can be enhanced by interpolation method.

2. Equivalent Model of The Capacitive Sensor Line

Capacitive sensor line can be modeled as a series of RC string on the 2.8 inch panel with total R = 150kΩ and C = 100pF shown in Fig. 1. Fanout is the equivalent parasitic RC of interconnect line between the sensor line to the output node Fin. Each node is pre-charged to the supply voltage (VDDA). When conductive objects such as finger touch the surface of touch panel, the touch capacitance Ct is connected to the equivalent circuit. Because of charge sharing, this capacitance results in a voltage variance on the node Fin and the final value of V_{Fin} can be expressed as:

$$V_{Fin} = VDDA \times \frac{Ctotal}{Ctotal + Ct}. \quad (1)$$

where Ctotal = 100pF.

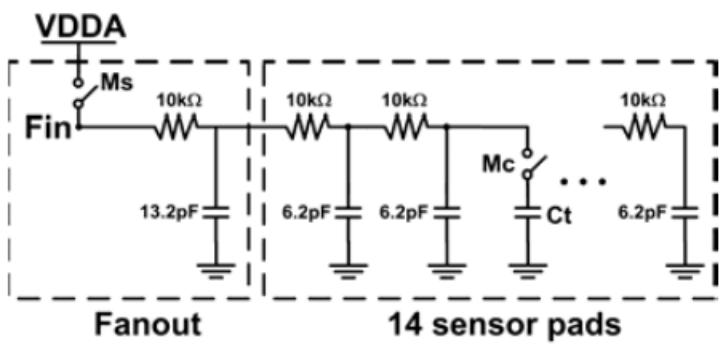


Fig. 1. Equivalent model of the capacitive sensor line on a 2.8 inch touch panel.

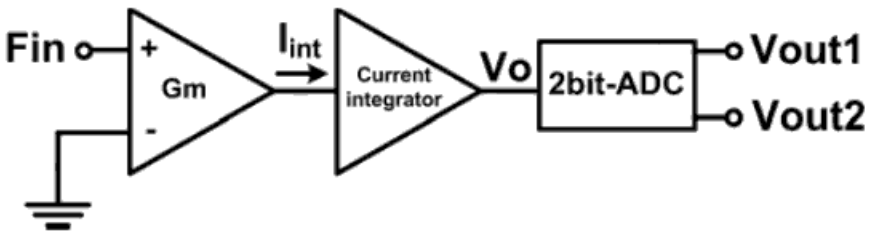


Fig. 2. Block diagram of the new proposed capacitive touch panel readout circuit with 2-bit ADC.

The value of Ct (around 1pF-2pF) is dependent on the distance between touch position and sensor line. Furthermore, different Ct leads to different V_{Fin}. If the value of Ct can be known, interpolation method can be applied to calculate the touch position when the conductive object touches the position between two sensor lines. The proposed readout circuit with 2-bit ADC can distinguish the difference between Ct and further enhances the overall resolution for touch panel.

3. New Proposed Readout Circuit for Capacitive Sensor

In order to reduce the influence of threshold voltage variation, a new readout circuit for capacitive sensor is proposed. The block diagram [6] of the new proposed readout circuit is shown in Fig. 2.

In the first stage, the input voltage is amplified by the transconductance amplifier (Gm amplifier) and transformed into the current Iint which equals to $V_{Fin} \times$ Gm. Secondly, the current Iint is converted into voltage Vo by charging the current integrator. Since Iint is proportional to V_{Fin}, Vo is also proportional to the integration of current Iint. In addition, with 2-bit ADC, the proposed circuit can judge the different V_{Fin} caused by different touch position.

A. Gm Amplifier and Current Integrator

Fig. 3 shows the new proposed capacitive touch panel readout circuit with its timing chart. The circuit consists of five pTFT devices, one nTFT device and a loading capacitance Cout. The transistors M1~M5 are switches and transistor M6 is in the charge of transconducting voltage into current as a Gm amplifier. The timing chart consists of three periods: (1) compensation period, (2) reset period, and (3) amplification period. In the compensation period, M2, M3, M5, and M6 are turned on. The node Va is charged by the supply voltage VDDA until M6 is in cut-off region. The voltage difference between the source and gate of M6 equals to the threshold voltage of M6 (V_{th6}). At meanwhile, the node V_C is set to the supply voltage VDDA. The voltage difference between node Va and V_C is stored in capacitance C1. In the reset period, M2 and M5 are turned off as well as M1 is switched on. Therefore, the output voltage Vo is discharged to ground by M1 and the node Va maintains the same voltage (VDDA-$|V_{th6}|$). During the amplification period, the node Vc is connected to node Fin, dropping a voltage (ΔV) which equals to the voltage difference between VDDA and V_{Fin}. Because of the charge conservation at the node Va, the voltage of node Va also drops ΔV and becomes equal to (VDDA-V_{Fin}-$|V_{th6}|$).

The basic current formula of TFT device can be expressed as following equation:

$$I = \frac{W}{2L}\mu_0 C_{ox}(|V_{GS}| - |V_{th}|)^2 . \qquad (2)$$

where μ_0 is the carrier mobility, L denotes the effective channel length, W is the effective channel width, C_{ox} is the gate oxide capacitance per unit area, V_{th} is the threshold voltage of TFT device. M6 in the amplification period transconducts the voltage of node Va into a current shown in equation (2):

$$I_{M6} = \frac{W}{2L}\mu_0 C_{ox}(VDDA - V_{Fin})^2 . \qquad (3)$$

This current is not relevant to the threshold voltage of TFT device. Using the compensated current charges the loading capacitance Cout which can be seen as current integrator, the impact of threshold voltage variation on the output voltage Vo can be reduced as shown in Fig. 4. When the fixed V_{Fin} and different $|V_{th}|$ values 0.765V, 0.9V and 1.035V are applied, the output voltages Vo for proposed circuit with threshold voltage compensation are almost the same. Compared to the readout circuit without threshold voltage compensation, the current Iint variation in amplification period can be reduced from 54.4% to 10.9%.

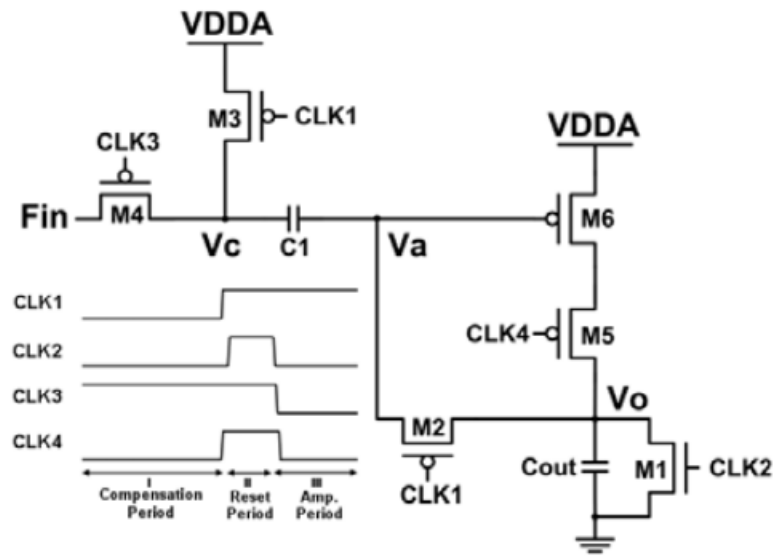
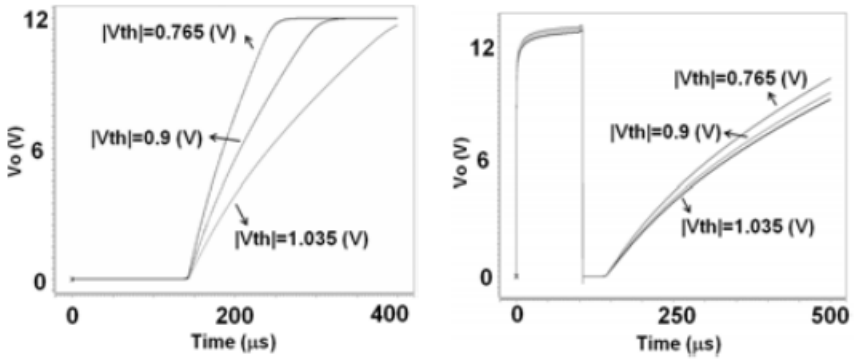


Fig. 3. Schematic of proposed readout circuit with threshold voltage compensation and timing chart for each clock.



(a) (b)

Fig. 4. Simulated results of the proposed readout circuit for capacitive sensor (a) without threshold voltage compensation and (b) with threshold voltage compensation under different threshold voltage.

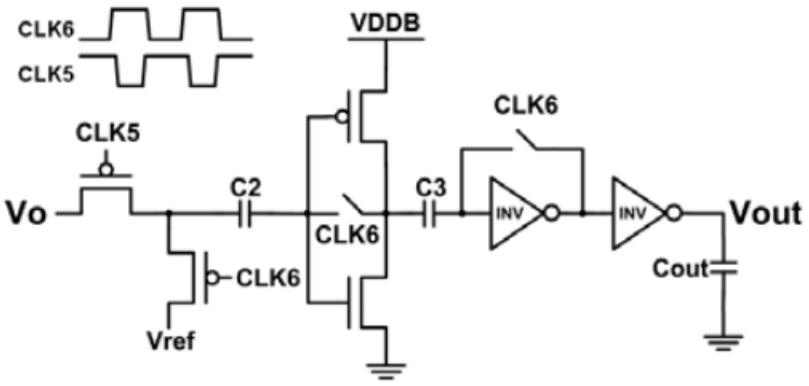


Fig. 5. Circuit configuration of A/D converter.

B. Analog-to-Digital Converter

Fig. 5 shows the configuration of A/D converter suitable for LTPS technology [8], [9]. Switch capacitor technique is applied to cancel the influence of threshold voltage variation of TFT device. All switches are controlled by clock signals CLK5 or CLK6. The circuit operation has two steps, 1) storing the logic threshold voltage $V_{th,log}$ on capacitor and 2) eliminating $V_{th,log}$ and comparing Vo with reference voltage. At first, CLK6 is set to high and the difference between logic threshold voltage $V_{th,log}$ of inverter and Vref is stored on the capacitor C2. In the comparison period, CLK6 is switched to low and CLK5 is set to high. The input voltage of inverter becomes ($Vo+V_{th,log}$-Vref) due to charge conservation. Two inverter stages as buffer are added to guarantee full-swing of the output voltage.

Furthermore, this circuit has immunity from threshold voltage variation since the $V_{th,log}$ is cancelled by storing itself on C2. Two bit resolution is implemented by using two different reference voltages Vref1 and Vref2. The simulation results are shown in Fig. 6. Depending on the digital bits of Vout, different touch position between two sensor lines can be judged and the overall resolution for touch panel can be enhanced.

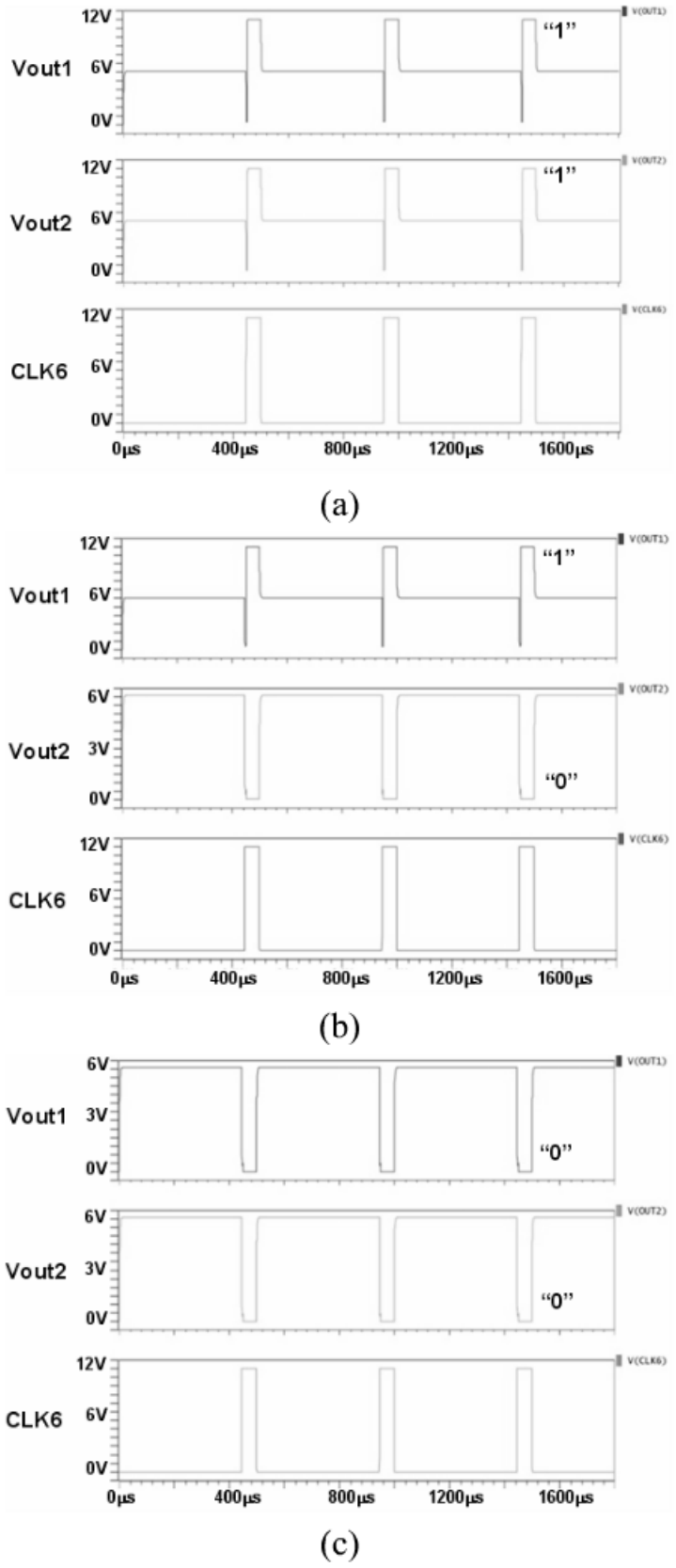


Fig. 6. Simulation results of the proposed circuit with 2 bit-ADC with (a) panel is non-touched (b) Ct = 1pF and (c) Ct = 2pF.

4. Experimental Results

The new proposed readout circuit has been designed and fabricated in a 3-μm LTPS technology. The measurement setup is shown in Fig. 7, where CLK1 and CLK6 are given by HP 81110A pulse/patent generator, CLK2 to CLK5 are assigned by Keithley4200 dual pulse generator, power supply is GPS 4303 DC power supply and the output waveforms are observed by SDO603A oscilloscope. Fig. 8 shows the measured results of the proposed circuit with VDDA = VDDB = 12V, Vref1 = 10.6V and Vref2 = 9.8V.

When CLK6 is high, digital output Vout1 and Vout2 define the value of Ct locates in which interval. "00", "01" and "11" stand for 2pF, 1pF and non-touched respectively. Different capacitance value can be distinguished successfully by the proposed circuit with 2-bit ADC.

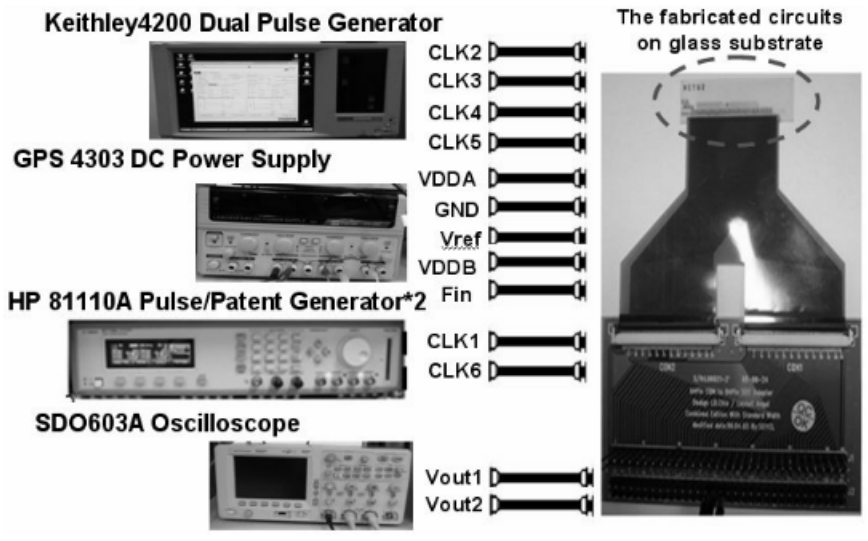


Fig. 7. The fabricated circuits on glass substrate to verify the readout function of the proposed circuit and its corresponding measurement setup.

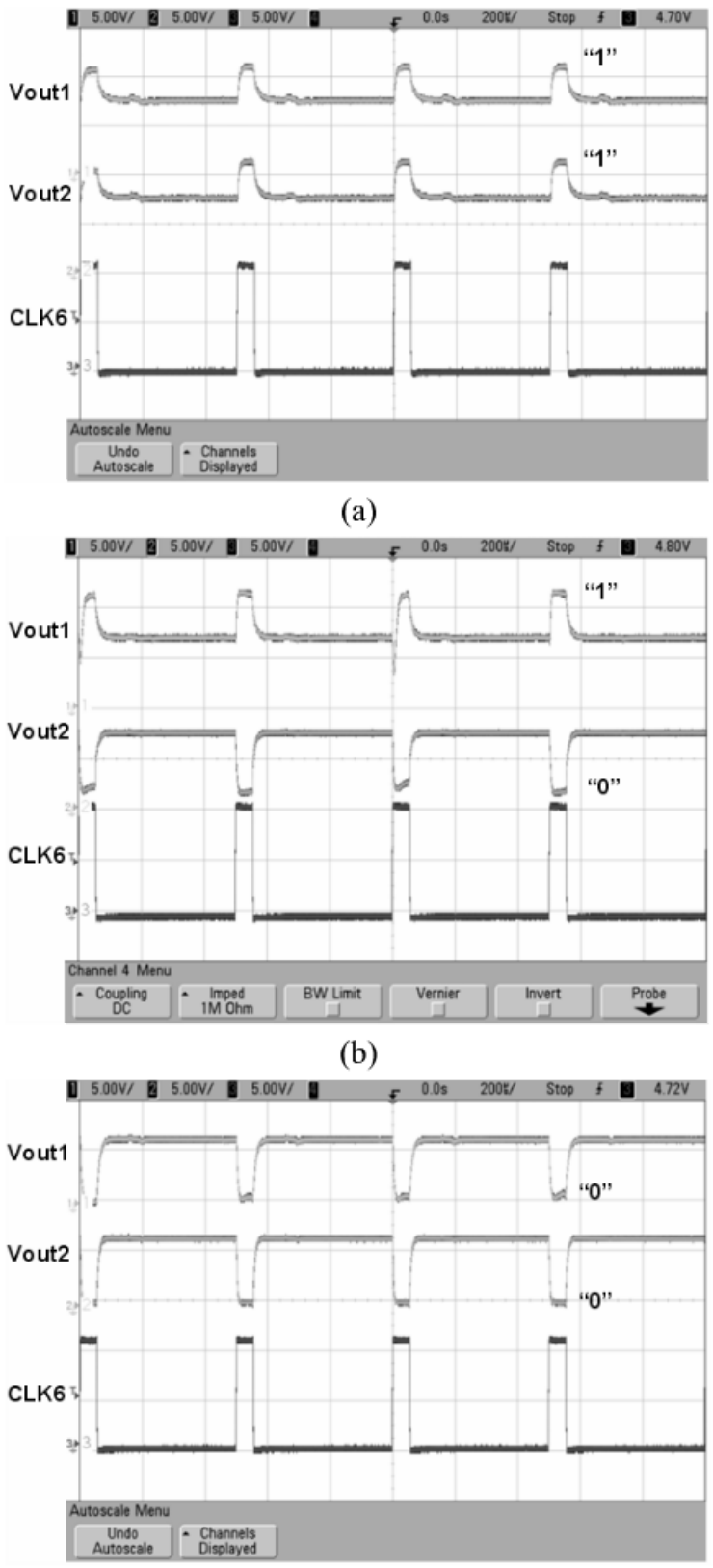


Fig. 8. Measured results of the proposed readout circuit with 2-bit ADC for capacitive sensor with (a) panel is non-touched (b) Ct is 1pF and (c) Ct is 2pF.

5. Conclusions

An analog readout circuit for capacitive sensor on glass substrate for panel application has been successfully designed and fabricated in a 3-μm LTPS technology. By employing switch capacitor technique, the influence of threshold voltage variation can be reduced successfully. This new proposed circuit architecture can not only distinguish the panel is touched or not, but also distinguish different value of touch capacitance and further know the touch position between sensor line.

Acknowledgments

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