

Protection Design Against System-Level ESD Transient Disturbance on Display Panels

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Abstract—A hardware/firmware system co-design has been proposed in this work to protect display electronic products against system-level electrostatic discharge (ESD) transient disturbance. By including transient detection circuit, the firmware can execute system recovery procedure to recover all electrical functions under system-level ESD tests. The transient detection circuit is designed to detect different positive and negative fast electrical transients and verified in a 0.13- μm CMOS process. The experimental results have confirmed that the proposed hardware/firmware design can successfully improve the susceptibility of display products against system-level ESD zapping.

I. INTRODUCTION

The system-level electrostatic discharge (ESD) events have attracted more attention in modern circuits and microelectronic systems [1]-[9]. This tendency results from not only the progress of more integrated functions into a single chip but also from the strict requirements of reliability test standards, such as the system-level ESD test standard of IEC 61000-4-2 [10]. Typically, if microelectronic products are required to achieve the immunity of “level 4” in the IEC 61000-4-2 standard, the equipment under test (EUT) should sustain the ESD stress level of as high as ± 8 kV (± 15 kV) under contact-discharge (air-discharge) test mode. Such high-energy ESD-induced electrical transients often cause damage or malfunction to CMOS ICs inside the EUT. For example, a notebook under the system-level ESD test in the air-discharge test mode is shown in Fig. 1. The inset figure in Fig. 1 depicts a typical ESD-generated voltage waveform coupled to the power pins of CMOS ICs in the EUT under the system-level ESD test. Such ESD-generated transient voltage is quite large and randomly exists on power, ground, or I/O pins of ICs inside the microelectronic system. The CMOS ICs inside the microelectronic products are very susceptible to system-level electrical transient disturbance [11]-[13], even though they have passed the component-level ESD specifications such as human-body-model (HBM) of ± 2 kV, machine-model (MM) of ± 200 V, and charged-device-model (CDM) of ± 1 kV.

Component-level ESD tests often cause physical damage in a chip. For microelectronic systems with CMOS integrated circuits (ICs), system-level ESD tests often cause soft errors, including upset or locked states in the system. Typical on-chip ESD protection circuits in CMOS ICs can protect the internal circuits against ESD damage, but they can not release the locked or frozen states in microelectronic products under

system-level ESD tests. In IEC 61000-4-2 standard, four classifications of system-level ESD test results have been defined, as listed in Table I. Most microelectronic products are required to automatically recover the system functions without operator intervention to meet the “class B” criterion by IC industry [14], [15].

In this paper, a hardware/firmware system co-design including transient detection circuit has been proposed to protect display products against system-level ESD transient disturbance. The transient detection circuit is designed to detect fast electrical transients and verified in a 0.13- μm CMOS process. The experimental results have confirmed that the proposed hardware/firmware design can successfully improve the susceptibility of display products against system-level ESD zapping.

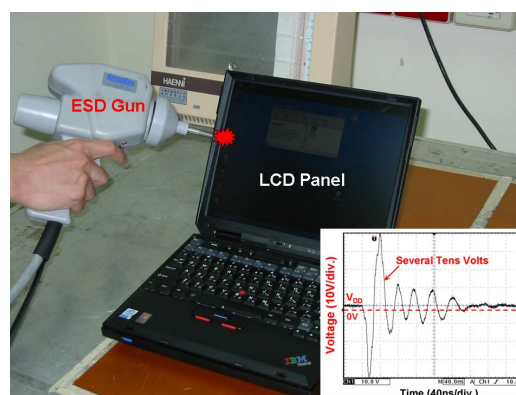


Fig. 1 System-level ESD test on a notebook with air-discharge mode. The inset figure depicts a typical waveform of transient noise voltage coupled to the power pin of CMOS ICs in the EUT.

TABLE I
RECOMMENDED CLASSIFICATIONS OF SYSTEM-LEVEL ESD TEST RESULTS

Criterion	Recommended Classification
Class A	Normal performance within limits specified by the manufacturer, requestor or purchaser.
Class B	Temporary loss of function or degradation of performance which ceases after the disturbance ceases, and from which the equipment under test recovers its normal performance, without operator intervention. (Automatic Recovery)
Class C	Temporary loss of function or degradation of performance, the correction of which requires operator intervention. (Manual Recovery)
Class D	Loss of function or degradation of performance which is not recoverable, owing to damage to hardware or software, or loss of data.

II. Display System Design for System-Level ESD Protection

A. Display System

For display system with thin-film transistor (TFT) liquid crystal display (LCD) panel, multiple power systems are needed for electrical display functions, as shown in Fig. 1. For example, in the backside of source driver IC, the analog power line (VDDA) is used for digital-to-analog converter circuit and digital power line (VDDD) is used for shifter register to store red, green, and blue (RGB) display signals. It has been reported, under system-level ESD test, the ESD energy can couple through the indium tin oxide (ITO) film from LCD panel into the driver ICs to cause display malfunction, as shown in Fig. 2 [13]. During the system-level ESD test, the power and ground lines of the driver ICs inside the display product no longer maintain normal voltage levels, but an underdamped sinusoidal voltage with the amplitude of several tens volts occurred. In this work, the transient detection circuit is connected with the VDDD power line to detect and memorize the occurrence of ESD-induced transient disturbance coupled on digital subsystem of display products. The output signal of transient detection circuit can be used as the system recovery index to protect display products against system-level ESD transient disturbance.

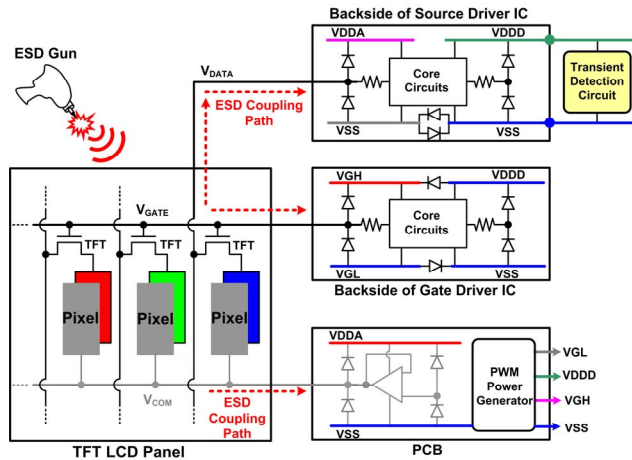


Fig. 2. Display system with TFT LCD panel and coupling paths under system-level ESD tests.

B. Hardware/Firmware System Co-Design

It had been proven that the hardware/firmware co-design can effectively improve the robustness of the microelectronic products against system-level ESD stresses [9]. To perform the hardware/firmware co-design, the detection result from the transient detection circuit can be temporarily stored as a system recover index for firmware check. For example, the output (V_{OUT}) state of the transient detection circuit is initially reset to logic “1”, in the beginning by the power-on reset circuit. When the electrical transients happen, the transient detection circuit can detect the occurrence of system-level electrical transient disturbance and transit the output state (V_{OUT}) to logic “0.” At this moment, the system check index is also changed to logic “0” to initiate firmware recover

procedure to restore system to a known stable state as soon as possible. After the recover procedure, the output of the transient detection circuit and the firmware index are re-set to logic “1” again for detecting the next electrical transient disturbance events. The firmware flowchart is shown in Fig. 3.

Under the normal power-on condition, the V_{DD} power-on voltage waveform has a rise time in the order of millisecond (ms). As there is no input signal except power-on voltage waveform, the power-on reset circuit is often designed with the internal delay longer than the rise time of the power-on transition. The transient detection circuit is designed to detect the ESD-induced fast electrical transients in the range of nanosecond (ns). However, if the power-on reset circuit would be mis-triggered under electrical transient disturbance, a two-input OR logic gate circuit can be further added into the hardware/firmware co-design flow. The output signals of power-on reset circuit and transient detection circuit are connected as the two input signals of OR logic gate. When electrical transient disturbance happens, the system recovery procedure can be still initiated to protect microelectronic products against the electrical transitions from system-level ESD events.

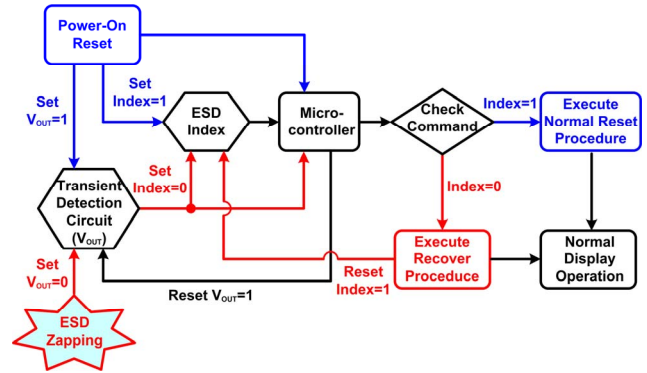


Fig. 3. Firmware flowchart to recover display system when electrical transients happen.

C. Transient Detection Circuit

Fig. 4 shows the RC-based transient detection circuit. The two-inverter latch (INV_2 and INV_3) is designed to memorize the logic state before and after system-level ESD stress. The NMOS (M_{nr}) is used to provide the initial reset function to set the initial output voltage (V_{OUT}) level to 1.8 V.

In Fig. 3, the node V_X is biased at V_{DD} and the node V_G is biased at V_{SS} under the normal circuit operation condition. During the system-level ESD test, the ESD voltage has a fast rise time in the order of nano-second (ns). The voltage level at V_X has a much slower voltage response than the voltage level at V_{DD} because the RC circuit has a time constant in the order of micro-second (μs). Due to the longer delay of voltage increase at the node V_X , the PMOS device in the inverter1 (INV_1) can be turned on by the overshooting ESD voltage and conducts a voltage to the node V_G to further turn on the M_{n1} device. The turned-on M_{n1} device will pull down the voltage level at the node V_A to V_{SS} . Therefore, the original logic state stored in the two-inverter latch can be changed to

detect the electrical transient disturbance caused by system-level ESD events. The output voltage (V_{OUT}) of the transient detection circuit is finally transited from 1.8 V (V_{DD}) to 0 V (V_{SS}) to memorize the occurrence of system-level ESD events.

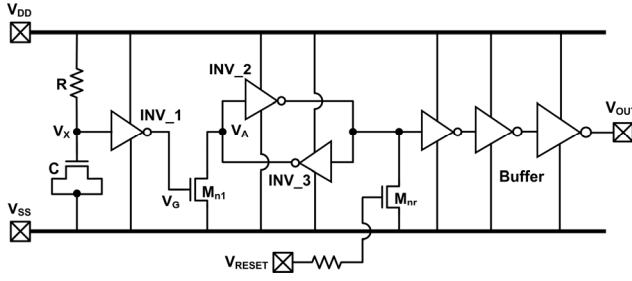


Fig. 4 The transient detection circuit.

III. SYSTEM-LEVEL ESD TEST

A. Measurement Setup

In the IEC 61000-4-2 standard [10], the equipment specifications for different testing modes have been defined. For table-top equipment, the measurement set-up should consist of a wooden table, standing on the ground reference plane (GRP). An insulating plane should be inserted between the EUT/cables and horizontal coupling plane (HCP).

In the IEC 61000-4-2 standard, two test modes have been also specified, which are the air-discharge test mode and the contact-discharge test mode. Under system-level ESD tests, the ESD energy is released from ESD gun. Different discharge tips are used for two different discharge test modes. The round tip of ESD gun is used for air-discharge test and brought close to the EUT. The sharp tip of ESD gun is used for contact-discharge test and held in contact with the EUT. The measurement setup of system-level ESD test with the air-discharge test mode in IEC 61000-4-2 standard is shown in Fig. 5. The round discharge tip should be approached as fast as possible to touch the EUT. The air discharge is actuated by a spark to the EUT and the ESD energy holding time is at least 5 seconds. Under system-level ESD zapping conditions, the transient voltage coming from ESD will be coupled into all CMOS ICs inside EUT. The operations of CMOS ICs inside EUT would be disturbed by the ESD-coupled energy.

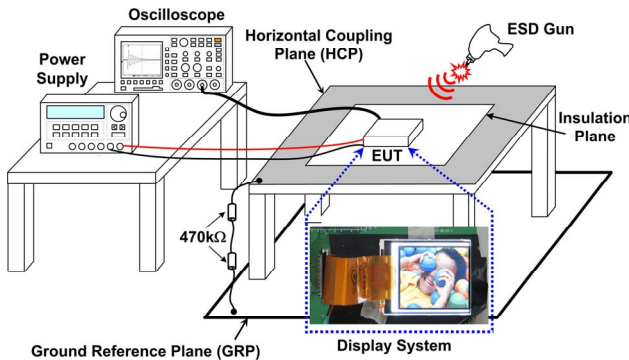


Fig. 5 Measurement setup for a system-level ESD test with air-discharge test mode.

B. Experimental Results

In this work, the output signal of transient detection circuit is connected to the microcontroller of display system. When the electrical transients happen, the transient detection circuit can detect the occurrence of system-level electrical transient disturbance and transit the output state (V_{OUT}) to logic "0." After checking the ESD index, the firmware can execute recovery procedure to recover system electrical functions to a stable state as soon as possible. The measurement setup shown in Fig. 5 can verify the circuit performance of transient detection circuit designed with the display system under system-level ESD test with air-discharge mode. The V_{DD} line of transient detection circuit is connected to the digital power line (V_{DDD}) of display system.

By using the digital oscilloscope, the transient responses on power lines and output signals of transient detection circuit inside the display products can be recorded and analyzed. Before each system-level ESD test, the initial output voltage (V_{OUT}) of the transient detection circuit is reset to 1.8 V by power-on firmware procedure. After each system-level ESD test, the output voltage (V_{OUT}) level is monitored to check the final voltage level and to verify the detection function. When the locked or frozen states of display products are released by such a hardware/firmware co-design, the LCD panel can continually show the normal display information without malfunction under system-level ESD tests.

The transient detection circuit has been designed and fabricated in a 0.13- μm CMOS process with 1.8-V devices. The measured V_{DD} and V_{OUT} waveforms of the transient detection circuit under a system-level ESD test with the ESD voltage of +4 kV zapping are shown in Fig. 6(a). V_{DD} begins to increase rapidly from the normal bias voltage of 1.8V. Meanwhile, V_{OUT} begins to change under such a high-energy ESD stress. During the fast transient disturbance, V_{DD} and V_{OUT} are influenced simultaneously. Finally, the output voltage of the transient detection circuit has been changed from 1.8 V to 0 V.

The measured V_{DD} and V_{OUT} transient waveforms of the transient detection circuit under system-level ESD test with an ESD voltage of -4 kV zapping are shown in Fig. 6(b). During the ESD-induced transient disturbance, V_{DD} begins to decrease rapidly from the original bias voltage of 1.8 V and V_{OUT} is disturbed simultaneously. Finally, V_{OUT} is pulled down to 0 V after the system-level ESD test. Therefore, the transient detection circuit can detect the electrical transient under system-level ESD test with negative ESD voltage.

From the system-level test results shown in Figs. 6(a) and 6(b), with positive or negative underdamped sinusoidal voltage waveforms coupled to power lines, the output voltages (V_{OUT}) of the transient detection circuit can be changed from 1.8 V to 0 V. Therefore, the transient detection circuit inside the display products can successfully detect the occurrence of ESD-induced transient disturbance and provide output signal as system recovery index.

The susceptibility of the display system with and without transient detection circuit are compared in Table II. By using the detection results as the firmware index, the display system

can automatically recover all electrical functions to release the locked or frozen states caused by system-level ESD transient disturbance. With such a hardware/firmware system co-design, the classification of display products under system-level ESD tests with ± 4 -kV ESD voltage level can be improved from “class C” to “class B” criterion. The transient detection circuit can further integrate into internal circuits and provide chip-level solutions to meet high transient disturbance immunity specification for microelectronic products against system-level ESD transient disturbance.

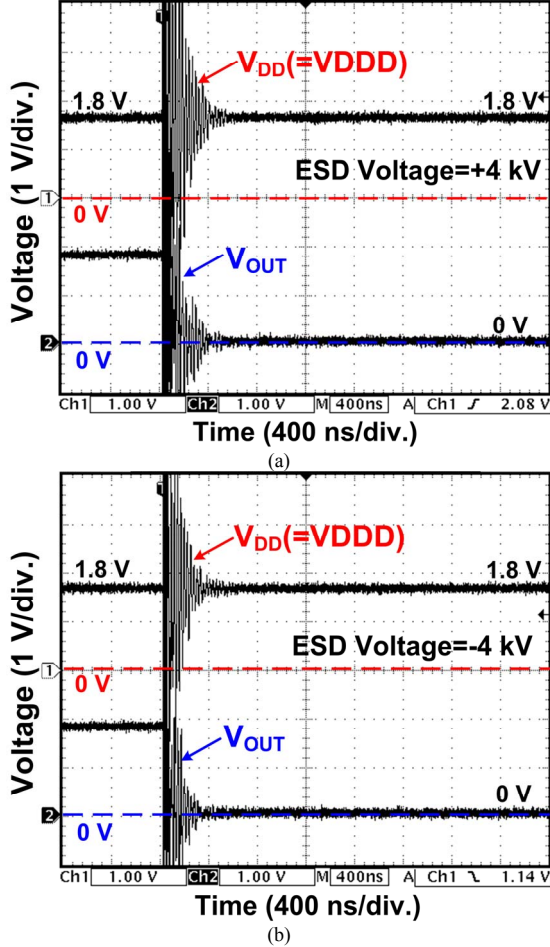


Fig. 6. Measured V_{DD} and V_{OUT} transient responses with ESD voltage of (a) +4 kV, and (b) -4 kV, zapping under system-level ESD test.

TABLE II

COMPARISON ON THE CLASSIFICATIONS BETWEEN DISPLAY SYSTEM WITH AND W/O TRANSIENT DETECTION CIRCUIT UNDER SYSTEM-LEVEL ESD TEST

Display System \ ESD Level	+4kV	-4kV
W/o Transient Detection Circuit	Class C	Class C
With Transient Detection Circuit	Class B	Class B

IV. CONCLUSIONS

A hardware/firmware system co-design including transient detection circuit has been proposed to protect display products under system-level ESD tests. The transient detection circuit is designed to detect fast electrical transients and verified in a 0.13- μ m CMOS process. The experimental results have confirmed that the proposed hardware/firmware design can successfully improve the susceptibility of display products from “class C” to “class B” criterion. Under system-level ESD tests, the display system can automatically recover all electrical functions without operator intervention. With hardware/firmware co-design, the transient detection circuit can be used as firmware index to provide an effective solution against the malfunction in microelectronic products caused by system-level electrical transient disturbance.

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