

ESD Protection Design for Differential Low-Noise Amplifier With Cross-Coupled SCR

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Abstract—A new electrostatic discharge (ESD) protection scheme for differential low-noise amplifier (LNA) was proposed in this paper. The new ESD protection scheme, which evolved from the conventional double-diode ESD protection scheme without adding any extra device, was realized with cross-coupled silicon-controlled rectifier (SCR). With the new ESD protection scheme, the pin-to-pin ESD robustness can be improved, which was the most critical ESD-test pin combination for differential input pads. Experimental results had shown that differential LNA with cross-coupled-SCR ESD protection scheme can achieve excellent ESD robustness and good RF performances.

I. INTRODUCTION

As the feature size of MOS transistor in CMOS technology is continuously scaled down to improve the high-frequency characteristics, the advanced nanoscale CMOS technology is more attractive to implement radio-frequency (RF) circuits. In an RF front-end, the low-noise amplifier (LNA) plays a very important role because it is the first stage in the RF receiver. In LNA design, differential configuration is popular because the differential LNA has the advantages of better common-mode noise rejection, as well as less sensitivity to substrate noise, supply noise, and bond-wire inductance variation [1], [2]. In addition, the differential output signals of the differential LNA can be directly connected to the differential inputs of the double balanced mixer.

With the evolution of CMOS technology, the electrostatic discharge (ESD) protection design in nanoscale CMOS process becomes more challenging [3]. The ESD protection design should be taken into consideration during the design phase of RF circuits to achieve satisfactory ESD robustness without seriously degrading circuit performances [4]. Since the LNA is usually connected to the external of the RF receiver chip such as the off-chip antenna, on-chip ESD protection circuits are needed for all input pads of the LNA. However, applying ESD protection circuits at the input pads

inevitably introduce some impacts from parasitics to RF performance. There are several ESD protection designs reported for RF front-end circuits to optimize RF performance and ESD robustness [5]-[7]. Some ESD protection designs have been presented to improve ESD robustness of LNA under pin-to-pin ESD stresses, since the pin-to-pin ESD stress was one of the most critical ESD events for differential input pads [5].

In this paper, a new ESD protection design is proposed to protect the differential LNA in a 130-nm CMOS process. The pin-to-pin ESD robustness is substantially improved by the new proposed ESD protection scheme in this work.

II. CONVENTIONAL DOUBLE-DIODE ESD PROTECTION SCHEME

The conventional double-diode ESD protection scheme for differential LNA is shown in Fig. 1. The P+/N-well diodes (D_P) are connected between each input pads and VDD, while the N+/P-well diodes (D_N) are connected between each input pads and VSS. To co-design the input matching network of LNA with ESD protection diodes, the source inductors (L_{S1} and L_{S2}) and gate inductors (L_{G1} and L_{G2}) are adjusted to achieve impedance match at the operating frequency.

Besides ESD protection diodes, the power-rail ESD clamp circuit is used to provide ESD current paths between VDD and VSS under ESD stresses. The power-rail ESD clamp circuit is placed between VDD and VSS, so it does not contribute any parasitic effects to input pads. During positive-to-VDD-mode (PD-mode) and negative-to-VSS-mode (NS-mode) ESD stresses, ESD current is discharged through the forward-biased D_P and D_N , respectively. During positive-to-VSS-mode (PS-mode) ESD stress, ESD current is discharged from the RF IN pad through the D_P and the power-rail ESD clamp circuit to VSS. Similarly, during negative-to-VDD-mode (ND-mode) ESD stress, ESD current is discharged from the VDD through the power-rail ESD clamp circuit and the D_N to the RF IN pad. Under pin-to-pin ESD stress, ESD current is discharged from the RF IN₁ (RF IN₂) pad through the D_{P1} (D_{P2}), the power-rail ESD clamp circuit, and the D_{N2} (D_{N1}) to RF IN₂ (RF IN₁) pad.

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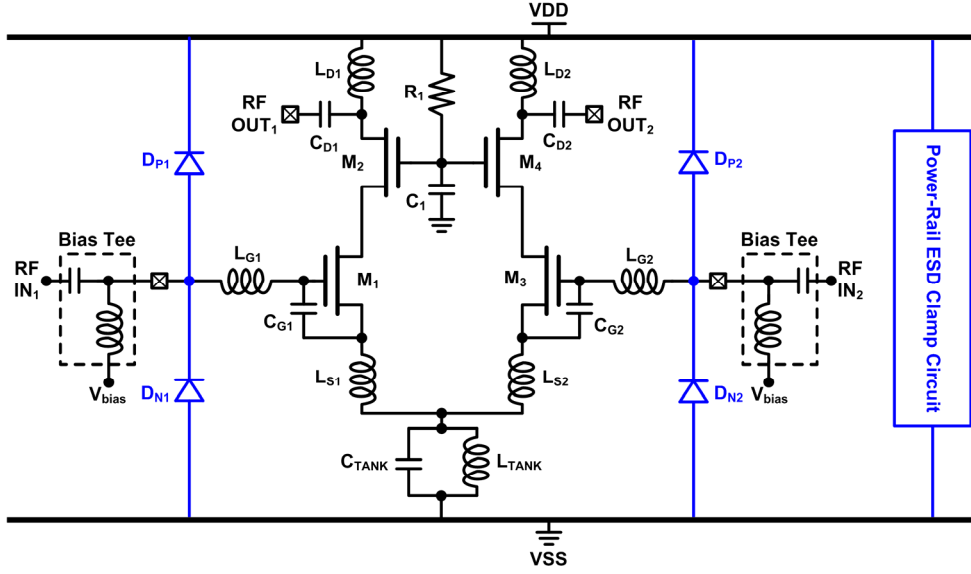


Figure 1. Conventional double-diode ESD protection scheme for differential LNA.

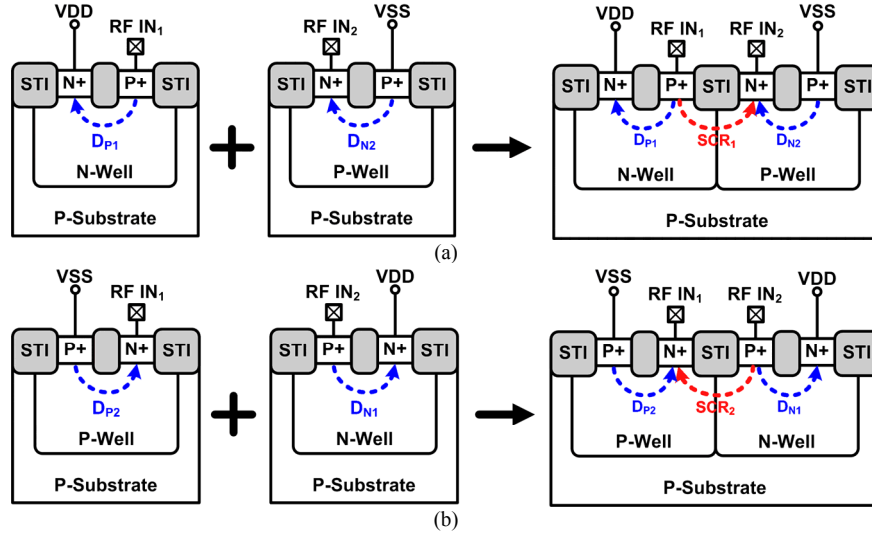


Figure 2. Establishing SCR paths from (a) RF IN₁ to RF IN₂, and (b) RF IN₂ to RF IN₁, by combining P+/N-well diodes with N+/P-well diodes.

This ESD protection scheme provides the corresponding current discharging paths for all ESD-test pin combinations.

III. NEW CROSS-COUPLED-SCR ESD PROTECTION SCHEME

Fig. 2 illustrates the concept of the proposed ESD protection scheme. The four ESD protection diodes at the differential input pads in the double-diode ESD protection scheme are reserved in this new design, but the placement is changed. In this new ESD protection scheme, the silicon-controlled rectifier (SCR) path is established directly from one differential input pad to the other differential input pad without adding any extra device. As illustrated in Fig. 2(a), by merging D_{P1} and D_{N2} together, an SCR path (SCR_1) from RF IN₁ pad to RF IN₂ pad can be established for pin-to-pin ESD protection. Similarly, D_{P2} and D_{N1} can be merged together to form another SCR path (SCR_2) from RF IN₂ pad to RF IN₁

pad, as illustrated in Fig. 2(b). The SCR path has very high ESD robustness due to its low clamping voltage under ESD stress conditions [8]. Since the pin-to-pin ESD path is established by SCR, the cross-coupled-SCR ESD protection scheme is expected to have high pin-to-pin ESD robustness. Under PD-, PS-, ND-, and NS-mode ESD stresses, the ESD levels are not altered, since D_{P1} , D_{N1} , D_{P2} , and D_{N2} still exist.

The circuit schematic of the differential LNA with the new proposed ESD protection scheme of cross-coupled SCR is shown in Fig. 3. The SCR_1 is placed close to the RF IN₁ pad to provide efficient pin-to-pin ESD current path from the RF IN₁ pad to the RF IN₂ pad. Similarly, the SCR_2 is placed close to the RF IN₂ pad to provide efficient ESD current path from the RF IN₂ pad to the RF IN₁ pad under pin-to-pin ESD stresses. To reduce the trigger voltage and increase the turn-on speed of the SCR under ESD stresses, the substrate-triggered technique is used [8]. The trigger port of SCR is connected to the ESD

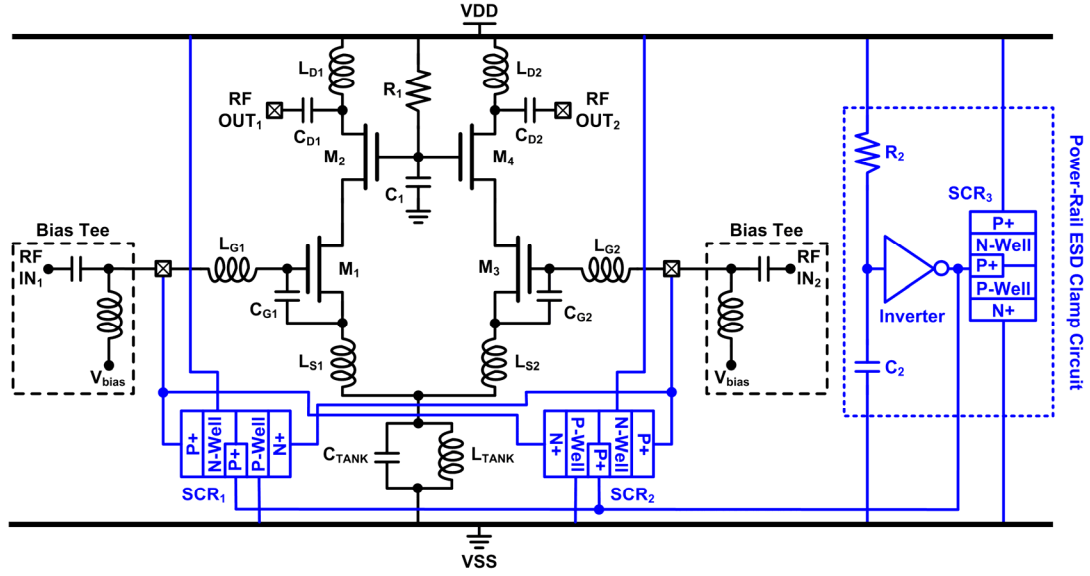


Figure 5. New cross-coupled-SCR ESD protection scheme for differential LNA.

detection circuit in the power-rail ESD clamp circuit. Under pin-to-pin ESD stress, the ESD detection circuit outputs trigger current to the trigger port of SCR₁ or SCR₂. As a result, the SCR₁ or SCR₂ is turned on to provide ESD current path between RF IN₁ and RF IN₂ pads. Under normal circuit operating conditions, the ESD detection circuit and the SCR are kept off.

The test circuits have been fabricated in a 130-nm CMOS process. The total parasitic capacitance from the cross-coupled SCR at each input pad is specified as 300 fF. To achieve the total parasitic capacitance of 300 fF at each differential input pad, the sizes of SCR₁ and SCR₂ are all drawn as 60 $\mu\text{m} \times 2.4 \mu\text{m}$ in layout. The source inductors (L_{S1} and L_{S2}) and gate inductors (L_{G1} and L_{G2}) are adjusted to achieve the input matching of LNA with the cross-coupled SCR.

IV. EXPERIMENTAL RESULTS

The human-body-model (HBM) and machine-model (MM) ESD levels of differential LNA with the proposed cross-coupled-SCR ESD protection scheme under different test pin combinations are listed in Table I. The ESD test results show that the differential LNA with cross-coupled-SCR ESD protection scheme can sustain pin-to-pin ESD stresses of over 8-kV HBM and 800-V MM. The proposed ESD-protected differential LNA in this work exhibits excellent ESD robustness, especially in the pin-to-pin ESD stresses.

The measured RF performances of the differential LNA with cross-coupled-SCR ESD protection scheme are compared with those of the original differential LNA without ESD protection in Figs. 4~7. To compare the input matching conditions, the measured S_{11} -parameters of these two differential LNAs are shown in Fig. 4. It is observed that the operating frequency of the differential LNA with cross-coupled-SCR ESD protection scheme is shifted from 5 GHz to 4.8 GHz. At 4.8-GHz, the measured S_{11} -parameter is -26.3 dB. The shift in the operating frequency is due to the lack of RF model for SCR device in the given CMOS process. To more

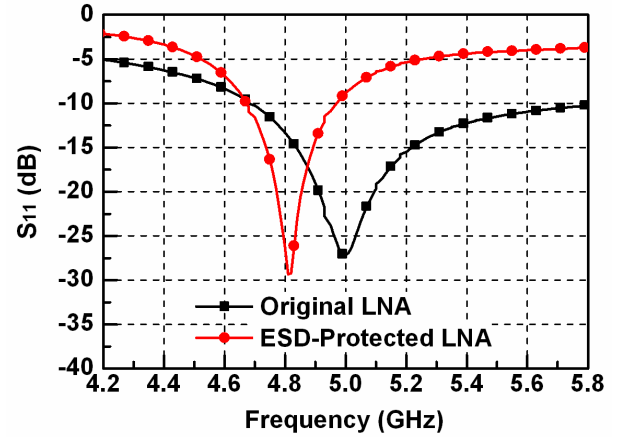


Figure 3. Measured S_{11} -parameters of differential LNA with and without cross-coupled-SCR ESD protection.

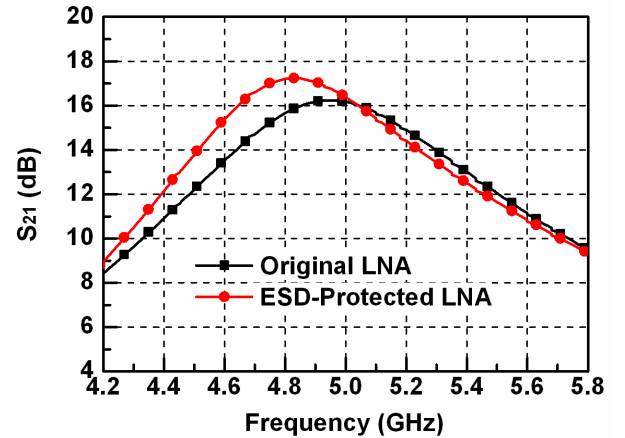


Figure 4. Measured S_{21} -parameters of differential LNA with and without cross-coupled-SCR ESD protection.

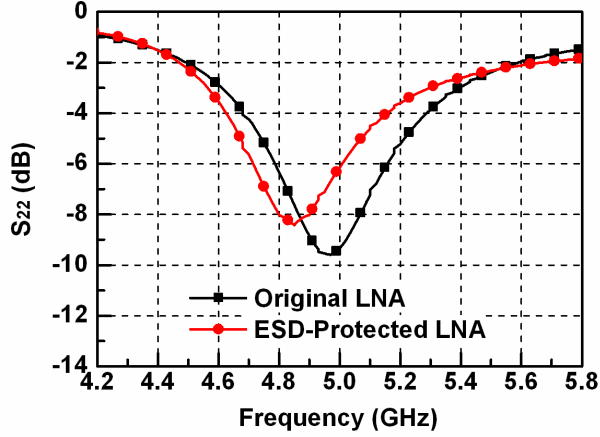


Figure 6. Measured S_{22} -parameters of differential LNA with and without cross-coupled-SCR ESD protection.

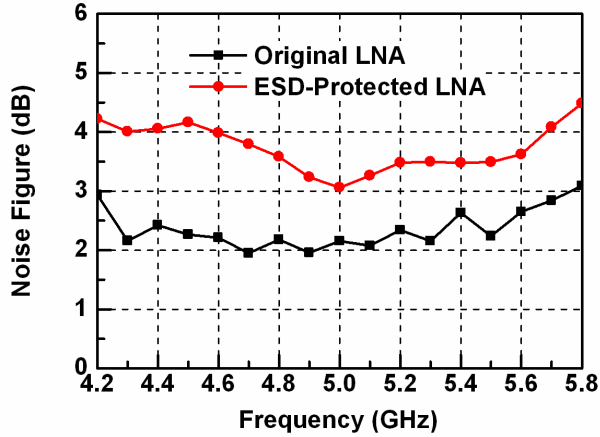


Figure 7. Measured noise figures of differential LNA with and without cross-coupled-SCR ESD protection.

precisely simulate the differential LNA with the cross-coupled-SCR ESD protection scheme, the parasitic effects of the SCR can be modeled by the diodes with P+/N-well, P-well/N-well, and N+/P-well junctions, rather than only the 300-fF capacitance. Fig. 5 compares the measured S_{21} -parameters (power gains) of these two differential LNAs. At 4.8 GHz, the S_{21} -parameter of differential LNA with cross-coupled-SCR ESD protection scheme is 17.2 dB. The S_{22} -parameter of differential LNA with cross-coupled-SCR ESD protection scheme is -8 dB at 4.8 GHz, as shown in Fig. 6.

Fig. 7 shows the measured noise figures of these two differential LNAs. At 4.8 GHz, the noise figure of differential LNA with cross-coupled-SCR ESD protection scheme is 3.58 dB. The increase in the noise figure is attributed to the parasitic effects of ESD protection devices with the overlapped wide metal lines in layout, which are connected between the differential input pads and the cross-coupled SCR devices. These measured performances of the differential LNA with and without cross-coupled-SCR ESD protection scheme are also summarized in Table I.

TABLE I. COMPARISON BETWEEN FABRICATED DIFFERENTIAL LNAs

		Original LNA	ESD-Protected LNA
ESD Robustness	Positive to VSS (HBM / MM)	< 50 V / < 10 V	3.5 kV / 300 V
	Negative to VDD (HBM / MM)	< 50 V / < 10 V	3.5 kV / 350 V
	Pin to Pin (HBM / MM)	< 50 V / < 10 V	> 8 kV / 800 V
	VDD to Vss (HBM / MM)	0.5 kV / < 10 V	> 8 kV / >1000 V
RF Performance	Operating Frequency	5 GHz	4.8 GHz
	Power Consumption	10.3 mW	10.3 mW
	S_{11}	-27.2 dB	-26.3 dB
	S_{21}	16.2 dB	17.2 dB
	Noise Figure	2.16 dB	3.58 dB

V. CONCLUSION

The new ESD protection scheme of cross-coupled SCR is realized without adding any extra device, as compared with the conventional double-diode ESD protection scheme. The differential LNA with the new cross-coupled-SCR ESD protection scheme can improve the pin-to-pin ESD robustness, which was the most critical ESD-test pin combination for differential input pads. Verified in a 130-nm CMOS process, the pin-to-pin ESD robustness of the differential LNA with the proposed cross-coupled-SCR ESD protection scheme has been substantially improved. The proposed ESD protection scheme co-designed with the differential LNA can achieve good RF performances and high ESD robustness simultaneously.

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