

New Transient Detection Circuit for Electrical Fast Transient (EFT) Protection Design in Display Panels

Ming-Dou Ker, Wan-Yen Lin, Cheng-Cheng Yen, Che-Ming Yang, Tung-Yang Chen, and Shih-Fan Chen

Abstract—A new transient detection circuit against electrical fast transient (EFT) disturbance is proposed for display panel protection. The circuit function to detect positive or negative electrical transients under EFT tests has been investigated in HSPICE simulation and verified in silicon chip. The output of the proposed transient detection circuit can be used as a firmware index to execute system automatic recovery operation. With hardware/firmware co-design, the immunity of display panel against transient disturbance under EFT tests can be significantly improved.

Index Terms —electromagnetic compatibility, electrical fast transient (EFT) test, transient detection circuit.

I. INTRODUCTION

Electrical fast transient (EFT) event has become an important reliability issue to microelectronic systems equipped with CMOS integrated circuits (ICs) [1]–[3]. This tendency results from not only the progress of more functions integrated into a single chip but also from the strict requirements of reliability test standards, such as the EFT test. The microelectronic product must sustain the EFT voltage level of ± 2 kV under EFT tests to achieve the immunity requirement of “level 4” in the IEC 61000-4-4 test standard [4]. During EFT tests, the power lines of the CMOS ICs in the microelectronic products no longer maintained normal voltage levels, but an exponential voltage pulse with the amplitude of several tens volts occurred, as shown in Fig. 1. The measured voltage waveform of a single pulse has a rise time of about ~ 5 ns and the pulse duration of ~ 50 ns. With the scaled clearance between PMOS and NMOS devices in advanced semiconductor technology, it has been proven that such EFT-induced electrical transient noises can cause transient-induced latchup (TLU) failure on the inevitable parasitic silicon controlled rectifier (SCR) in CMOS ICs. The high-voltage electrical fast transients often cause CMOS ICs inside the equipment under test (EUT) to be upset or frozen after the EFT-induced electrical transient disturbance. The CMOS ICs inside the microelectronic products are very susceptible to electrical transient disturbance

[5]–[12], even though they have passed the component-level ESD specifications such as human-body-model (HBM) of ± 2 kV, machine-model (MM) of ± 200 V, and charged-device-model (CDM) of ± 1 kV.

In order to solve such EFT issues, the traditional solution is to add some board-level noise filters into the microelectronic products to decouple, bypass, or absorb the electrical transients under EFT tests [12], [13]. However, with more functions integrated into a system-on-a-chip (SOC), such additional discrete noise-bypassing components may not be integrated into a single chip due to the limitation of chip area and substantially increase in the fabrication cost of microelectronic products. Therefore, to meet high EFT specifications for microelectronic products, the chip-level solutions without additional discrete components on the printed circuit board (PCB) are highly desired by the IC industry [15]–[17].

In this work, a new on-chip transient detection circuit is designed to detect electrical transient disturbance under EFT tests and verified in a $0.13\text{-}\mu\text{m}$ CMOS process. The circuit function to detect different positive or negative electrical transients has been investigated by HSPICE simulation. The EFT generator with attenuation network is used to evaluate the detection function of the proposed transient detection circuit. The proposed circuit can provide a hardware/firmware co-design solution to improve the susceptibility of microelectronic systems against EFT-induced electrical transient disturbance.

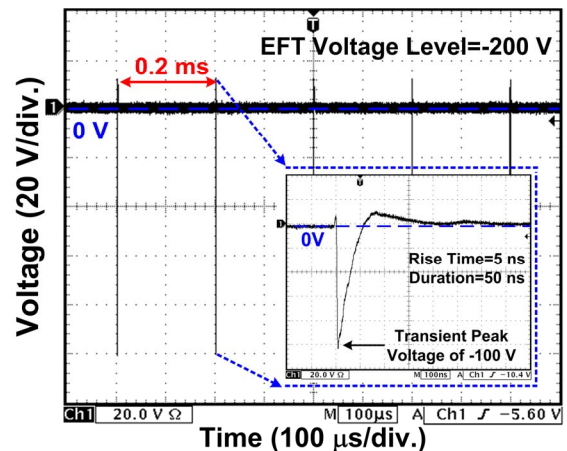


Fig. 1. Measured EFT transient voltage waveforms on a $50\ \Omega$ load with repetition rate of 5 kHz.

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II. NEW PROPOSED TRANSIENT DETECTION CIRCUIT

A. Circuit Implementation

In the previous proposed transient detection circuit [15], the detection sensitivity can be adjusted by the device ratio in the latch circuit and additional capacitors. However, the detection sensitivity could be degraded by the large on-chip decoupling capacitors between power lines in the CMOS IC products.

In this work, a new on-chip transient detection circuit has been proposed, as shown in Fig. 2. The RC-based circuit structure is designed to realize the transient detection function. The NMOS (M_{nr}) is used to provide the initial reset function to set the initial output voltage (V_{OUT}) as 1.8 V with the V_{DD} of 1.8 V in a 0.13- μm CMOS process. In Fig. 2, the node V_X is biased at V_{DD} during the normal operating condition. With the feedback loop connected between the output node of inverter1 (inv1) and the gate of NMOS device (M_{n1}), the node V_A can be kept at V_{SS} of 0 V after initial reset operation. Under the EFT zapping conditions, the EFT voltage has a fast rise time in the order of nanosecond (ns). The voltage level of V_X has much slower voltage response than the voltage level at V_{DD} because the RC circuit has a time constant in the order of microsecond (μs). Due to the longer delay of the voltage increase at the node V_X , the PMOS device (M_{p1}) can be turned on by the overshooting EFT voltage (coupled to V_{DD}) to raise the voltage level at the node V_A . Therefore, the logic level stored at the node V_A can be changed from “1” to “0” to detect the EFT events. With the buffer inverters, the output voltage of the new proposed on-chip transient detection circuit is finally changed from 1.8 V to 0 V to memorize the occurrence of EFT-induced transient disturbance.

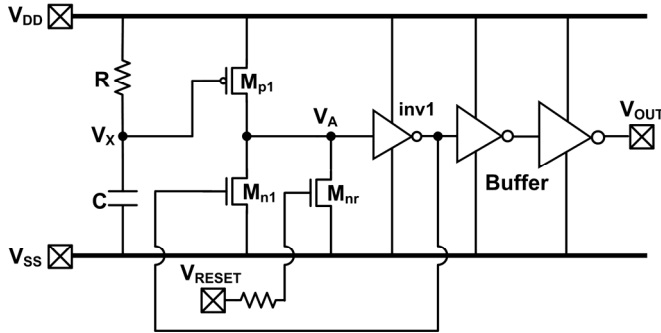


Fig. 2. The new proposed transient detection circuit.

B. HSPICE Simulation

From the measured electrical transient waveforms shown in Fig. 1, the approximated exponential voltage pulse waveforms during the EFT tests have been observed. Therefore, an exponential pulse time-dependent voltage source with rise/fall time constant parameters is used to simulate EFT-induced transient disturbance on the proposed transient detection circuit. The rising edge of this exponential time-dependent voltage pulse is expressed as

$$V_{p(\text{rise})}(t) = V_1 + (V_2 - V_1) \times \left[1 - \exp\left(-\frac{t - t_{d1}}{\tau_1}\right) \right], \text{ when } t_{d1} \leq t \leq t_{d2}. \quad (1)$$

The falling edge of this exponential time-dependent voltage pulse is expressed as

$$V_{p(\text{fall})}(t) = V_1 + (V_2 - V_1) \times \left[1 - \exp\left(-\frac{t - t_{d1}}{\tau_1}\right) \right] + (V_1 - V_2) \times \left[1 - \exp\left(-\frac{t - t_{d2}}{\tau_2}\right) \right], \quad (2)$$

when $t \geq t_{d2}$.

With the proper parameters (including the rise time constant τ_1 , fall time constant τ_2 , rise time delay t_{d1} , fall time delay t_{d2} , initial dc voltage value V_1 , and exponential pulse voltage value V_2), the exponential voltage pulse can be constructed to simulate the EFT-induced disturbance under EFT tests.

The simulated V_{DD} and V_{OUT} waveforms of the proposed on-chip transient detection circuit with positive and negative exponential pulse transient disturbance on V_{DD} line are shown in Figs. 3(a) and 3(b), respectively. From the simulated waveforms, V_{DD} begins to change rapidly from 1.8 V and acts with positive or negative exponential voltage pulse waveform during the simulated transient disturbance on power line. V_{OUT} is disturbed simultaneously during the EFT-induced disturbance in the simulation. After V_{DD} finally returns to its normal voltage level of 1.8 V, V_{OUT} will be changed from 1.8 V to 0 V, as shown in Figs. 3(a) and 3(b). Therefore, from the simulation results, the proposed transient detection circuit can detect and memorize the occurrence of EFT-induced exponential voltage pulse transient disturbance.

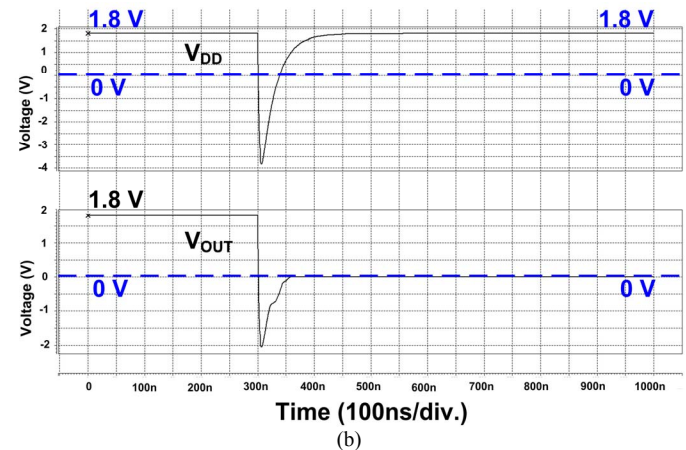
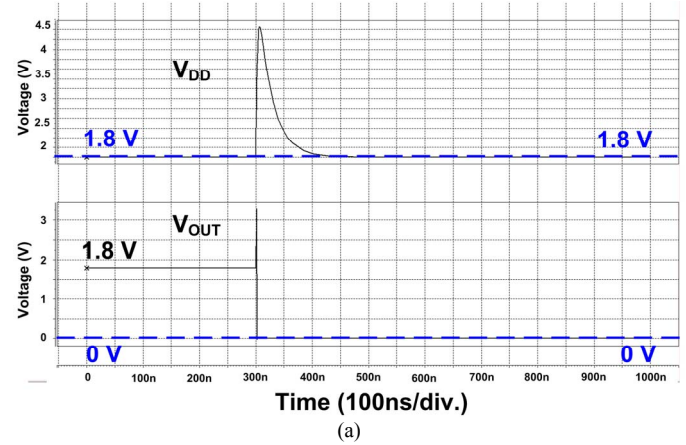


Fig. 3. Simulated V_{DD} and V_{OUT} waveforms of the new proposed transient detection circuit under EFT tests with (a) positive, and (b) negative, exponential voltage pulse waveforms coupled to V_{DD} .

III. EXPERIMENTAL RESULTS

According to the IEC 61000-4-4 standard [4], the simplified circuit diagram of the EFT generator is shown in Fig. 4. In particular, only the impedance matching resistor R_m (50 Ω) and the dc blocking capacitor C_d (10 nF) are fixed. The charging capacitor C_c is used to store the charging energy and R_s is used to shape the pulse duration. The EFT is a test with repetitive burst consisting of a number of fast pulses, coupled into power supply and signal ports of microelectronic products. With the repetition frequency of 5 kHz and 100 kHz, the burst repeats every 300 ms and the application time is not less than 1 minute.

In order to simulate the EFT-induced transient disturbance on CMOS ICs inside the microelectronic products, the attenuation network with -40 dB degradation is used in this work. The amplitude of EFT-induced transients can be adjusted through the attenuation network.

The measurement setup for EFT test combined with attenuation network is shown in Fig. 5. EFT generator is connected to the device under test (DUT) through the attenuation network with V_{DD} of 1.8 V. The V_{DD} and V_{OUT} transient responses of the proposed transient detection circuit are monitored by the digital oscilloscope. Before each EFT test, the initial output voltage (V_{OUT}) of the proposed transient detection circuit is reset to 1.8 V. After each EFT test, the output voltage (V_{OUT}) level is monitored to check the final voltage level and to verify the detection function.

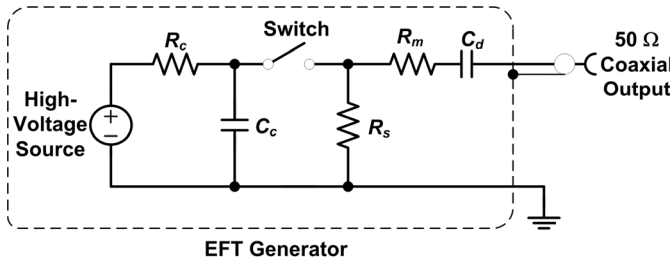


Fig. 4. Simplified circuit diagram of EFT generator.

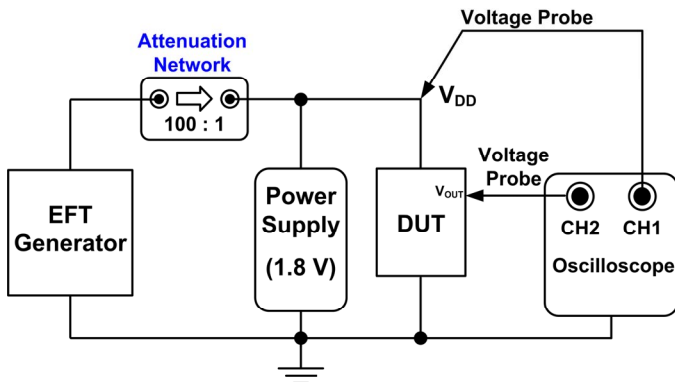


Fig. 5. Measurement setup for EFT test combined with attenuation network.

The measured V_{DD} and V_{OUT} waveforms of the on-chip transient detection circuit under EFT test with EFT voltage of +400 V are shown in Fig. 6(a). As shown in Fig. 6(a), under the EFT test with positive EFT voltage, V_{DD} begins to increase

rapidly from 1.8 V. Meanwhile, V_{OUT} starts to greatly increase with positive exponential voltage pulse coupled on V_{DD} power line. Finally, after the EFT-induced transient disturbance, the output voltage (V_{OUT}) of the on-chip transient detection circuit is changed from 1.8 V to 0 V. Therefore, the on-chip transient detection circuit can memorize the occurrence of the EFT event with positive EFT voltage.

The measured V_{DD} and V_{OUT} transient waveforms of the on-chip transient detection circuit under EFT test with EFT voltage of -600V are shown in Fig. 6(b). As shown in Fig. 6(b), under the EFT test with negative EFT voltage, V_{DD} begins to decrease rapidly from 1.8 V. V_{OUT} is disturbed simultaneously with negative exponential voltage pulse coupled on V_{DD} power line. Finally, after the negative EFT-induced transient disturbance, the output voltage (V_{OUT}) of the on-chip transient detection circuit transits from 1.8 V to 0 V.

From the EFT test results shown in Figs. 6(a) and 6(b), with positive or negative exponential voltage pulses coupled to V_{DD} power line, the new proposed on-chip transient detection circuit can successfully memorize the occurrence of EFT-induced transient disturbance events.

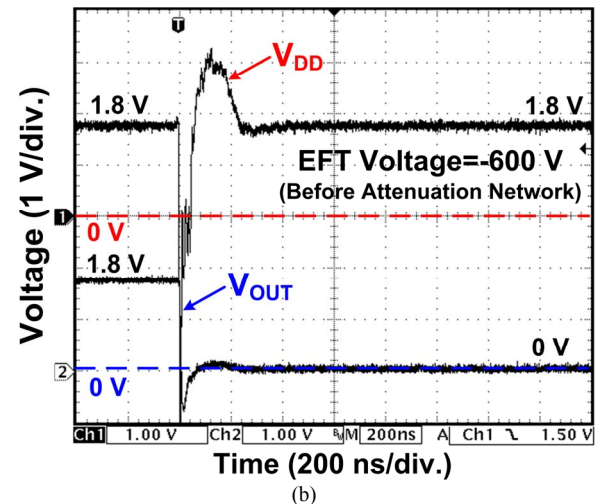
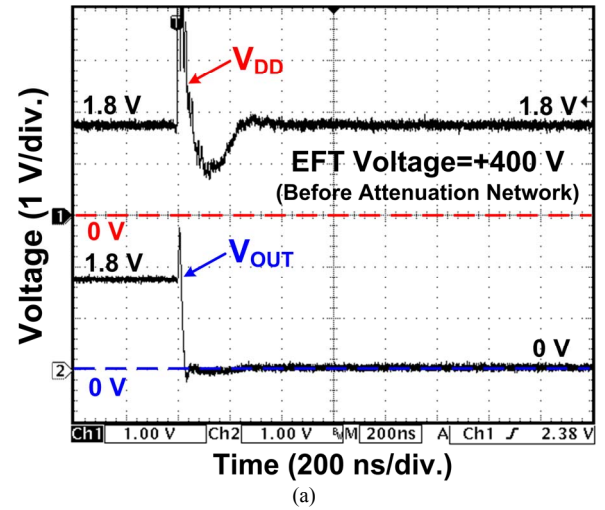


Fig. 6. Measured V_{DD} and V_{OUT} waveforms on the new proposed on-chip transient detection circuit under EFT tests with (a) positive, and (b) negative, EFT voltages combined with attenuation network.

IV. APPLICATION IN DISPLAY PANEL

It had been proven that the hardware/firmware co-design can effectively improve the robustness of the microelectronic products against electrical transient disturbance [12]. For display system with thin-film transistor (TFT) liquid crystal display (LCD) panel, multiple power supplies are needed for electrical display functions, as shown in Fig. 7. For example, in the backside of source driver IC, the analog power line (VDDA) is used for digital-to-analog converter circuit and digital power line (VDDD) is used for shifter register and memory units to store red, green, and blue (RGB) display signals.

In the hardware/firmware system co-design, the transient detection circuit is connected with 1.8-V VDDD power line to detect and memorize the occurrence of EFT-induced transient disturbance coupled on digital subsystems of display panel products. The detection results from the transient detection circuit can be temporarily stored as a system recovery index for firmware check, as shown in Fig. 7. In the beginning, the output (V_{OUT}) state of the transient detection circuit is initially reset to logic “1” by the power-on reset circuit. When the electrical transients happen, the transient detection circuit can detect the occurrence of EFT-induced electrical transient disturbance and transit the output state (V_{OUT}) to logic “0.” At this moment, the system recovery index is also changed to logic “0” to initiate automatic recovery operation to restore the microelectronic system to a desired stable state as soon as possible. After the automatic recovery operation, the output of the transient detection circuit and the system recovery index are re-set to logic “1” again for detecting the next EFT-induced electrical transient disturbance events.

By using the detection results as the firmware index, the display panel can automatically recover all electrical functions to release the locked or frozen states caused by EFT-induced transient disturbance. With such a hardware/firmware system co-design, the susceptibility of display panels against EFT tests can be effectively enhanced without additional operator manual intervention.

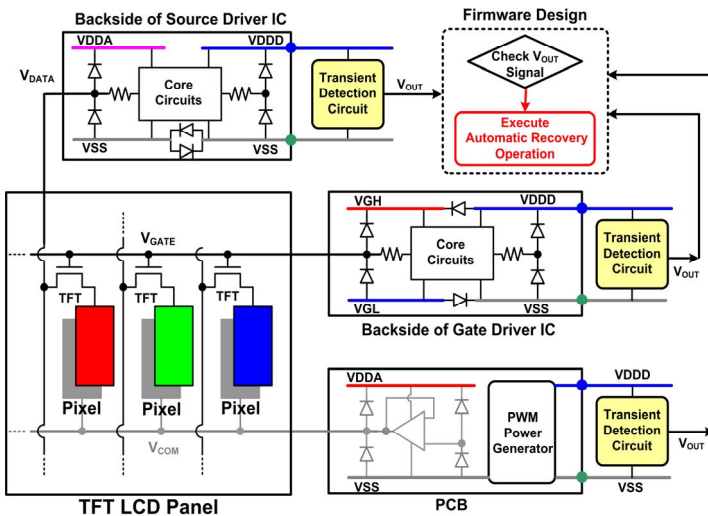


Fig. 7. Hardware/firmware system co-design on display system with TFT-LCD panel and the new proposed transient detection circuit.

V. CONCLUSIONS

A new on-chip transient detection circuit to detect EFT events has been proposed and successfully verified in a CMOS 0.13- μm process. The circuit performance under different positive and negative EFT-induced transient disturbance has been investigated by HSPICE simulation. The experimental results in silicon chip have confirmed that the proposed transient detection circuit can successfully detect and memorize the occurrence of fast electrical transients during EFT tests. The proposed transient detection circuit can be further combined with firmware design to provide an effective solution against the frozen or locked states in microelectronic display products caused by EFT-induced transient disturbance events.

REFERENCES

- [1] M.-D. Ker and S.-F. Hsu, *Transient-Induced Latchup in CMOS Integrated Circuits*, John Wiley & Sons, 2009.
- [2] C.-C. Yen, M.-D. Ker, and T.-Y. Chen, "Transient-induced latchup in complementary-metal-oxide-semiconductor integrated circuits under electrical fast transient test," *IEEE Trans. Device Mater. Reliab.*, vol. 9, no. 2, pp. 255–264, Jun. 2009.
- [3] G. Cerri, R. Leo, and V. Primiani, "Electrical fast-transient: conducted and radiated disturbance determination by a complete source modeling," *IEEE Trans. Electromagn. Compat.*, vol. 43, no. 1, pp. 37–44, Feb. 2001.
- [4] IEC 61000-4-4 Standard, "EMC – Part 4-4: Testing and Measurement Techniques – Electrostatic Fast Transient/Burst Immunity Test," 2004.
- [5] D. Liu, D. Pommerenke, S. Kwon, and K. Martwick, "Full wave model for simulating a noiseken ESD generator parameters," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, 2009, pp. 334–339.
- [6] J. Koo, L. Han, S. Herrin, R. Moseley, R. Carlton, D. Beetmer, and D. Pommerenke, "A nonlinear microcontroller power distribution network model for the characterization of immunity to electrical fast transients," *IEEE Trans. Electromagn. Compat.*, vol. 51, no. 3, pp. 611–619, Aug. 2009.
- [7] C. Rostamzadeh, H. Dadgostar, and F. Canavero, "Electrostatic discharge analysis of multi layer ceramic capacitors," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, 2009, pp. 35–40.
- [8] S. Marum, C. Duvvury, J. Park, A. Chadwick, and A. Jahanzeb, "Protecting circuits from the transient voltage suppressor's residual pulse during IEC 61000-4-2 stress," in *Proc. EOS/ESD Symp.*, 2009, pp. 377–386.
- [9] K. Muhonen, P. Erie, N. Peachey, and A. Testin, "Human metal model (HMM) testing, challenges to using ESD guns," in *Proc. EOS/ESD Symp.*, 2009, pp. 387–395.
- [10] E. Grund, K. Muhonen, P. Erie, and N. Peachey, "Delivering IEC 61000-4-2 current pulses through transmission lines at 100 and 330 ohm system impedances," in *Proc. EOS/ESD Symp.*, 2008, pp. 132–141.
- [11] M. Honda, "Measurement of ESD-gun radiated fields," in *Proc. EOS/ESD Symp.*, 2007, pp. 323–327.
- [12] M.-D. Ker and Y.-Y. Sung, "Hardware/firmware co-design in a 8-bits microcontroller to solve the system-level ESD issue on keyboard," in *Proc. EOS/ESD Symp.*, 1999, pp. 352–360.
- [13] M.-D. Ker and S.-F. Hsu, "Evaluation on board-level noise filter networks to suppress transient-induced latchup in CMOS ICs under system-level ESD test," *IEEE Trans. Electromagnetic Compatibility*, vol. 48, no. 1, pp. 161–171, Feb. 2006.
- [14] M. Montrose, *Printed Circuit Board Design Techniques for EMC Compliance*, IEEE Press, 2000.
- [15] M.-D. Ker, C.-C. Yen, and P.-C. Shin, "On-chip transient detection circuit for system-level ESD protection in CMOS ICs," in *Proc. IEEE Custom Integrated Circuits Conf.*, 2006, pp. 361–364.
- [16] C.-C. Yen, C.-S. Liao, and M.-D. Ker, "New transient detection circuit for system-level ESD protection," in *Proc. IEEE Int. Symp. VLSI Design, Automation and Test (VLSI-DAT)*, 2008, pp. 180–183.
- [17] M.-D. Ker, C.-S. Liao, and C.-C. Yen, "Transient detection circuit for system-level ESD protection and its on-board behavior with EMI/EMC filters," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, 2008.