On-Chip ESD Detection Circuit for System-Level ESD Protection Design

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Abstract

A new on-chip CR-based electrostatic discharge (ESD) detection circuit for system-level ESD protection design is proposed in this work. The circuit performance to detect positive or negative electrical transients generated by system-level ESD tests has been analyzed in HSPICE simulation and verified in silicon chip. The experimental results in a 0.13-μm CMOS process have confirmed that the proposed detection circuit can detect ESD-induced transient disturbance during system-level ESD zapping. The detection results can be used as system recovery firmware index to improve the immunity of CMOS IC products against system-level ESD stress.

1. Introduction

Recently, the system-level electrostatic discharge (ESD) events have become an important reliability issue in modern microelectronic circuits and systems [1]-[7]. It has been proven that, for PMOS and NMOS devices fabricated in advanced semiconductor technology, the system-level ESD-induced electrical transient disturbance can cause transient-induced latchup (TLU) failure on the inevitable parasitic silicon controlled rectifier (SCR) inside CMOS ICs. It has been also reported that, for keyboard controller and liquid crystal display (LCD) driver circuits, the underdamped sinusoidal voltage generated by system-level ESD tests can cause locked or frozen states in microelectronic products. This serious reliability issue results from not only the progress of more integrated functions into a single chip, such as mixed-signal, mixed-voltage, system-on-chip (SOC), etc., but also from the strict requirements of reliability test standards, such as the system-level ESD test standard of IEC 61000-4-2 [8]. Typically, if microelectronic products are required to achieve the immunity of "level 4" in the IEC 61000-4-2 standard, the equipment under test (EUT) should sustain the ESD stress level of as high as ±8 kV (±15 kV) under contact-discharge (air-discharge) test mode. For modern microelectronic products, some CMOS ICs are very susceptible to system-level ESD stress, even though they have passed the component-level ESD qualifications such as the human-body-model (HBM) of ±2 kV, the machine-model (MM) of ±200 V, and the charged-device-model (CDM) of ±1 kV.

In this work, a new on-chip CR-based ESD detection circuit is designed to detect fast electrical transients and verified in a 0.13-μm CMOS process. The experimental results have confirmed that the proposed detection circuit can successfully memorize the occurrence of transient disturbance under system-level ESD tests.

2. New Proposed ESD detection circuit

2.1 Circuit Implementation

Fig. 1 shows the new proposed on-chip CR-based ESD detection circuit. The CR-based circuit structure is designed to realize the transient detection function. The NMOS (M_{nr}) is used to provide the initial reset function to set the initial voltages at node V_{OUT} and node V_A as 1.8 V with the V_{DD} of 1.8 V in a 0.13-μm CMOS process. In Fig. 1, the node V_G is biased at V_{SS} during the normal operating condition. Under the system-level ESD stress with an overshooting ESD voltage, the node V_G will be coupled with positive voltage. Then, the NMOS device (M_{n1}) can be turned on by the overshooting ESD voltage to pull down the voltage level at the node V_A. Therefore, the logic level stored at the node V_A can be changed from logic "1" to logic "0" to memorize the system-level ESD event. With the buffer inverters, the output voltage of the new proposed on-chip CR-based ESD detection circuit is finally changed from 1.8 V to 0 V to detect the occurrence of system-level ESD events.

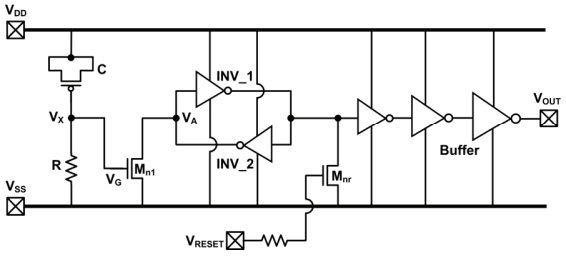

Figure 1. The proposed CR-based ESD detection circuit.

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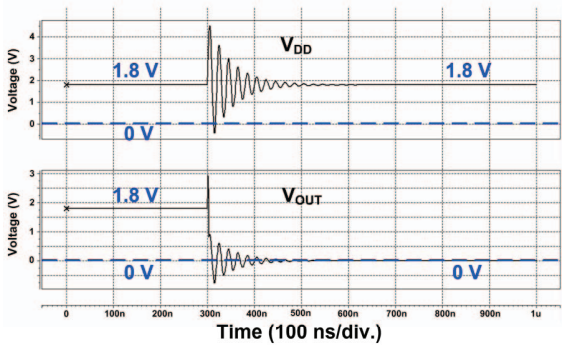
2.2 HSPICE Simulation

In HSPICE simulation, a sinusoidal time-dependent voltage source with damping factor parameter, given by

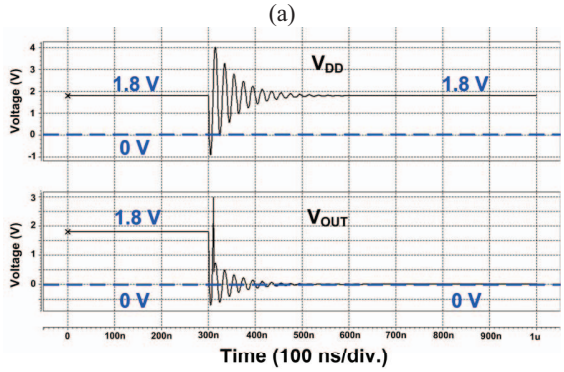
$$V(t) = V_0 + V_a \cdot \sin(2\pi f(t - t_d)) \cdot \exp(-(t - t_d)D_a), \quad (1)$$

is used to simulate the coupling transient voltage during the system-level ESD event. With the proper parameters (including the voltage amplitude V_a, initial dc voltage V_0, damping factor D_a, frequency f, and time delay t_d), the underdamped sinusoidal voltage can be used to simulate the electrical transient waveforms under system-level ESD tests.

The simulated V_{DD} and V_{OUT} waveforms of the proposed on-chip ESD detection circuit with positive-going and negative-going underdamped sinusoidal voltages on V_{DD} power lines are shown in Figs. 2(a) and 2(b), respectively. Under the simulated positive-going (negative-going) underdamped sinusoidal ESD stress condition, V_{DD} begins to increase (decrease) rapidly from 1.8 V. V_{OUT} is disturbed simultaneously during the V_{DD} disturbance. As a result, after V_{DD} finally returns to its normal voltage level of 1.8 V, V_{OUT} will be changed from 1.8 V to 0 V, as shown in Fig. 2(a) (Fig. 2(b)).



(a)



(b)

Figure 2. Simulated V_{DD} and V_{OUT} waveforms of proposed circuit under system-level ESD tests with (a) positive-going, and (b) negative-going, underdamped sinusoidal voltages.

3. System-Level ESD Test

The proposed CR-based ESD detection circuit has been designed and fabricated in a 0.13-μm 1P5M CMOS process. The fabricated chip is shown in Fig. 3.

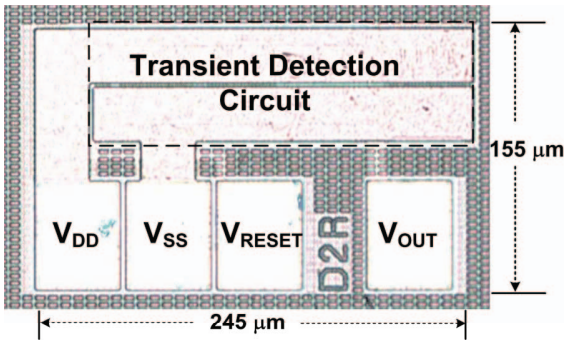


Figure 3. Die photo of the new proposed CR-based ESD detection circuit fabricated in a 0.13-μm CMOS process.

3.1 Measurement Setup

In the IEC 61000-4-2 standard [8], two test modes have been also specified, which are the air-discharge test mode and the contact-discharge test mode. Contact discharge is further divided into direct discharge to the system under test, and indirect discharge to horizontal or vertical coupling planes. The measurement setup of system-level ESD test with the indirect contact-discharge test mode in IEC 61000-4-2 standard is shown in Fig. 4. Horizontal or vertical coupling planes should be placed on the wooden table. An insulating plane should be inserted between the EUT/cables and horizontal coupling plane (HCP). The HCP is connected to the ground reference plane (GRP) with bleeder wire through two 470 kΩ resistors in series mounded on both ends of the wire. When the ESD gun zaps to the HCP, the transient voltage coming from ESD will be coupled into all CMOS ICs inside EUT. The operations of CMOS ICs inside EUT would be disturbed by the ESD-coupled energy.

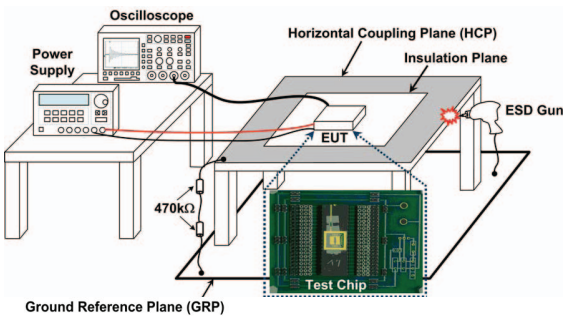


Figure 4. Measurement setup for a system-level ESD test with indirect contact-discharge test mode [8].

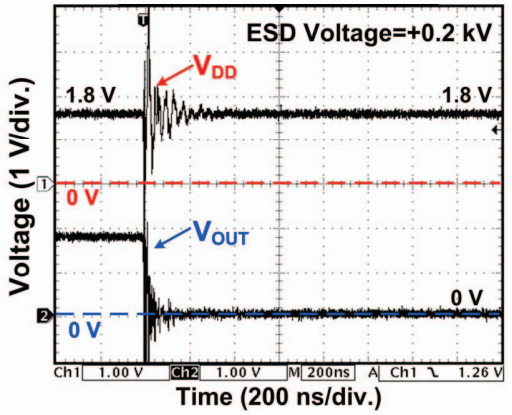
3.2 Measurement Results

The proposed on-chip CR-based ESD detection circuit has been designed and fabricated in a 0.13-μm CMOS process with 1.8-V devices. With measurement setup shown in Fig. 4, the circuit function of the proposed ESD detection circuit after system-level ESD tests can be evaluated. By using the digital oscilloscope, the transient responses on power lines of CMOS ICs can be recorded and analyzed. Before each system-level ESD test, the initial output voltage (V_{OUT}) of the ESD detection circuit is reset to 1.8 V. After each system-level ESD test, the output voltage (V_{OUT}) level is monitored to check the final voltage level and to verify the detection function. Thus, the circuit performance can be evaluated under system-level ESD test with indirect contact discharge mode.

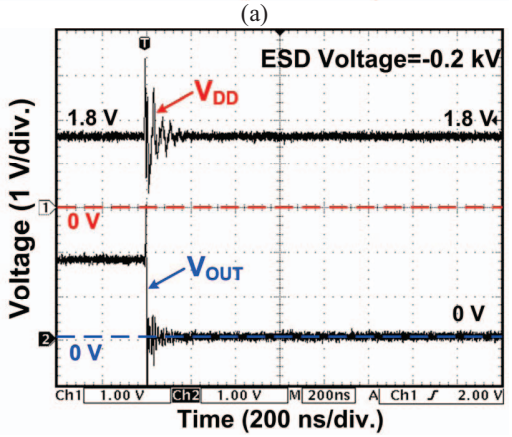
The measured V_{DD} and V_{OUT} waveforms of the fabricated ESD detection circuit under a system-level ESD test with the ESD voltage of +0.2 kV zapping on the HCP are shown in Fig. 5(a). V_{DD} begins to increase rapidly from the normal bias voltage of 1.8 V. Meanwhile, V_{OUT} begins to change under such a high-energy ESD stress. During the fast transient disturbance, V_{DD} and V_{OUT} are influenced simultaneously. Finally, when V_{DD} returns to its normal voltage level of 1.8 V, the output voltage of the ESD detection circuit has been changed from 1.8 V to 0 V. Therefore, the new proposed CR-based ESD detection circuit can sense the positive electrical transient on the power line and memorize the occurrence of system-level ESD event.

The measured V_{DD} and V_{OUT} transient waveforms of the detection circuit under system-level ESD test with an ESD voltage of -0.2 kV zapping on the HCP are shown in Fig. 5(b). During the ESD-induced transient disturbance, V_{DD} begins to decrease rapidly from the original bias voltage of 1.8 V and V_{OUT} is disturbed simultaneously. Finally, when V_{DD} returns to its normal voltage level of 1.8 V, V_{OUT} is pulled down to 0 V after the system-level ESD event. Therefore, the on-chip CR-based ESD detection circuit can successfully detect the electrical transients under system-level ESD tests with positive and negative ESD voltages.

The proposed ESD detection circuit has been practically applied to display panels of mobile phones to release the system locked or frozen states caused by ESD-induced transient disturbance under system-level ESD tests. In addition, by combining with different on-chip RC noise filter networks, the proposed on-chip CR-based ESD detection circuit can be further designed to become a transient-to-digital converter to detect different ESD voltage levels into digital thermometer codes under system-level ESD stress [3]. With higher ESD voltage level under system-level ESD tests, the transferred digital thermometer code goes higher.



(a)



(b)

Figure 5. Measured V_{DD} and V_{OUT} responses with ESD zapping voltages of (a) +0.2 kV, and (b) -0.2 kV.

4. Application in Display Panel

It had been proven that the hardware/firmware co-design can effectively improve the robustness of the microelectronic products against electrical transient disturbance [7]. For display system with thin-film transistor (TFT) liquid crystal display (LCD) panel, multiple power supplies are needed for electrical display functions, as shown in Fig. 6. For example, in the backside of source driver IC, the analog power line (VDDA) is used for digital-to-analog converter circuit and digital power line (VDDD) is used for register and memory units.

In the hardware/firmware system co-design, the CR-based ESD detection circuit is connected with 1.8-V VDDD power line to detect and memorize the occurrence of ESD-induced transient disturbance coupled on digital subsystems of display panel products. The detection results from the CR-based ESD detection circuit can be temporarily stored as a system recovery index for firmware check, as shown in Fig. 6. In the

beginning, the output (V_{OUT}) state of the ESD detection circuit is initially reset to logic "1". When the electrical transients happen, the ESD detection circuit can detect the occurrence of ESD-induced electrical transient disturbance and transit the output state (V_{OUT}) to logic "0." At this moment, the firmware index is also changed to logic "0" to initiate automatic recovery operation to restore the display system to a stable state as soon as possible.

Under system-level ESD zapping with air discharge test mode, the measurement results on TFT-LCD display panel without and with hardware/firmware system co-design are shown in Figs. 7(a) and 7(b), respectively. By using the detection results as the firmware index, the display panel can automatically recover all electrical functions to successfully release the locked or frozen states caused by system-level ESD transient disturbance, as shown in Fig. 7(b).

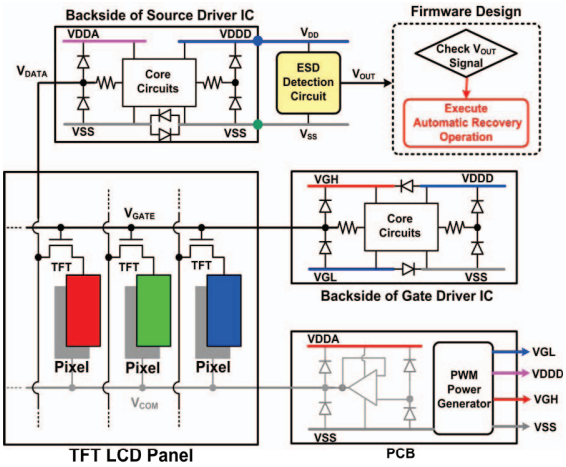
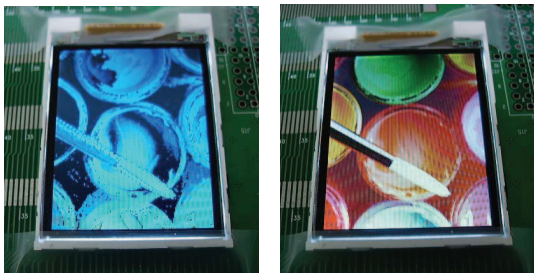


Figure 6. Hardware/firmware system co-design on TFT-LCD panel display system with the new proposed CR-based ESD detection circuit.



(a) (b)

Figure 7. Measurement results on TFT-LCD display panel (a) without, and (b) with, hardware/firmware system co-design under system-level ESD zapping.

5. Summary

A new on-chip CR-based ESD detection circuit to memorize the occurrence of system-level ESD events has been proposed and successfully verified in a CMOS 0.13-μm process. The circuit performance under different positive and negative ESD-induced transient disturbance has been investigated by HSPICE simulation. The experimental results in silicon chip have confirmed that the proposed ESD detection circuit can successfully detect and memorize the positive/negative fast electrical transients under system-level ESD tests.

Acknowledgments

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