Optimized Layout on ESD Protection Diode with Low Parasitic Capacitance

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Abstract

The diode operated in forward-biased condition has been widely used as an effective on-chip electrostatic discharge (ESD) protection device at GHz RF and high-speed I/O pads in CMOS integrated circuits (ICs) due to the small parasitic loading effect and high ESD robustness. Based on waffle layout style, two modified layout styles have been proposed, which are called as multi-waffle and multi-waffle-hollow layout styles. Experimental results in a 90-nm CMOS process have confirmed that the figures of merit (FOMs) of ESD protection diodes with new proposed layout styles can be successfully improved.

1. Introduction

Electrostatic discharge (ESD) has become the major concern of reliability for integrated circuits (ICs) in nanoscale CMOS technology. The thinner gate oxide and shallower diffusion junction seriously degraded the ESD robustness of ICs and raised the difficulty of ESD protection design for ICs in nanoscale CMOS technology [1]. In order to sustain the required ESD level, the ESD protection devices must be drawn with large device dimension. However, the parasitic capacitance (C_{ESD}) of the devices with large device dimension will obviously degrade the circuit performance [2]. Therefore, the C_{ESD} of the ESD protection devices must be minimized but the ESD robustness is kept at the reasonable level [3].

A typical on-chip ESD protection scheme for GHz RF or high-speed I/O applications is shown in Fig. 1, where the dual-diode circuit has been widely adopted for on-chip ESD protection due to the highest value of current-sinking per unit capacitance. The layout style of ESD protection diode will directly affect its ESD robustness and parasitic capacitance. In previous studies [4]-[5], the ESD protection diodes realized in the waffle layout style have been verified to achieve better FOMs, which is suitable to GHz RF and high-speed I/O applications.

Generally, the most important figures of merit (FOMs) used to evaluate the performance of the ESD protection diode is I_{CP}/C_{ESD}, where I_{CP} is the current level at which the measured I-V curve deviates from its linearly extrapolated value by 20% [6]. Consequently, it is desired to implement the ESD protection diode with a large ratio of I_{CP}/C_{ESD}. It is better for the ESD protection diode to achieve higher I_{CP} and lower C_{ESD} at the specific layout area.

In this work, the ESD protection diodes realized in waffle, multi-waffle, and multi-waffle-hollow layout styles are fabricated in a 90-nm CMOS process. According to the measured results, the ESD protection diodes with new modified layout styles can successfully improve the FOMs to make the diodes more adequate to GHz RF and high-speed I/O applications.

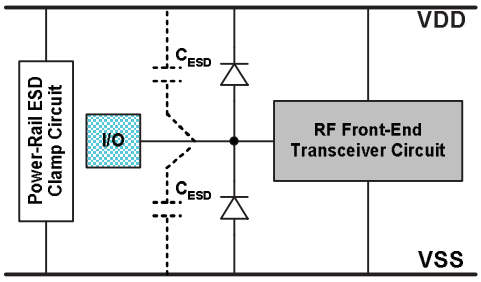

Figure 1. Typical ESD protection scheme with double diodes for RF front-end or high-speed I/O applications.

2. ESD Protection Diodes

2.1 Waffle Layout Style

The device layout top view of the ESD protection diode with waffle layout style is shown in Fig. 2(a). The waffle diode has been proposed in previous works [6]-[7]. For the $N+/P_{sub}$ diode, The N+ diffusion region is surrounded by a P+ diffusion region. In order to obtain different current-handling capability of the diode, multiple waffle diodes can be joined in parallel to form an array structure.

2.2 Multi-Waffle and Multi-Waffle-Hollow Layout Styles

The two new proposed diodes investigated in this study are illustrated in Figs. 2(b) and 2(c), which are called as the multi-waffle and multi-waffle-hollow layout styles, respectively. The multi-waffle layout style is formed from waffle layout style. The P+ diffusion region extends into the N+ diffusion region from four sides. The junction area can be theoretically reduced by a factor of 44%. Besides, the junction perimeter can also be increased by a factor of 67% at the same time. The multi-waffle-hollow layout style is formed from multi-waffle layout style by removing the N+ central diffusion region of $N+/P_{sub}$ diodes. The purpose is to reduce the junction area and to keep the junction perimeter at the same time. To form the hollow layout style, the N+ central diffusion region is removed to directly reduce the junction area of the diode. The ESD discharging current can be effectively concentrated in the remaining N+ diffusion region of the diode.

The major layout parameters of those $N+/P_{sub}$ diodes are listed in Table I, where the different spacings are also marked in Fig. 2.

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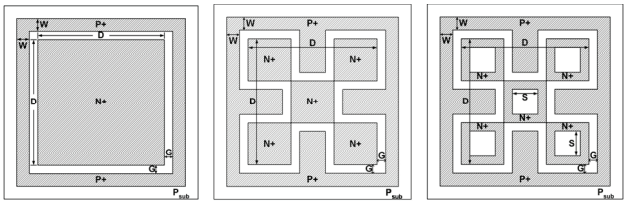

(a) (b) (c)

Figure 2. Layout top views of the ESD diodes with (a) waffle, (b) multi-waffle, and (c) multi-waffle-hollow layout styles.

Table 1. Measured device characteristics of diode under different layout styles

Layout Style	Size	Dimensions of Device (μm)	Array	Junction Perimeter (μm)	Junction Area (μm^2)	Layout Area, A_{Layout} (μm^2)
Waffle	A	W=0.22, D=0.56, G=0.34	5x1	11.2	1.57	14.11
	B	W=0.22, D=1.12, G=0.34	5x1	22.4	6.27	25.09
	C	W=0.22, D=2.24, G=0.34	5x1	44.8	25.09	56.45
	D	W=0.22, D=3.36, G=0.34	5x1	67.2	56.45	100.35
	E	W=0.22, D=4.20, G=0.34	5x1	84.0	88.20	141.51
	F	W=0.22, D=5.04, G=0.34	5x1	100.8	127.01	189.73
Multi-waffle	D	W=0.22, D=3.36, G=0.34	5x1	112.0	31.36	100.35
	E	W=0.22, D=4.20, G=0.34	5x1	140.0	49.00	141.51
	F	W=0.22, D=5.04, G=0.34	5x1	168.0	70.56	189.73
Multi-waffle-hollow	D	W=0.22, D=3.36, S=0.34, G=0.34	5x1	112.0	28.47	100.35
	E	W=0.22, D=4.20, S=0.62, G=0.34	5x1	140.0	39.39	141.51
	F	W=0.22, D=5.04, S=0.90, G=0.34	5x1	168.0	50.31	189.73

3. Experimental Results

Under normal circuit operation, the diode is kept off under the reverse-biased condition. Although the diode is turned off, there is still an intrinsic junction capacitance of the diode seen by the signals at the I/O pad. On the other hand, the diode should be turned on to discharge ESD current at forward-biased condition under ESD stresses. Therefore, the junction capacitance of the diode at reverse-biased condition and the ESD protection capability of the diode at forward-biased condition are important characteristics to be investigated.

3.1 Parasitic Capacitance

The diode devices are arranged with ground-signal-ground (G-S-G) pads to facilitate on-wafer two-port *S*-parameter measurement. During the *S*-parameter measurement, the N+ and P+ diffusion regions of the diode devices are connected to port 1 and port 2, respectively, and they are both biased at 0V.

In order to extract the characteristics of the intrinsic device at high frequency, the parasitic effects of the pad must be de-embedded [8]. The measured Y_{11}-parameter can be obtained from the measured two-port *S*-parameters by

$$Y_{11} = \frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{Z_0((1+S_{11})(1+S_{22})-S_{12}S_{21})}, \quad (1)$$

where Z_0 is the termination resistance of 50Ω. The measured *Y*-parameter of the including-DUT pattern is labeled as $Y_{11\text{-meas}}$, and the measured *Y*-parameter of the excluding-DUT pattern is labeled as $Y_{11\text{-open}}$. The intrinsic device characteristics, $Y_{11\text{-DUT}}$, can be obtained by subtracting $Y_{11\text{-open}}$ from $Y_{11\text{-meas}}$. The C_{ESD} of each diode can be extracted from the $Y_{11\text{-DUT}}$ by

$$C_{ESD} = \frac{Im(Y_{11-DUT})}{2\pi f}, \quad (2)$$

where *f* is the operating frequency. The extracted C_{ESD} of the ESD diodes from 4 to 5GHz under zero DC bias are listed in Table II and shown in Fig. 3.

From the measured results of the waffle, multi-waffle, and multi-waffle-hollow diodes, the extracted C_{ESD} are practically proportional to the N+ junction area. When the diodes are modified from waffle to multi-waffle and multi-waffle-hollow layout styles, the contribution of parasitic sidewall capacitance would be gradually emerged due to increased junction perimeter. Therefore, the C_{ESD} of the multi-waffle and multi-waffle-hollow diodes in Fig. 3 are larger than that of waffle diode. Compared to the waffle diodes in size D ~ F, the reductions of C_{ESD} can be achieved to 33%, 34%, and 36% (32%, 39%, and 46%) for the multi-waffle diodes (multi-waffle-hollow diodes), respectively. The great reduction of C_{ESD} is the major factor to significantly improve the FOMs of the diodes with new modified layout styles.

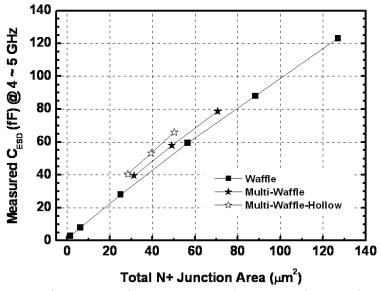

Figure 3. Dependence of C_{ESD} on the total N+ junction area of the diode devices with different layout styles.

Table 2. Measured results and FOMs of diode devices with different layout styles

Layout Style	Size	C_{ESD} (fF)	I_{CP} (A)	R_{ON} (Ω)	I_{2} (A)	V_{HBM} (kV)	R_{ON}*C_{ESD} (Ω·fF)	I_{CP}/C_{ESD} (mA/fF)	V_{HBM}/C_{ESD} (V/fF)	I_{CP}/A_{Layout} (mA/μm²)
Waffle	A	2.84	0.158	10.148	0.178	0.3	28.82	55.63	105.63	11.20
	B	8.01	0.416	3.980	0.476	0.8	31.88	51.94	99.88	16.58
	C	28.10	1.243	1.427	1.494	2.5	40.10	44.23	88.97	22.02
	D	59.44	2.100	0.871	2.361	3.8	51.77	35.33	63.93	20.93
	E	88.00	2.777	0.738	2.890	4.8	64.94	31.56	54.55	19.62
	F	123.09	3.328	0.694	3.536	5.5	85.42	27.04	44.68	17.54
Multi-waffle	D	39.56	1.862	0.819	2.252	3.7	32.40	47.07	93.53	18.56
	E	58.02	2.722	0.699	3.096	5.1	40.56	46.91	87.90	19.24
	F	78.76	3.561	0.601	3.902	6.5	47.33	45.21	82.53	18.77
Multi-waffle-hollow	D	40.51	1.790	0.821	2.229	3.6	33.26	44.19	88.87	17.84
	E	53.31	2.531	0.709	3.017	5.0	37.80	47.48	93.79	17.89
	F	66.03	3.258	0.620	3.752	6.2	40.94	49.34	93.90	17.17

3.2 Transmission Line Pulsing (TLP) Measurement

TLP generator is utilized to obtain the device behavior during high ESD current stress [9]. The on-resistance (R_{ON}), It_2, and I_{CP} of the diodes under forward-biased condition were characterized and listed in Table II. Apparently, the R_{ON} is decreased and the I_{CP} is increased with the increased N+ junction perimeter. Fig. 4 shows the I_{CP} versus the total N+ junction area of the diodes with different layout styles.

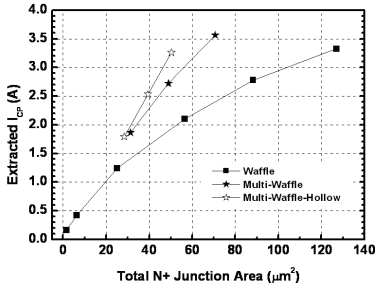

Figure 4. Dependence of extracted I_{CP} on the total N+ junction area of diodes with different layout styles.

3.3 FOM Comparison and Discussion

The FOMs of the ESD diodes are listed in Table II. The R_{ON} and C_{ESD} of the ESD diode are highly demanded to be small to effectively clamp the voltage and to minimize the degradation of circuit performance. Therefore, the R_{ON}*C_{ESD} is a useful justification and illustrated in Fig. 5. In the figure, the values of the diodes with new modified layout styles in size D can be comparable to that of waffle diodes in small size.

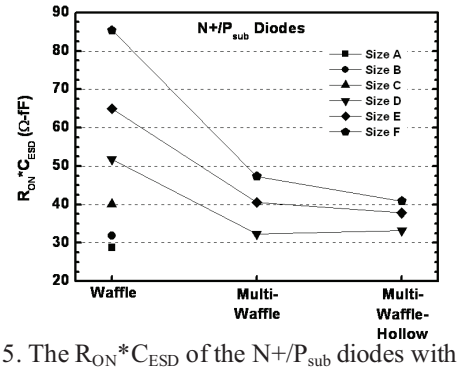

Figure 5. The R_{ON}*C_{ESD} of the N+/P_{sub} diodes with different layout styles.

The most important FOM of I_{CP}/C_{ESD} of the diodes with different layout styles is shown in Fig. 6. It is obvious that the I_{CP}/C_{ESD} of the diodes with new modified layout styles can be greatly improved to the range where is quite comparable to that of waffle diodes in small size. Based on the Figs. 5 and 6, the characteristics of the diodes in large size can be improved to the level of waffle diodes in small size by adequately modifying the layout style.

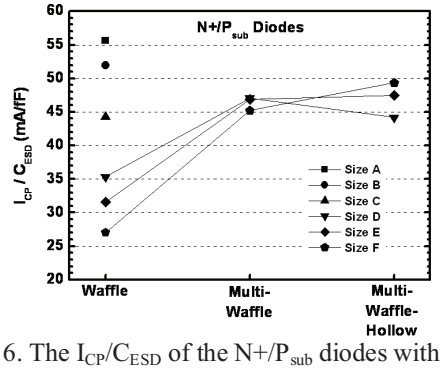

Figure 6. The I_{CP}/C_{ESD} of the N+/P_{sub} diodes with different layout styles.

Another design concern for the circuit applications is layout area. In advanced CMOS technology, the fabrication cost per die area is getting higher and higher. Therefore, the biggest concern of some ESD designers might be to save the layout area of the protection circuit but to sustain required ESD robustness. The values of I_{CP}/A_{Layout} of the diodes with different layout styles are shown in Fig. 7. In the figure, the value of the waffle diode in size A is obviously the smallest. For the diodes with new modified layout styles, the values of I_{CP}/A_{Layout} are within the range from 17 to 19mA/μm^2.

Although the waffle diode in small size theoretically has larger ratio of junction perimeter to total junction area, the size of waffle diode is still required to be carefully optimized. The penalties of parasitic sidewall capacitance and significant reduction on I_{CP} for the waffle diode in small size are gradually emerged. Therefore, it should not to simply shrink the device size of waffle diode for achieving better FOMs. Among the waffle diodes, the ones in size B and size C are more suitable to be implemented to the high-speed I/O circuits. Meanwhile, the diodes with new modified layout styles also can perform as well as those waffle diodes in size B and size C.

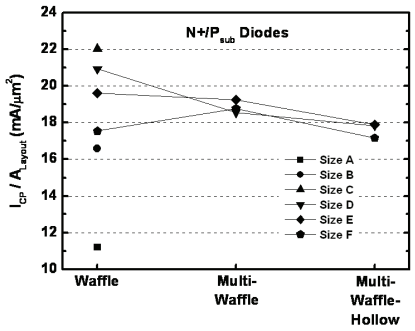

Figure 7. The I_{CP}/A_{Layout} of the N+/P_{sub} diodes with different layout styles.

4. Conclusion

The ESD diodes with new modified layout styles, multi-waffle and multi-waffle-hollow, have been successfully verified in a 90-nm CMOS technology. They are characterized in terms of some FOMs (R_{ON}*C_{ESD}, I_{CP}/C_{ESD}, and I_{CP}/A_{Layout}) to evaluate the suitability for high-speed I/O applications. The new proposed diodes in large size can avoid the penalty of local heat distribution. The reduction of junction area by using new modified layout styles is the key factor to significantly improve the FOMs of the diodes. As compared to the FOMs of waffle diodes, it reveals that the large size diodes can be enhanced by modifying the layout styles. Therefore, the proposed multi-waffle and multi-waffle-hollow diodes are also suitable for high-speed I/O circuits.

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