CDM ESD Protection Design With Initial-On Concept in Nanoscale CMOS Process

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***Abstract* - Integrated circuits (ICs) have been fabricated with thinner gate oxides to achieve higher speed and lower power consumption in nanoscale CMOS processes. However, the charged-device-model (CDM) electrostatic discharge (ESD) events became more critical because of the thinner gate oxide in nanoscale CMOS transistors and the larger die size for the system-on-chip (SoC) applications. Thus, effective on-chip ESD protection design against CDM ESD stresses has become more challenging to be implemented. A novel on-chip ESD protection design against CDM ESD events was proposed in this work, and its performance has been verified by the silicon chip fabricated in 55-nm CMOS process.**

I. Introduction

Transistors have been scaled down to improve circuit performances with the decreased power supply in the nanoscale CMOS technology. However, the thinner gate oxide of the transistors in nanoscale CMOS technology seriously degrades the electrostatic discharge (ESD) robustness of IC products [1], [2]. Among the three chip-level ESD test standards, which are human body model (HBM), machine model (MM), and charged device model (CDM), CDM becomes more and more critical [3], [4]. The CDM ESD event happens as a certain pin of the IC is suddenly grounded, and the electrostatic charges originally stored within the IC will be discharged through the grounded pin. The thinner gate oxide causes a lower gate-oxide breakdown voltage, and an IC with larger die size can store more static charges, which leads to larger discharging current during CDM ESD events. As compared with HBM and MM ESD events, the discharging current in CDM ESD event is larger and faster.

The CDM failure normally happens across the gate oxide over source or bulk in the MOS devices, as shown in Fig. 1 [5]. Although the circuit is equipped with ESD clamp devices at its input pad and the separated V_{SS} lines, it still suffers CDM ESD issue, because the ESD clamp device may not be efficiently turned-on to protect the gate oxide of the internal circuits during CDM ESD events. The ESD protection design against not only HBM and MM but also CDM ESD events is needed for all IC in the advanced CMOS process. In this paper, some CDM ESD protection design techniques are reviewed in section II. To further improve the CDM ESD robustness, a new ESD protection design is proposed and realized in a 55-nm CMOS process. The theory for CDM improvement and the experimental results of this novel design are provided in the sections III and IV, respectively.

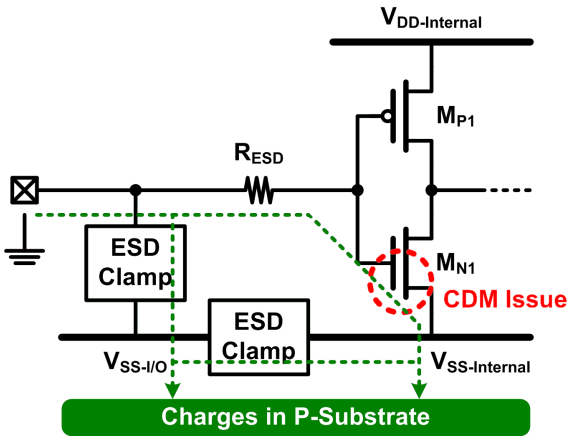

Fig. 1. CDM ESD issue in an input buffer.

II. Prior Designs against CDM ESD Events

Against CDM ESD failure, the ESD protection design with the additional deep N-well structure is shown in Fig. 2 [6]. By using the deep N-well structure in the NMOS of the input buffer, the stand-along P-well has a much smaller silicon area compared to the whole P-substrate of the chip, and the CDM charges in the stand-along P-well have a much lower amount than those in the P-substrate. Therefore, the NMOS of input buffer can prevent from CDM damages. However, the additional mask and process steps are needed for the deep N-well layer, which leads to the higher chip cost.

The other method against CDM ESD failure is to add a small ESD clamp device beside the gate of the input buffer, as shown in Fig. 3 [7]. The small ESD clamp device can be a gate-grounded NMOS (GGNMOS) to clamp the CDM ESD overstress voltage across the gate of the input buffer.

To improve ESD robustness of the input stage with thin gate oxide in nanoscale CMOS process, as well as to extend the design window of ESD protection circuits, the source pumping design has been used to reduce the ESD overstress voltage across the gate-to-source terminal in the NMOS of input stage under CDM ESD events. The design against CDM ESD failure with the self-biased current trigger (SBCT) design and source pumping is shown in Fig. 4, which employed additional NMOS

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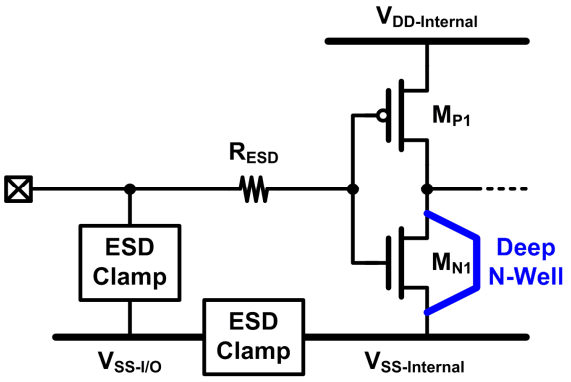

Fig. 2. Deep N-well isolating technique to prevent from CDM ESD stress.

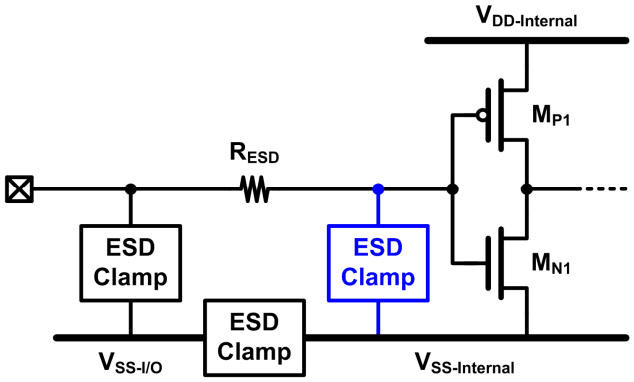

Fig. 3. Traditional CDM ESD protection with local clamp added to the gate of input stages.

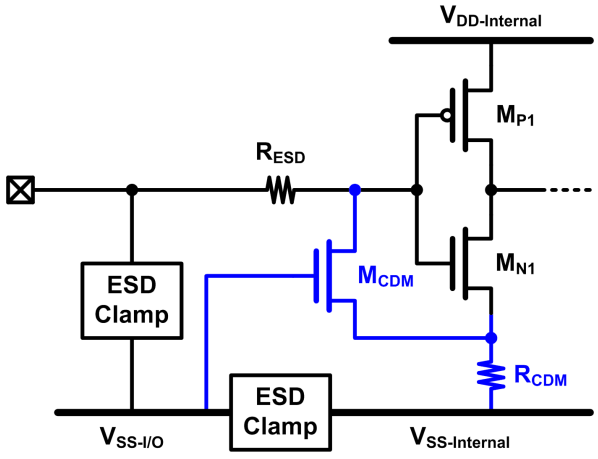

Fig. 4. Traditional CDM ESD protection of the self-biased current trigger (SBCT) design with source pumping.

device (M_{CDM}) in conjunction with a source pumping resistor (R_{CDM}) [8]. The drain terminal of the additional NMOS is connected to the input pad through an input series resistance (R_{ESD}). The source terminal of the additional NMOS device is connected to the internal V_{SS} line ($V_{SS\text{-}Internal}$) through the pumping resistor. In addition, the source terminal of the input NMOS (M_{N1}) is also connected to $V_{SS\text{-}Internal}$ line through the same resistor. Under CDM ESD events, the gate terminal of the additional NMOS device can be biased by CDM ESD current discharging through the ESD clamp between $V_{SS\text{-}I/O}$ and $V_{SS\text{-}Internal}$ lines. The gate oxide of the input NMOS can be protected by the additional NMOS with self-biased current trigger design and the pumping resistor under CDM ESD stresses.

III. New Proposed Design against CDM ESD Events

A. Initial-On Concept

The discharging current in CDM ESD event is not only larger but also much faster than that in HBM and MM ESD events. In order to effectively protect the core circuits from CDM ESD damages, the turn-on speed of ESD protection circuits is wished to be as fast as better. The initial-on ESD protection concept was ever presented in the literature to effectively protect the core circuits against HBM and MM ESD stresses [9]. The initial-on concept could be further applied to the CDM ESD protection design. The PMOS ESD clamp device is initially on as the IC is floating without any power bias, but the PMOS ESD clamp device is kept off as the IC is in the normal circuit operation conditions.

With the initial-on concept, Figs. 5(a) and 5(b) show the new proposed designs A and B, respectively. The proposed CDM ESD protection designs are implemented by additional PMOS device (M_{CDM}) in conjunction with source pumping resistor (R_{CDM}). When the input pad is suddenly grounded under CDM ESD events, the electrostatic charges originally stored within the substrate can be quickly discharged through the initial-on PMOS device to the grounded input pad. Fig. 6 shows the discharging paths of the design B under CDM stress events. Under normal circuit operating condition, the gate voltage of the additional PMOS device is biased at logic high (V_{DD}), and this ESD device is kept off.

B. Test Circuit Implementation

A reference input stage circuit, as shown in Fig. 1, without CDM ESD protection is drawn. Its ESD clamp devices at input pad and the separated V_{SS} lines are composed of the GGNMOS and back-to-back diodes, respectively. Another input stage circuit with the local GGNMOS for CDM ESD protection is drawn with the sizes of 2.5- and 20-μm for ESD verification. The prior design of the self-biased current trigger (SBCT) NMOS is drawn with the sizes of 2.5-, 10-, and 20-μm under the 100-Ω pumping resistor. The new proposed designs A and B are also drawn with the sizes of 2.5-, 10-, and 20-μm under the same 100-Ω pumping resistor. All these circuits have been fabricated in a 55-nm CMOS process with the thin-gate oxide of ~20 Å.

C. Simulation Results

The aforementioned CDM ESD protection circuits with additional 15-μm MOS and 100-Ω pumping resistor under CDM-like stresses are simulated. Fig. 7 shows the simulated voltage of the CDM ESD protection circuits under the CDM-like transitions, where the ± 5 V voltage pulses with rise time of 0.3 ns are applied between I/O pin and P-substrate to simulate the fast transient voltage of CDM ESD event. With a

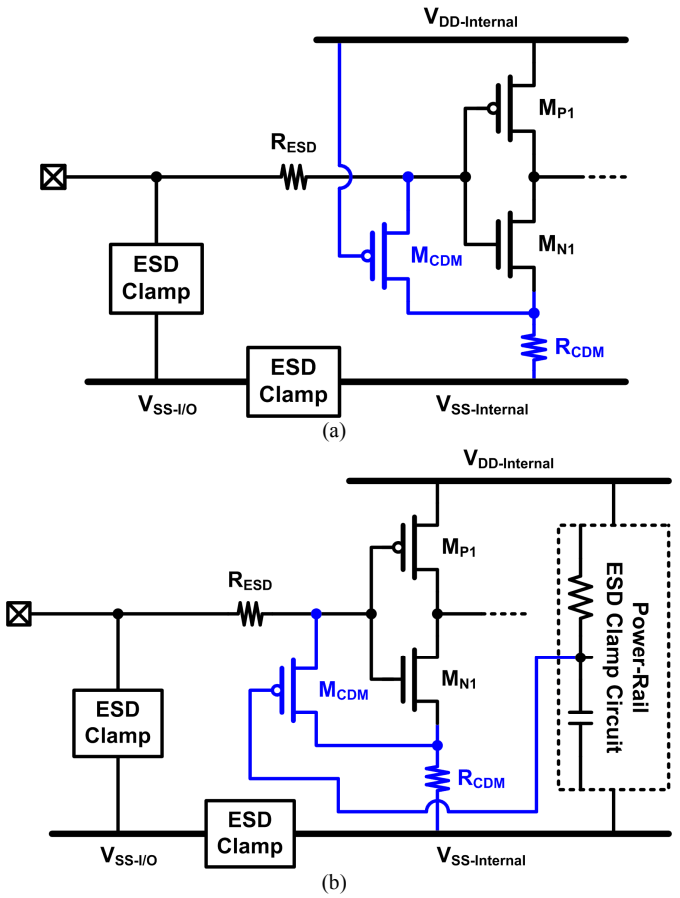

Fig. 5. The new proposed CDM ESD protection (a) design A, and (b) design B, with the initial-on concept and source pumping resistor.

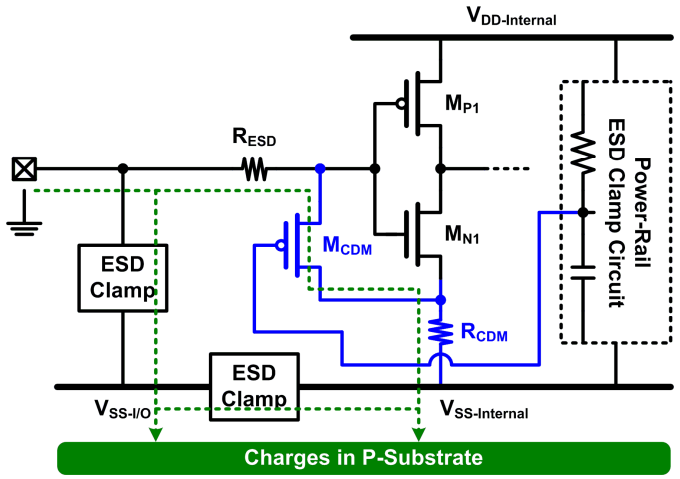

Fig. 6. CDM ESD current discharging paths in the CDM ESD protection with proposed design B under CDM ESD stresses.

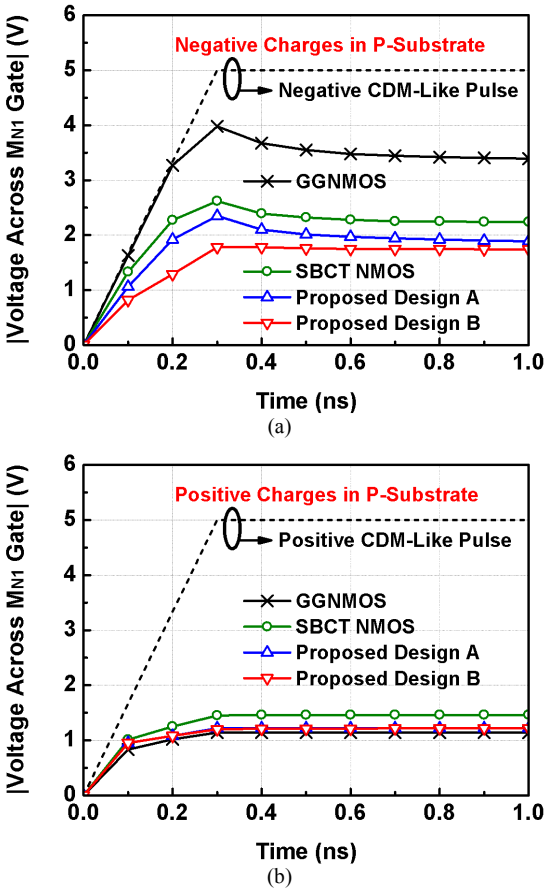

Fig. 7. HSPICE-simulated voltages across the input NMOS gate of all test circuits under (a) negative, and (b) positive, 0-to-5 V CDM-like pulse between P-substrate and input pin.

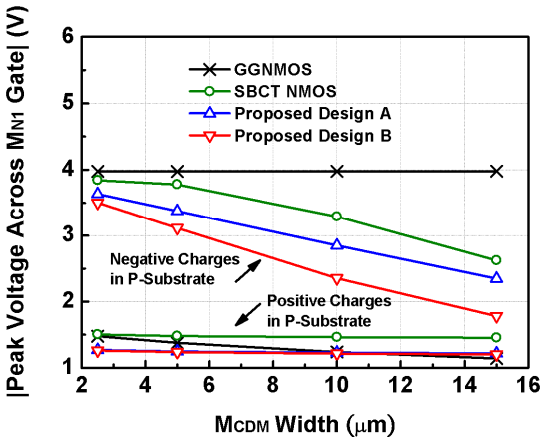

Fig. 8. Comparison on the simulated transient peak voltages among the CDM ESD protection designs with different MOS widths (M_{CDM}) under negative and positive CDM-like pulses.

limited voltage height of 5 V in the voltage pulse, the voltage drop across the input NMOS gate of all test circuits can be simulated to check the clamping performance before device breakdown. The transient voltage peak of all CDM ESD protection circuits with different MOS widths under negative and positive CDM-like events are compared in Fig. 8. Under positive CDM ESD events, the peak voltages across the gate are lower, since the CDM currents can be discharged through the forward-biased parasitic diode paths in the additional MOS devices. Under negative CDM ESD events, the new proposed CDM ESD protection designs have the lower clamped voltage to effectively protect the core circuits.

IV. Experimental Verification in Silicon

The aforementioned test circuits have been fabricated in a 55-nm CMOS process and assembled in DIP-40-pin package. The CDM ESD stresses are applied by the field-induced CDM tester with socket. The failure criterion is 30% shift of the leakage current under 1-V V_{DD} bias from its original level. CDM ESD robustness among these test circuits are listed in Table I ~ IV, and these results are also compared in Fig. 9. The negative CDM ESD level of the input stage without any additional CDM ESD protection design is lower than 100 V. With the additional GGNMOS or SBCT NMOS, the CDM ESD robustness can be slightly improved to 100 or 300 V. The input stage with the new proposed design A or B can sustains 400- or 500-V CDM ESD stresses, which performs the best CDM ESD robustness in this experimental silicon chip.

V. Conclusion

New CDM ESD protection circuits realized with the initial-on concept and source pumping resistor have been successfully verified in a 55-nm CMOS process. Without any extra process steps in nanoscale CMOS technology, such CDM ESD protection designs can provide efficient CDM ESD protection for input stages of CMOS ICs.

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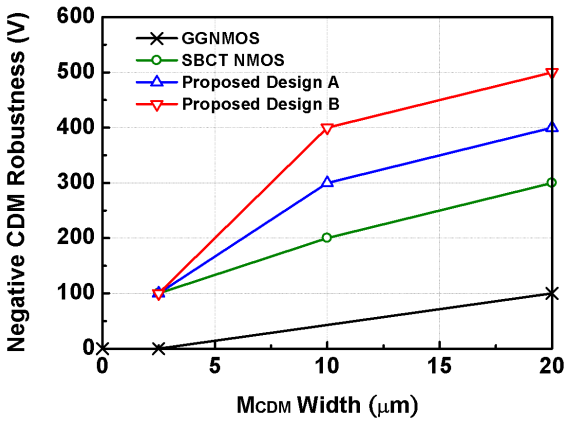

Fig. 9. Summary on negative CDM ESD test results in silicon chip.

Table I
CDM ESD robustness of the traditional protection design with GGNMOS.

M_{CDM} (GGNMOS) Width	Positive CDM	Negative CDM
0 μm	100 V	< 100 V
2.5 μm	200 V	< 100 V
20 μm	600 V	100 V

Table II
CDM ESD robustness of the traditional protection design with self-bised current trigger mechanism and source pumping.

M_{CDM} (SBCT NMOS) Width	Positive CDM	Negative CDM
2.5 μm	200 V	100 V
10 μm	400 V	200 V
20 μm	600 V	300 V

Table III
CDM ESD robustness of the protection with proposed design A.

M_{CDM} (PMOS) Width	Positive CDM	Negative CDM
2.5 μm	200 V	100 V
10 μm	400 V	300 V
20 μm	600 V	400 V

Table IV
CDM ESD robustness of the protection with proposed design B.

M_{CDM} (PMOS) Width	Positive CDM	Negative CDM
2.5 μm	200 V	100 V
10 μm	400 V	400 V
20 μm	600 V	500 V